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Chapter 6

Application of one-dimensional metal oxide semiconductor in field effect transistor

Fengyun Wang and Hongliang Zu

One-dimensional metal oxide nanostructures, especially nanowires (NWs) and nanofibers (NFs), due to their excellent physical and chemical properties, exhibit unique optical, electrical, chemical, thermal, and magnetic properties, making them suitable for the next-generation, high-performance electronic products. In this article, we will introduce the development and application of one-dimensional metal oxide field effect transistors (FETs), summarize the characteristics of different kinds of metal oxide FET and the methods to improve their performance, and discuss various application areas. Finally, the challenges and development prospects of metal oxide (NW) transistors are discussed, including the investigation of material properties, and the design and application of device structures.

6.1 Introduction

Two-dimensional metal oxide thin film materials have great value in scientific research and practical applications and have been successfully applied to thin film transistor (TFT) devices. However, as science and technology applications have progressed, two-dimensional thin-film materials have been found to have some shortcomings. The electron transmission path of two-dimensional thin-film semiconductor materials is not fixed [1], which leads to the scattering of electrons in the channel and reduces the carrier mobility of the device. Additionally, the specific surface area of the dimensional thin film material is small, which severely limits the application of any device it constitutes to detect gas and photoelectrons. One-dimensional metal oxides with unique, short electron transport channels and large specific areas have become the focus of research, and are being widely applied in the areas of logic circuits, photoelectric detectors, gas detectors and other fields [2–21].

In this article, we will summarize the latest progress in high-performance metal oxide nanowire field-effect transistors (NWFETs) [22], covering all aspects from

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basic materials to important applications. In section 6.2, we will briefly introduce the preparation of metal oxide NWs, and in section 6.3, we will introduce the basic physical principles of one-dimensional metal oxide semiconductor FETs. After that, in section 6.4, various FETs, manufactured using different metal oxide NWs or NFs, are introduced. In section 6.5, several examples of metal oxide NWFETs used in different fields will be discussed. Finally, at the end of the article, we summarize the existing problems and future developmental directions of metal oxide NWFETs.

6.2 Preparation of one-dimensional metal oxide materials

Since the preparation of carbon nanotubes by Dr Iijima in Japan in 1991, the study of one-dimensional materials has attracted great attention from experts and scholars in the fields of materials, physics, and chemistry. One-dimensional nanostructures have the characteristics of surface and interface effects, small size effects, quantum size effects, and macroscopic quantum tunneling effects, and they exhibit unique properties applicable in the fields of optics, electricity, thermodynamics, and magnetism. Compared with two-dimensional thin-film materials, one-dimensional metal oxide semiconductor nanomaterials have a directional electron transmission path and a large specific surface area. Therefore, one-dimensional metal oxide semiconductor nanomaterials were prepared with suitable forbidden band widths, large carrier concentrations, and good stability. Metal oxide semiconductor nanomaterials have become a research hot topic. The current methods for preparing one-dimensional metal oxide semiconductor nanomaterials are chemical vapor deposition, the sol–gel method, the solvo-thermal method, molecular beam epitaxy, and electrospinning [23].

6.2.1 Chemical vapor deposition

Chemical vapor deposition (CVD) is a relatively new technology for preparing inorganic materials [24]. Chemical vapor deposition has been widely used to purify substances, develop new crystals, and deposit various single crystal, polycrystalline, or glassy inorganic materials. These materials can be oxides, sulfides, nitrides, or carbides and binary or multi-element compounds in the groups III–V, II–IV, IV–VI. The doping process can also be precisely controlled. CVD has become a new field of inorganic synthetic chemistry [23, 25–28].

CVD technology is a process that uses gaseous substances to produce chemical and transport reactions on solids, thus producing the solid deposits [2–4], as shown in figure 6.1. It generally includes three steps:

1. Formation of volatile substances;
2. Transfer of these substances to the deposition area;
3. Production of chemical reactions on solids to produce solid deposits.

Metal oxides are one of the synthesized compounds. One-dimensional metal oxide nanostructures can be easily synthesized using CVD technology. Nano-sized metal catalysts are used in CVD technology to grow one-dimensional metal oxide nanostructures. The diameter or width of the one-dimensional metal oxide

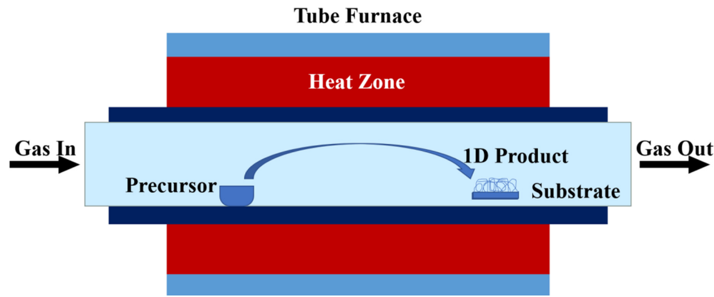

Figure 6.1. Schematic of a tube furnace for CVD synthesis of 1D nanostructures.

nanostructure depends largely on the size of the nanoscale metal catalyst. The structural morphology of the one-dimensional metal oxide nanostructures is related to the substrate temperature, molecular surface diffusion rate, and the concentration of metal and oxygen vapor.

Based on this knowledge of CVD, metal organic chemical vapor deposition (MOCVD) technology has been developed. MOCVD can reduce the deposition temperature for the growth of one-dimensional metal oxide nanostructures. MOCVD technology has the advantages of thickness control, precise doping, large area deposition and morphological diversity. Most CVD synthesis techniques can only provide autocatalytic growth or layer-by-layer growth of one-dimensional metal oxide nanostructures.

6.2.2 Sol–gel technique

The sol–gel method uses a compound containing a highly chemically active component as a precursor. These raw materials are uniformly mixed in the liquid phase. Then hydrolysis and condensation chemical reactions are preformed to stabilize the transparent sol system in solution [2–4, 23]. The colloidal particles slowly polymerize to form a three-dimensional network structure, and the solvent loses fluidity to form a gel. The gel is dried, sintered and solidified to prepare molecular and even nano-substructure materials. Sol–gel technology can be used to synthesize one-dimensional metal oxide nanostructures. The precursors are alkali metal oxides or metal salts, such as chlorides, nitrates and acetates, usually surrounded by various reactive ligands. Therefore, the precursor can undergo various hydrolysis and condensation reaction processes. The raw materials in the sol are processed to form dispersed metal oxides in contact with liquid water or dilute acid. Removal of the liquid water or dilute acid from the sol produces a gel, and the sol/gel transition controls the particle size and shape. For example, the calcination of a gel produces metal oxides. Figure 6.2 shows how a colloidal suspension (sol) of an alkali metal oxide or metal salt is dissolved in a solute. Hydrolysis and condensation occur in the sol when poured onto the rotating substrate. As the sol rotates, hydrolysis and condensation proceed outward. As the sol gradually turns into a gel, the colloidal suspension coalesces to form a 1D nanostructure by self-assembly. The gel can be heated to

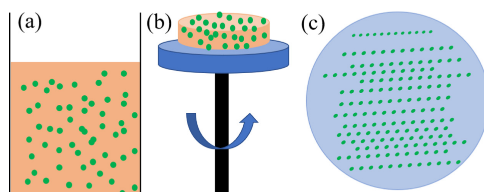

Figure 6.2. Schematic diagrams of the sol–gel technique: (a) the colloidal suspension in the sol is represented by green spots; (b) sol is spun to form a gel; and (c) after the heat treatment 1D metal-oxide nanostructures grow on the substrate.

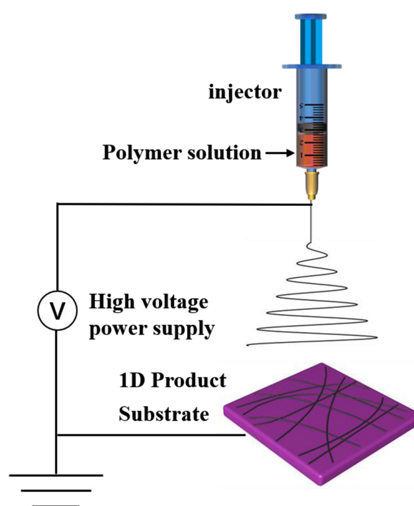

Figure 6.3. Schematic diagram of one-dimensional nanostructure prepared by electrospinning.

completely remove the liquid water or dilute acid, thus forming a one-dimensional metal oxide nanostructure.

6.2.3 Electrospinning technology

Electrostatic spinning equipment is mainly composed of three parts: a propulsion pump, a high-voltage power supply, and a receiving substrate, as shown in figure 6.3. The propulsion pump pushes the liquid out of the syringe, the droplet is stretched into a wire under the action of a high-voltage power supply, and then received by the receiving substrate. Electrospinning technology can not only be used to prepare nanofibers, but also nanotubes, core–shell structures, multi-wall nanofibers, nanoflowers and other similar nanostructures [29–35]. Electrospinning technology has the advantages of simple operation, low cost, high efficiency and large output. The prepared nanofibers are widely used in the fields of catalysis, energy, and electronic devices due to the advantages of larger specific surface areas, better stability and uniform morphology [35–41].

The configuration of the precursor solution determines the spinning quality. In general, *N*,*N*-dimethylformamide (DMF), alcohol, or deionized water, are usually

used. In addition, it is necessary to add a polymer as a binder to the precursor to control the viscosity. The proper viscosity is a necessary condition for fiber formation and is very important for the formation of nanofibers. In the preparation of inorganic nanofibers, the following polymers are commonly used: polyvinylpyrrolidone (PVP), polylactic acid (PLA), polyvinyl alcohol (PVA), etc.

Compared with other technologies, electrospinning has the following advantages: (1) large area nanofiber thin layers can be prepared. (2) The prepared fiber has a very large specific surface area. (3) The method is simple, only a high-voltage power supply, propulsion pump and receiving substrate are necessary. (4) The cost is low. No precious metal is needed as a catalyst, and no subsequent photolithography technology is needed to prepare the electrode. (5) It is easy to uniformly incorporate other elements. Just add the doping metal salt to the precursor solution. These advantages make electrostatic spinning technology very suitable for the preparation of electronic devices and optoelectronic devices.

6.3 Basic principle of one-dimensional metal oxide semiconductor FET

The one-dimensional metal oxide semiconductor FET is a field effect transistor that uses one-dimensional metal oxide as a conductive channel, and controls the current of the NW by controlling the voltage of the gate [42, 43]. The basic structure is shown in figure 6.4.

Laid out from top to bottom are the source and drain electrodes, the semiconductor layer, the dielectric layer and the gate. The FET is a three-terminal device, that is, the opening and closing of the device is controlled by three electrodes, the source electrode, the drain electrode, and the gate electrode [44]. For enhanced n-channel FETs, where only a certain voltage value V_{DS} is added between the source and drain electrodes, the current in the transistor is very small or nonexistent. The concentration of freely moving carriers in the semiconductor layer is very low, so the current generated by the voltage is very low. The lowest current generated at this

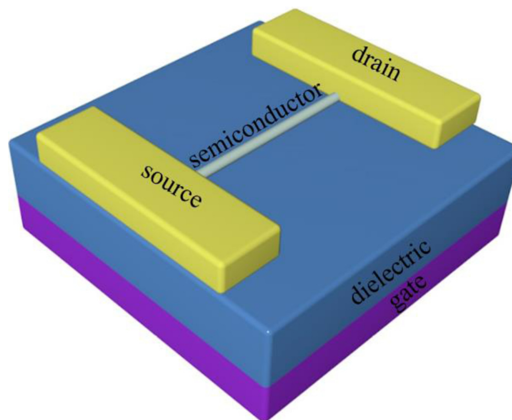

Figure 6.4. Schematic diagram of NW-FET structure.

time is called the off-state current of the FET. Therefore, to make the transistor work, a voltage V_{GS} is added between G and S and a voltage V_{DS} is added between D and S. When a bias is applied to the gate, the dielectric layer will form a capacitor, and carriers will be induced between the semiconductor layer and the node dielectric layer by the applied voltage. In this way, carriers will now move from the source to the drain, forming a current between the source and drain electrodes. The current channel is close to the interface between the semiconductor layer and the dielectric layer. The channel length (L) is defined as the distance between the source electrode and the drain electrode, and the channel width (W) is defined as the total length of the source electrode and the drain electrode in parallel. The channel is generally located a few nanometers above the dielectric layer, and its thickness is extremely narrow, which plays a crucial role in the performance of the transistor. The interface between the semiconductor layer and the dielectric layer is very important [45, 46].

There are six main evaluation parameters of FET performance: threshold voltage (V_{TH}), off-state current (I_{off}), on-state current (I_{on}), switching ratio (I_{on}/I_{off}), carrier mobility (μ), and sub-threshold swing (SS). The V_{TH} usually refers to the input voltage corresponding to the midpoint of the transition area where the output current in the transfer characteristic curve changes abruptly as the input voltage changes. The V_{TH} can be the value of V_{TH} at the intersection of the tangent and the V_G axis in the relationship curve between the square root of the current ${I_{DS}}^{1/2}$ and V_G. The V_{TH} of an ideal FET should be 0 V, but in there will always be deviations. In practical applications, there will be a high carrier concentration in the semiconductor or a current between the semiconductor and the interface of the dielectric layer sub-traps which will cause the V_{TH} to be positive or negative from time to time. When $V_{TH} < 0$ V, the device is in depletion mode (D-mode) and when $V_{TH} > 0$ V, the device is in enhancement mode (E-mode). Turning off a D-mode device requires an application of a negative pressure. Thus, a D-mode device consumes more energy than the E-mode device. The current switching ratio (I_{on}/I_{off}) represents the ratio of the on-state current to the off-state current. Since the transistor has a switching function in the circuit, the current switching ratio of an excellent transistor should be $I_{on}/I_{off} = 10^6$ or higher. Carrier mobility refers to the average drift velocity of carriers (electrons and holes) under the action of a unit electric field. In the different semiconductor material, carrier types are different, and mobility is different. Generally, the mobility of electrons is higher than that of holes. Mobility mainly affects two properties of transistors. First, the carrier concentration determines the conductivity (reciprocal of resistivity) of semiconductor materials. The greater the mobility, the smaller the resistivity. When passing the same current, the power consumption is smaller, and the current carrying capacity is greater. Second, the rate of carrier mobility also affects the refresh rate of the device. When the mobility is small, it can be used in devices with low refresh frequency requirements, such as e-books. High mobility is useful in some high-end devices, such as TVs, computers, and some screens used in eSports. The SS value is equal to the gate voltage increment ΔV_G required to change the current I_{DS} by an order of magnitude. Note that SS is extracted from the maximum slope on the V_G–I_D curve. It indicates the rise rate of

the $\tilde{I_D}V_G$ relationship curve. In order to increase the operating speed of the sub-threshold region of the transistor, the smaller the SS value, the better.

6.4 Individual one-dimensional metal oxide NW transistors

6.4.1 Binary metal oxide NW transistor

6.4.1.1 ZnO NW transistors

ZnO has excellent optical and electrical properties, has received great attention in the fields of electronics, optoelectronics and piezoelectric electronics, and is one of the most outstanding materials in the metal oxide family. ZnO is a direct gap wide band gap compound semiconductor material with a band gap width of 3.37 eV at room temperature [47]. It has a wurtzite structure and belongs to a hexagonal system of point groups. ZnO can produce high-efficiency ultraviolet laser emissions at room temperature, and has broad application prospects in the field of short-wavelength optical devices [26, 48–52]. ZnO is also a piezoelectric and thermoelectric semiconductor material with good performance. Because of its piezoelectric and photoelectric effects, ZnO nanofibers are widely used in electrical, optical, and detector devices, and are further made into photodetectors, gas detectors, and filters [13, 15, 17, 29, 31, 43, 47, 53–55].

Although significant progress has been made in the use of ZnO NWs in high-performance and low-cost electronic products, due to the large surface roughness and granular structure of the obtained NFs, they still suffer from insufficient device performance. It should be noted, Wang *et al* proposed a simple one-step electrospinning process to obtain a controllable ZnO NW network of high-performance, large-scale, low-power TFTs [31]. By precisely controlling the annealing temperature during the manufacturing process, the crystallinity, grain size distribution, surface morphology, etc can be reliably adjusted to enhance the performance of the transistor. An annealing temperature of 500 °C produces a device with a positive threshold voltage (V_{TH}) of approximately 0.9 V, a low leakage current of approximately 10^{-12} A and an excellent on/off current ratio 10^6. This is one of the best performing ZnO NF devices reported so far. When high-κ AlO_x films are used as the gate dielectric, the source/drain voltage (V_{DS}) can be reduced by a factor of 10 to only 0.3 V. These results indicate the potential of these nanofibers in next-generation low-power devices (figure 6.5) [31].

6.4.1.2 In_2O_3 NW transistors

In_2O_3 is a new n-type transparent semiconductor material with a wide band gap (direct band gap of about 3.6 eV and indirect band gap of about 2.5 eV), small resistivity, and high catalytic activity. It is widely used in the field of optoelectronics, gas sensors, catalysts, solar cells, and diodes. In_2O_3 has higher electron mobility and carrier concentration than other semiconductor materials and has better conductivity. When In_2O_3 nanofibers are built into transistors, the carrier mobility range is about 70–250 $cm^2\ V^{-1}\ s^{-1}$. However, the current switching ratio is one order of magnitude lower than that of ZnO semiconductor. Because In_2O_3 semiconductors

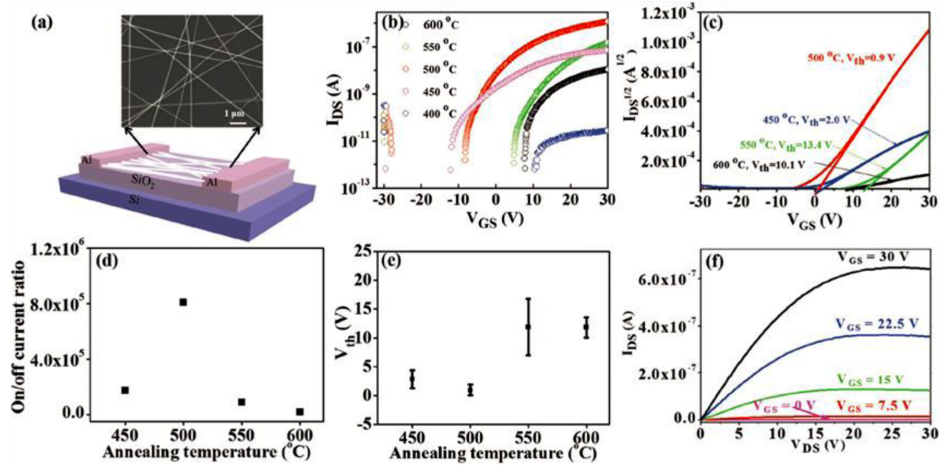

Figure 6.5. (a) Top: SEM image and bottom: model of a typical back-gated ZnO NFTFT fabricated with Al electrodes and heavily doped silicon substrates covered with 300 nm thick SiO_2. (b) The transfer curves, (c) V_{TH}, (d) average on/off current ratio, and (e) average V_{TH} of ZnO NFTFTs annealed at different temperatures. (f) The output curves of ZnO NFTFT annealed at 500 °C. [31] John Wiley & Sons. © 2018 WILEY-VCH Verlag GmbH & Co., KGaA, Weinheim.

have lower off-state currents due to lower resistivity, the switching ratio is about 10^3 to 10^6 [56, 57].

At the same time, In_2O_3 semiconductor nanomaterials also have good optical transmittance, and their transmittance in the visible light region generally exceeds 80% and 90%. Thus In_2O_3 is an ideal material for preparing transistors [13, 29–31]. Park *et al* prepared In_2O_3 nanofibers by electrospinning [58]. After annealing to remove the polymer, a bottom-gate top-contact FET was prepared. The transistor showed typical n-channel properties. In order to improve the performance of the transistor, insulating zirconia (ZrO_2) was used in a double-layer structure of a NW network. ZrO_2 has a high binding energy with oxygen which is helpful in reducing the oxygen-related defects in the NW. The resulting transistor has a high current switching ratio, high carrier mobility, small sub-threshold swing (figure 6.6) [58].

6.4.1.3 SnO_2 NW transistors

SnO_2 is also an n-type semiconductor material with a forbidden band width of 3.6 eV, a square rutile structure, a transmittance of 80% in the visible and infrared regions, and good chemical stability [48]. It was the first commercially available transparent conductive material. Due to the small size effect, quantum size effect, surface effect and macroscopic quantum tunneling effect, SnO_2 nanomaterials show significant changes to its physical properties in regards to light [59], heat, electricity, sound, magnetism, and other macroscopic properties compared with traditional SnO_2. The carriers of a SnO_2 semiconductor mainly comes from crystal defects, such as oxygen vacancies and electrons provided by the doping impurities [15, 16, 48, 59, 60].

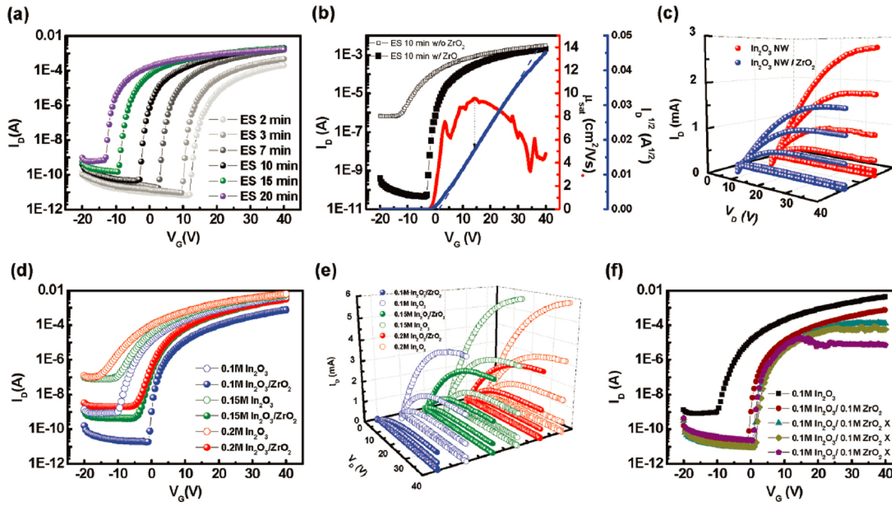

Figure 6.6. (a) Transfer characteristics of the hybrid In_2O_3 nanowire/ZrO_2 thin film FET as a function of electrospinning time. (b) Transfer characteristics and (c) output characteristics of bare In_2O_3 nanowire FET and nanowire/ZrO_2 film FET after the optimized collecting time (10 min). (d) Transfer and (e) output characteristics of single In_2O_3 channel and In_2O_3/ZrO_2 bilayer channel TFTs as a function of the In_2O_3 thickness. (f) Transfer characteristics of 0.1 m In_2O_3 TFTs with different thickness of ZrO_2 films. [58] John Wiley & Sons. © 2018 WILEY-VCH Verlag GmbH & Co., KGaA, Weinheim.

Wang *et al* have grown SnO_2 NWs on sapphire substrates by using a vapor–liquid–solid (VLS) process in a low-pressure chemical vapor deposition system [61]. The length of these parallel NWs can reach 100 μm. The fabricated transistor had an on/off current ratio of 10^6, a carrier mobility of about 71.68 cm^2 V^{-1} s^{-1} and a sufficiently high current to drive an external organic light-emitting diode display. Not only is the device sensitive to ultraviolet light, it can distinguish between 254 and 365 nm wavelengths of light, and detect NO_2 with a concentration of 0.2 ppb (figure 6.7) [61].

6.4.2 Ternary metal oxide NW transistor

With the continuous development of NW transistors, the disadvantages of binary metal oxides have been gradually revealed. In_2O_3 semiconductors are a good example. Although they have excellent electrical and optical properties, transistors based on In_2O_3 semiconductor nanofibers have many disadvantages: high leakage current, low current switching ratio, and negative threshold voltage. This leads to poor device performance and energy consumption. At this time, the electrical properties of NWs can be adjusted by introducing other metal elements to improve the performance of the transistor [15].

In order to improve the performance of In_2O_3 NW transistors, Zhang *et al* prepared Mg-doped In_2O_3 NWs by electrospinning. The produced a high-performance enhanced FET [29]. The performance of the transistor can be controlled by simply adjusting the Mg content in the NW. At the optimal Mg concentration of

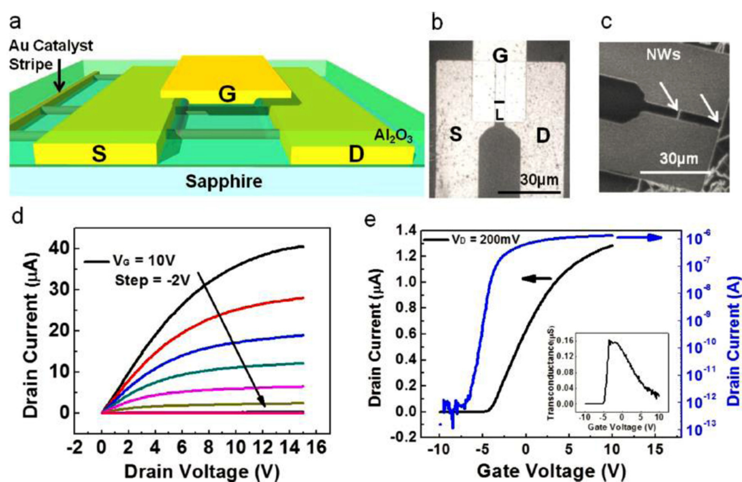

Figure 6.7. Aligned SnO_2 nanowire transistor study. (a) Diagram of device fabrication. (b) Top-view optical image of an aligned SnO_2 nanowire transistor. (c) SEM image of two aligned SnO_2 nanowires bridging the source and drain electrodes of a nanowire transistor. (d) $I_D - V_D$ family plot of the transistor shown in (c). (e) $I_D - V_G$ plot of the transistor in (c) plotted with standard scale in black and logarithmic scale in blue. The subplot shows the transconductance of the same device. Reprinted with permission from [61]. Copyright (2014) American Chemical Society.

2 mol%, the device carrier mobility is 2.04 $cm^2\ V^{-1}\ s^{-1}$, the current switching ratio is greater than 10^8 and the threshold voltage is 3.2 V (figure 6.8) [29].

Due to various shortcomings of single metal element oxides, Song *et al* doped Sr into indium oxide NWs by the electrospinning method to improve the electrical properties, thereby effectively controlling the carrier concentration in indium oxide NFs [30]. By simply controlling the concentration of Sr, In_2O_3 NFs with controllable electrical properties were obtained. Using 3.6 mol% Sr-In_2O_3 NFs as the channel material, an enhancement mode (E mode) FET was successfully constructed. By doping the Sr element, the off-state current of the device was not only reduced by at least 5 orders of magnitude, and the threshold voltage was adjusted to 0.3 V, but also its stability was improved. The carrier mobility of the device was 3.67 $cm^2\ V^{-1}\ s^{-1}$, the threshold voltage was between 0 and 5 V, and the current switching ratio was 10^7 to 10^8. In addition, when Al_2O_3 is used as a dielectric layer, the operating voltage is reduced to one-tenth of the original. This not only reduces costs and energy consumption, but also the stability of the equipment stays very high. Moreover, when a resistive load inverter is paired with the completed device, there is a good voltage gain. These results show that the preparation of NFs by the electrostatic spinning method has broad application prospectives in electronic products with low cost, low energy consumption, high efficiency and high performance (figure 6.9) [30].

6.4.3 Quaternary metal oxide NW transistor

Although amorphous IGZO materials have been widely used in various thin film transistor (TFT) applications, their device performance is still limited by inherent

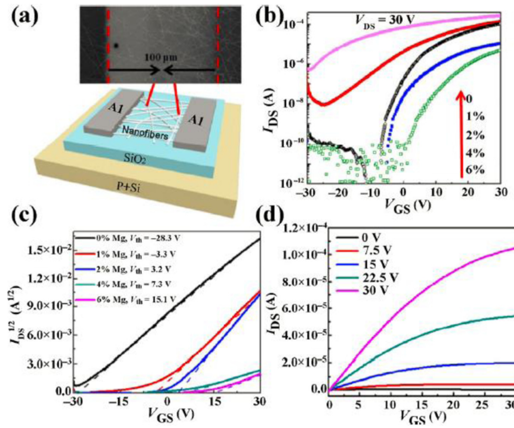

Figure 6.8. (a) (Top) SEM image and (bottom) schematic of a back-gated Mg-doped In_2O_3 NF FETs fabricated with Al electrodes and heavily doped silicon substrates covered with 150 nm thick thermally grown SiO_2. The SEM image illustrates the density of Mg-doped In_2O_3 NFs in the channel and when the density was 0.43 pillars/μm (spinning time of 30 s); the Mg-doped In_2O_3 NF FETs show the best performance. (b) Transfer curves for the backgated FETs with different Mg doping concentrations (0, 1, 2, 4, and 6 mol%). (c) $I_{DS}^{1/2}$ versus V_{GS} curves for the back-gated FET with different Mg doping concentrations (0, 1, 2, 4, and 6 mol%), demonstrating the D-mode FET being successfully transformed into an E-mode one. (d) Output curves of 2 mol% Mg-doped In_2O_3 NF FETs. Reproduced from [29] Tsinghua University Press.

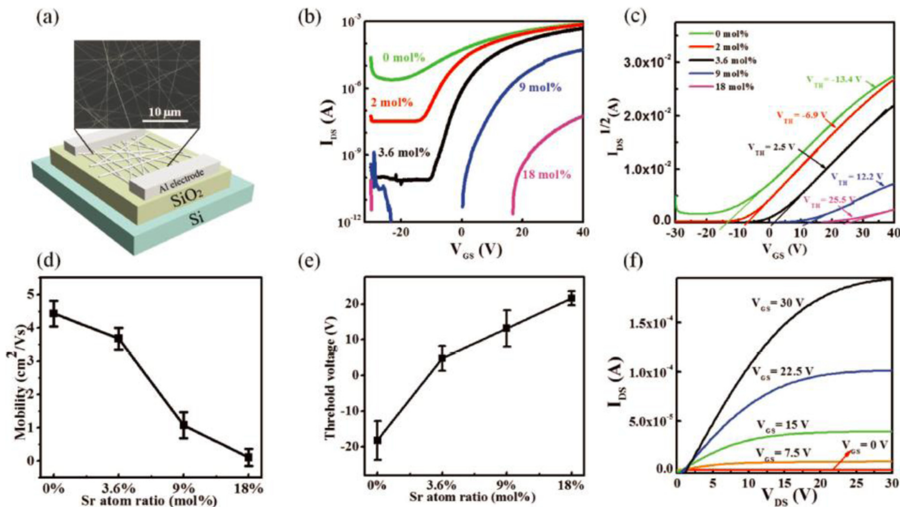

Figure 6.9. (a) Schematic diagram of NF-FET, inset is the SEM image of In_2O_3 NFs. (b) Transfer characteristic of undoped, 2, 3.6, 9, and 18 mol% Sr–In_2O_3 devices, respectively. (c) V_{TH} corresponding to the transfer curves in (b). (d) The corresponding average field effect mobility. (e) The corresponding average V_{TH} of all Sr–In_2O_3 devices. (f) Output characteristic of 3.6 mol% Sr–In_2O_3/SiO_2 device. [30] John Wiley & Sons. © 2019 WILEY-VCH Verlag GmbH & Co., KGaA, Weinheim.

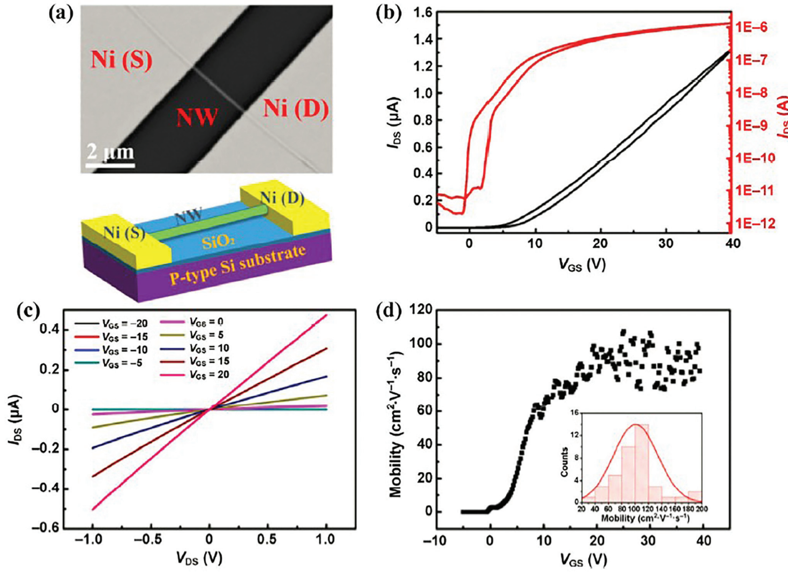

Figure 6.10. Electrical characterization of a typical FET based on a single $In_{1.8}Ga_{1.8}Zn_{2.4}O_7$ NW under vacuum. (a) SEM image and the schematic illustration of the FET device. (b) Transfer characteristics of the device ($V_{DS} = 1$ V). (c) Output characteristics of the device. (d) Field-effect electron mobility assessment for the same device presented in (b) and (c) with $V_{DS} = 1$ V. The inset shows the statistics of field-effect mobility based on 40 devices. Reproduced from [63] Tsinghua University Press.

material issues, specifically due to their amorphous nature [62]. Li *et al* successfully produced high crystal superlattice structure IGZO NWs with different Ga element concentrations by chemical vapor deposition (CVD) [63]. In this study, it was found that when the ratio of In:Ga:Zn:O is 1.8:1.8:2.4:7, the prepared NWs have the best performance when using FETs. The average electron mobility of the device is about 110 cm^2 V^{-1} s^{-1}, and the on/off current ratio is about 10^6. The introduction of the Ga element effectively adjusts the carrier concentration in the fiber. The high binding energy of Ga and oxygen will preferentially form gallium oxide. This reduces the oxygen vacancy in the NFs, thus reducing the carrier concentration and the carrier scattering, and improving the switching current ratio of the device. These results prove that the fabricated devices have good application prospects in the arena of next generation display technologies (figure 6.10) [63].

6.4.4 Other metal oxide NF transistors

The research on one-dimensional n-type metal oxide semiconductor NFs is becoming more and more extensive, but there are few studies on p-type nanostructures. The lack of effective manufacturing methods and relatively low field-effect performance have seriously hindered the further development of complementary logic circuits. In complementary logic circuits, both n-type and p-type semiconductors are necessary [64]. Therefore, there is an urgent need to develop p-type semiconductor NFs. Zhu *et al* prepared CuO NWs semiconductor by electrostatic

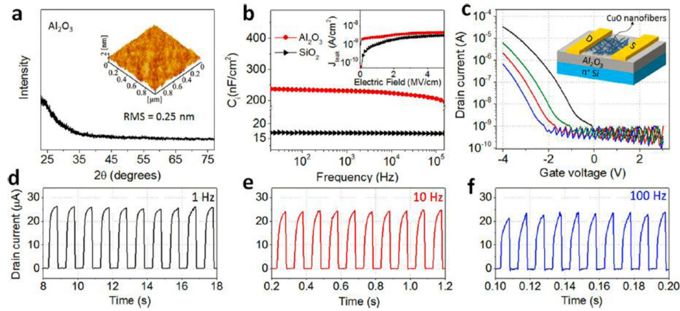

Figure 6.11. (a) The XRD pattern and AFM image of the solution-processed high-κ Al_2O_3 thin film. (b) The J_{leak} versus voltage and C_i versus frequency curves of Al_2O_3 and SiO_2 thin films. (c) The transfer curves of CuO nanofiber network FETs based on the Al_2O_3 dielectric with different V_{DS} values (i.e. 1, 2, 3, and 4 V). I_{DS} responses to a square wave signal applied to the gate voltage with the frequency of (d) 1 Hz, (e) 10 Hz, and (f) 100 Hz. Reprinted from [65], with the permission of AIP Publishing.

spinning and applied them in FET. They exhibited typical p-type properties [65, 66] as figure 6.11 shows.

When using SiO_2 as the gate dielectric, the carrier mobility is 10^{-2} cm^2 V^{-1} s^{-1}, and the current switching ratio is about 10^4. When Al_2O_3 is used instead of SiO_2 as the gate dielectric, the carrier mobility is increased to 3.5 cm^2 V^{-1} s^{-1}. The I_{on}/I_{off} is 3×10^5, and the lower operating voltage is 4 V. Devices based on CuO nanofibers have the advantages of light weight, low pressure, and high performance. They have great application potential in the next-generation chemical/biosensor and electronics (photoelectron) fields.

Matsubara *et al* successfully manufactured highly uniform and continuous NiO NWs by electrospinning [67]. Compared with other methods, electrospinning provides a convenient, scalable, and low-cost way to produce ultra-long NFs with ultra-long aspect ratios exceeding 10^5. Another advantage of electrospinning is that, because the sol–gel-based process can precisely control the doping concentration, it is possible to achieve enhanced conductivity by introducing an appropriate amount of Li^+ into NiO NWs. The assembled FET exhibits typical p-type conductivity, and the doping effect is greatly enhanced by Li doping (figure 6.12) [67].

6.5 Application of one-dimensional metal oxide semiconductor FET

6.5.1 Transparent and flexible electronic devices

The concept of flexible 'transparent electronics' will play a pivotal role in the fields of science, technology and commercial application because they can be used in fast consumer electronics, new energy and transportation [68]. For example, popular car head-up display systems, mobiles and computer display can use 'transparent electronics.' Optically transparent and mechanically flexible electronic circuits will be the center of the next-generation of display technology. Transistors based on polysilicon or amorphous silicon and widely used in current commercial displays, have the problem of low carrier mobility and non-transparent. This limits the further improvement of the refresh frequency and resolution of the display. The metal oxide

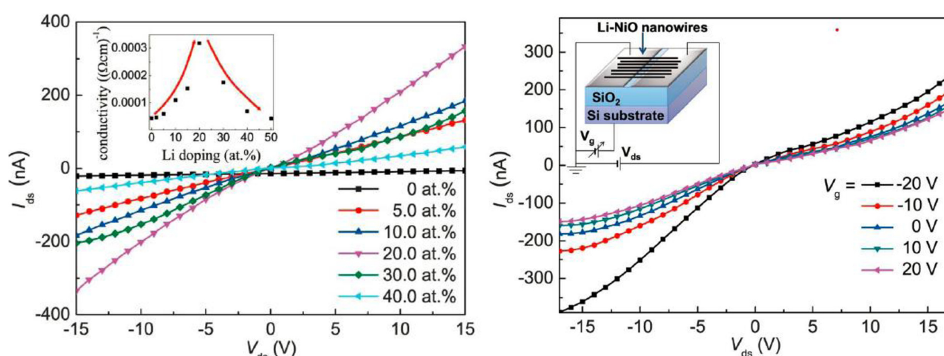

Figure 6.12. (a) Full range XRD of NiO NWs doped with different Li concentrations (0–50.0 at.%). (b) *I–V* curves of NiO nanowires with different Li concentrations. Inset: conductivity as a function of Li at.%. Reproduced from [67] with permission of The Royal Society of Chemistry.

nanomaterials such as ZnO, In_2O_3, and SnO_2 have proper forbidden band widths and high optical transmittance in the visible light range. Compared with the bulk and thin film materials, the 1D metal oxide nanomaterials will have huge application prospects in transparent flexible electronic circuits [15, 20, 68].

The development of optically transparent and mechanically flexible electronic circuits is a key step in the development of skin-like, wearable and display devices. A transparent transistor should have a transparent conductive electrode, dielectric layer, and metal oxide semiconductor layer. In 2007, Ju *et al* using graphic IZO as the gate, ALD deposited alumina dioxide as the dielectric layer, ZnO or In_2O_3 NWs as the semiconductor channel, ITO as the source/drain electrodes, prepared a fully transparent NWe transistor [69]. The optical properties of the device on the glass substrate are excellent, with optical transmittance of 83%. Using forced terephthalate (PET) as substrate, the optical transmittance of the device was 81%. In addition, the device had excellent mechanical flexibility and excellent electrical performance under bending conditions. Figure 6.13 shows a fully transparent and flexible In_2O_3 devices [69]. This research shows great potential of 1D metal oxide nanomaterials in the future development of transparent flexible devices.

6.5.2 Gas sensor devices

Sensing behavior is another important characteristic of metal oxides [56]. One-dimensional metal oxide NWs have a large specific surface area, abundant oxygen vacancies, and surface defects. The NFs can absorb gas from the surrounding environment and undergo a redox reaction, thereby changing the electrical conductivity of the NFs [11, 12, 15–17, 19, 56, 64, 70]. For n-type metal oxides, the reducing gas reacts with the adsorbed oxygen species and releases electrons into the metal oxide, resulting in increased conductivity, while the oxidizing gas uses a reverse process to capture electrons from the metal oxide, thereby reducing conductivity.

Carbon monoxide (CO) plays an important role in the chemical and metallurgical industry, but is toxic to humans [64]. Inhaling an excessive amount of high-concentration carbon monoxide in a short period of time results in carbon monoxide

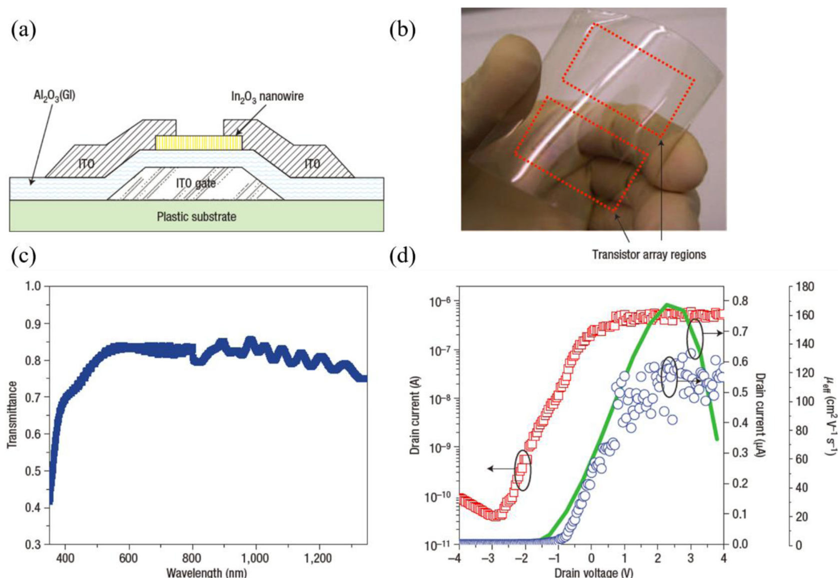

Figure 6.13. Fully transparent and flexible In_2O_3 NW transistors (NWTs). (a) Cross-sectional view of fully transparent and flexible NWT device structure consisting of a plastic substrate, patterned ITO gate electrode (120 nm), ALD-deposited Al_2O_3 gate insulator (50 nm), a single In_2O_3 nanowire (D/L ~20 nm/1.79 mm) for the active channel, and ITO for the source/drain electrodes (120 nm). (b) Image of In_2O_3 NWTs on the plastic substrate, showing the optical clarity and mechanical flexibility. (c) Optical transmission spectrum of region containing In_2O_3 NWTs on the plastic substrate (ITO(S/D)/In_2O_3 nanowires/Al_2O_3/ITO(G)/plastic substrates). (d) The I_{ds}–V_{gs} characteristic of In_2O_3 NWTs at $V_d = 0.5$ V. Blue, red and green data points correspond to linear-scale I_{ds}–V_{gs}, log-scale I_{ds}–V_{gs} and μ_{eff}, respectively. Arrows indicate appropriate axis. [69] (2007) Copyright. With permission of Springer.

poisoning and causes secondary oxygen depletion damage to the brain, heart, liver, kidneys, lungs, and other tissues. The detection of indoor carbon monoxide concentration is extremely important. Singh *et al* prepared Zn-doped In_2O_3 NWs by CVD, using a single NW as a semiconductor layer, and SiN_x as a dielectric layer. The transistors showed excellent electrical performance with on-state current of 8×10^{-6} A, a current switching ratio of about 10^6, and a carrier mobility of 139 cm^2 V^{-1} s^{-1}. Using these transistors to detect CO gas at room temperature, gave results that showed that when compared with pure In_2O_3 NW transistors, Zn-doped In_2O_3 NW transistors have a more sensitive detection effect, and can selectively detect CO gas when in concentration with NO and NO_2 [71]. When exposed to CO gas at a concentration of 5 ppm, a significant threshold voltage shift of −3.5 V can be observed, as shown in figure 6.14 [71].

Ammonia is a colorless gas with irritating properties, mainly used in industrial production. It is very harmful to the human respiratory tract, eyes and skin. The detection of ammonia at room temperature has attracted widespread attention. Huang *et al* prepared polycrystalline $SrGe_4O_9$ nanotubes (NTs) through the electrospinning process [72]. The prepared NTs is a new type of gas sensing material, which can detect NH_3 at room temperature. The maximum sensing response of

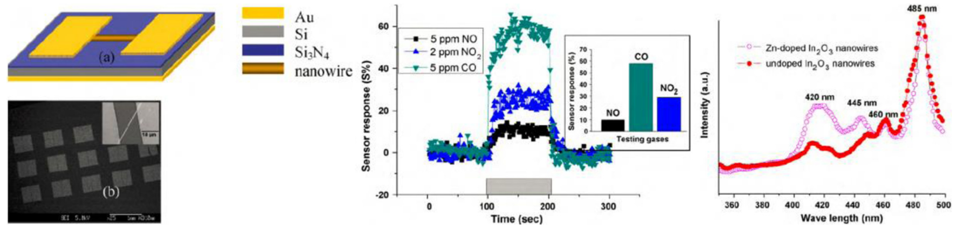

Figure 6.14. (a) Schematic diagram of single NWe FET, with Cr (10 nm)/Au (50 nm) serving as electrodes, SiN_x serving as gate electrode and highly doped (resistivity 0.005 Ω cm) n-type Si as back gate. (b) FESEM image of an array of devices and in the inset a single NW-FET device touching the two electrodes with a channel length of 18 μm. (c) Response of single Zn–In_2O_3 NW sensor to the different gases at a fixed $V_D = 3$ V and $V_G = -15$ V, sensor was operated at room temperature. (d) Photoluminescence spectrum measured from the as deposited Zn-doped and undoped In_2O_3 NWs with an excitation wavelength of 264 nm at room temperature. Reprinted from [71], Copyright (2010), with permission from Elsevier.

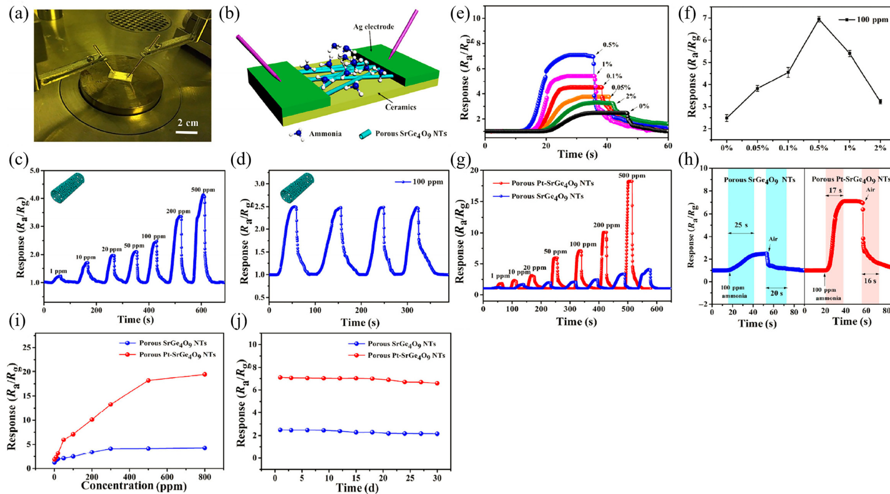

Figure 6.15. (a) Digital photograph, (b) schematic of the $SrGe_4O_9$ NT sensor. (c) Response curves of pure $SrGe_4O_9$ NT sensors to NH_3 gas with different concentrations. (d) Dynamic response of pure SrGe4O9 NT sensors to 100 ppm NH_3 at room temperature. (e) Response curves of the Pt-decorated $SrGe_4O_9$ NT sensors with various Pt concentrations. (f) Error curve of the Pt-decorated $SrGe_4O_9$ NT sensors with various Pt concentrations. (g) Sensitivity with respect to the ammonia concentration, in the range of 1–500 ppm. (h) Dynamic response–recovery curves to 100 ppm ammonia. (i) Gas response to ammonia with various concentrations. (j) Long-term response stability. Reproduced from [72] Tsinghua University Press.

$SrGe_4O_9$ NTs to 100 ppm NH_3 is 2.49. The maximum sensor response obtained is 7.08. Manufactured flexible gas sensors made from these NTs, show excellent flexibility in different bending states, mechanical stability, and sensing stability. Their performance is shown in the figure 6.15 [72]. These properties indicate that the prepared devices have a future in wearable electronic products.

6.5.3 Photodetector

A photodetector can be produced using the photoconductive effect of semiconductor materials. The photoconductivity effect refers to changes in the conductivity of irradiated material when irradiated. Photoconductive detectors are widely used in various fields of the military and national economy. When the irradiated photon energy $h\nu$ is equal to or greater than the forbidden band width E_g of the semiconductor, the photon can excite the electrons in the valence band allowing them to travel to the conduction band, thereby generating conductive electron–hole pairs. This is an intrinsic photoconductive effect. The long wave limit of intrinsic photoconductive materials is limited by the width of the forbidden band. This photoconductive effect is used in FET. When the semiconductor material in the channel is irradiated, the carrier concentration and mobility change, so that the current between the source and drain electrodes changes [18, 20, 73].

Because superlattice NWs have a unique energy band structure for effective photocarrier separation and collection, they have a great potential as active materials for high-performance optoelectronic devices. Li *et al* obtained InGaZnO NFs with superlattice structure and controllable stoichiometry through ambient pressure chemical vapor deposition [74]. Along the nanofiber axis, InGaO $(ZnO)^{4+}$ blocks and InO^{2-} layers are alternately arranged to form a periodic layered structure. When configured as a photodetector, it exhibits surprising performance. When the ratio of In:Ga:Zn:O is 1.8:1.8:2.4:7, a single device has a response of 1.95×10^5 A W^{-1} for ultraviolet light detection, and an external quantum efficiency as high as 9.28×10^7%, The detection time is 0.93 s, and the decay time is 0.2 s. The reason for such excellent performance is due to the incorporation of Ga. The concentration of Ga has a great influence on the device. Ga reduces the oxygen vacancies in the fiber and reduces the carriers in the channel, which reduces the O^{2-} adsorption, thereby improving the photoelectric detection performance of the device. The optical transmittance of the material is high, so a completely transparent ultraviolet light detector can be produced (figure 6.16) [74].

One-dimensional nanostructured SnO_2 has been widely studied due to its large specific surface area, high optical permeability, and n-type semiconductor properties. Based on this, Liu *et al* used a low-cost electrospinning method to prepare SnO_2 NFs and NT arrays [18]. Using this as a channel material, an FET was prepared. By simply adjusting the content of Sn in the precursor solution, the electrical and optoelectronic properties of the fabricated device were easily adjusted. When 5 ml of precursor solution contains 0.2 g $SnCl_{2\cdot4}H_2O$, the prepared device shows the best performance, high saturation current and large current switching ratio. It also could detect deep ultraviolet light (wavelength 240–320 nm), including an ultra-high photocurrent of 307 μA, a high photosensitivity of 2003, respond ability of 214 A W^{-1} and detectivity of 2.19×10^{13} Jones. When fluorine-doped tin oxide (FTO) glass was used as the base material, it showed high optical transmittance and photosensitivity (figure 6.17) [18]. These results indicate that the one-dimensional SnO_2 prepared by electrospinning has application prospects in the next generation of functional electronic devices and optoelectronic devices.

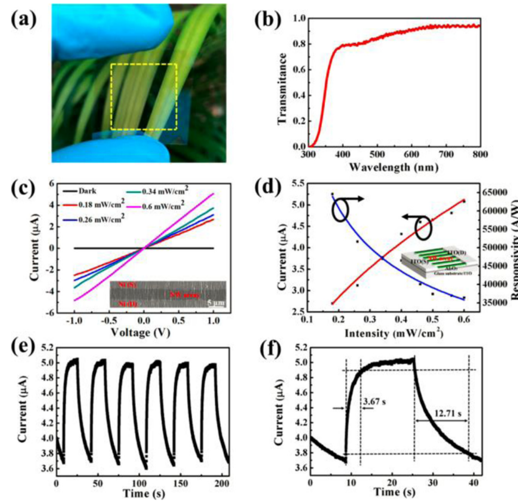

Figure 6.16. Transparent photodetector device based on $In_{1.8}Ga_{1.8}Zn_{2.4}O_7$ NW parallel arrays. (a) Optical image of the leaves covered by the as-fabricated device, while the device area is highlighted by the yellow dashed rectangle. (b) Transmittance measurement of the device. (c) $I-V$ curves of the device under different power intensities of 261 nm light illumination and in the dark. The inset shows the top-view SEM image of the NW parallel arrayed device channel. (d) Dependence of the photocurrent and the responsivity on the light intensity. The inset gives the device schematic of the photodetector fabricated on glass substrates. (e) Photoresponse characteristics (current versus time) of the device. The light intensity is 0.6 mW cm^{-2}. (f) Corresponding high-resolution current versus time curve. The bias is 1 V and $V_G = -20$ V. Reprinted with permission from [74]. Copyright (2019) American Chemical Society.

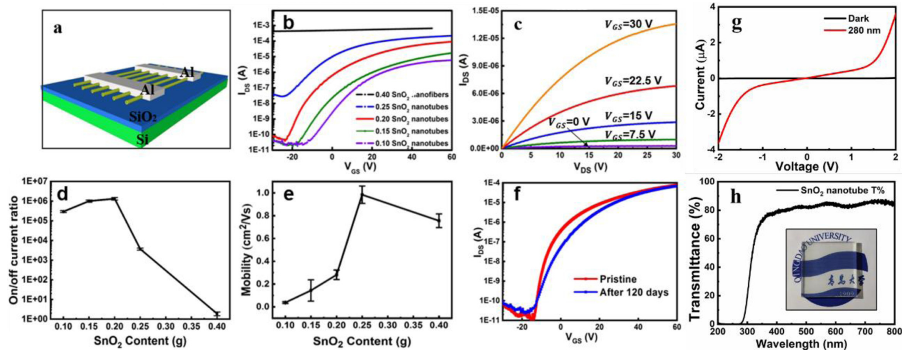

Figure 6.17. (a) FET structure of SnO_2 NTs array. (b) The output curve of the SnO_2 NTs FET. (c) Transfer curves of SnO_2 FETs with different Sn amount. (d) Average on/off current ratio of SnO_2 FETs of different Sn contents. (e) Average mobility of SnO_2 FETs with different Sn contents. (f) The stability of 0.2 SnO_2 NTs FET after 120 days. (g) The $I–V$ curve of 0.2 SnO_2 nanotubes photodetector using FTO glass as substrate. (h) The optical transmittance curve of the FTO glass after being covered by 0.2 SnO_2 nanotubes. Reproduced from [18]. © IOP Publishing Ltd. All rights reserved.

6.5.4 Synapse-like devices

As a representative of the development of human science and technology, computers play an irreplaceable role in people's daily lives. With the rapid increase in the amount of information in human society, while the speed of computer calculations has increased, energy consumption has also increased rapidly. The human brain is essentially a very efficient and energy-saving information processing system. Adult brains have only about 20 W of power. This huge difference in energy consumption is mainly due to differences in the structure and information processing methods of computers and human brains. The human brain consists of a network of neurons formed by the cross-connection of approximately 10^{11} neurons. The connections between neurons are called synapses, and there are about 10^{15} synapses in the human brain. By changing the connection strength between neurons (called synaptic weights) to store and process information, the brain has a self-learning function to achieve the integration of storage and processing. In view of the characteristics of neural networks, in order to improve the information processing efficiency of computers, researchers have long begun to use traditional silicon-based CMOS processing devices to simulate neuron information processing methods. However, on the one hand, since the traditional silicon-based semiconductor devices are mostly volatile or binary nonvolatile memory devices, this is inconsistent with the simulated characteristics of neural synapses. On the other hand, with the development of CMOS technology for decades, the size of the device channel has entered more than a dozen nanometers, or even a few nanometers, not only facing extremely high manufacturing difficulties, but also getting closer to physical limits (such as thermal effects, quantum tunneling effect). Therefore, when building large-scale neural networks, CMOS devices face huge challenges in terms of high-density integration and energy consumption reduction. In order to overcome the difficulties faced by CMOS devices, it has become an important goal of scientific research and industry to find new materials and devices that meet the characteristics of neuromorphic computing [75–77].

Gou *et al* manufactured a synaptic transistor with a multi-face gate structure by using a single SnO_2 NW as a channel layer [78]. The in-plane-gate electrode is regarded as the presynaptic terminal and the SnO_2 nanowire channel with a Vds biased is used as the postsynaptic terminal. Due to the proton-related electric-double-layer (EDL) coupling of synaptic devices, it not only successfully mimics important synaptic functions including excitatory postsynaptic current (EPSC), paired-pulse facilitation (PPF), dynamic logic, adaptive and synaptic filtering. Moreover, the synaptic behavior can be adjusted in the dynamic range through multi-terminal adjustment of synaptic input. In addition, a SnO_2 NW synaptic transistor is irradiated with a light source as a light modulation terminal, and the observed neuromorphic function is dynamically modulated by optical density. Figure 6.18 shows a schematic diagram of a synaptic transistor and the electrical signals of the transistor when simulating the behavior of a synapse [78]. These excellent nanoscale synaptic transistors have broad application prospects in synaptic electronics.

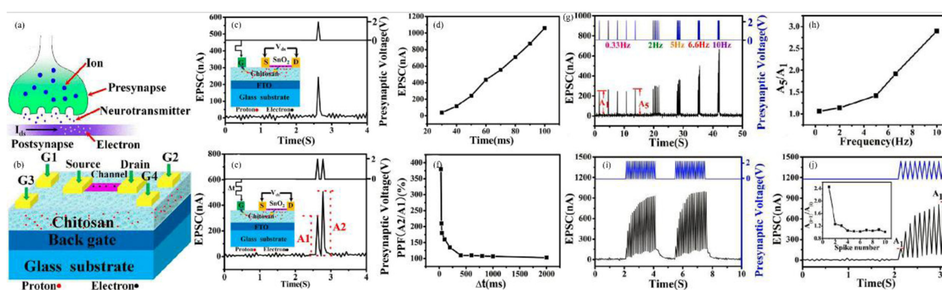

Figure 6.18. (a) Schematic image of a biological synapse simulated by synaptic transistors. (b) The schematic diagram of SnO_2 NW-based neuron transistor gated by the chitosan film on FTO glass substrate. (c) EPSC triggered by an in-plane presynaptic spike (2.0 V, 50 ms). (d) Spike duration-dependent EPSC, the amplitude of the spike is 2.0 V. (e) The EPSCs triggered by a pair of presynaptic spike with a time interval (Δt) = 100 ms. (f) PPF index (100% × A2/A1) plotted as a function of spike Δt. (g) EPSCs recorded in response to the stimulus train with different frequencies. (h) EPSC amplitude ratio (A_5/A_1) plotted as a function of presynaptic spike frequency. (i) A train of spikes (2.0 V, 50 ms, $\Delta t = 50$ ms) is applied on the in-plane-gate and EPSC is measured as a function of time. (j) The amplified sections of a 2.0–3.2 s range corresponding to adaptation training from 4 (i). Inset: the rate of A_{i+1}/A_i (A_{i+1} and A_i are the amplitudes of the previous and latter EPSC amplitude, respectively). Reproduced from [78] with permission of The Royal Society of Chemistry.

6.6 Summary and outlook

In summary, one-dimensional metal oxides have excellent optical, electrical and gas detection performance, and are the basis for building multi-functional and high-performance field-effect transistors. Through continuous adjustment and optimization of transistor performance, the application of transistors will be widely used in electronic display technology, sensing equipment, electronic memory, and logic circuits.

At present, there are still some problems in the preparation of one-dimensional metal oxide semiconductors. For example, the cost of preparing nanofibers using CVD molecular beam epitaxy, or other methods is relatively high, the equipment size is large, and it is difficult to prepare and grow on a large scale. The orientation of the fiber is inconsistent, and the fibers needs to be transferred to the substrate and then subjected to a photolithography process. The utilization rate of the raw material is also low. When using the electrospinning method to prepare nanofibers, high temperature annealing is required to remove the presence of the fiber polymer. If the required temperature is higher, normal transparent flexible substrates will deform or even decompose.

With the continuous development of science and technology, the focus of future research will be on transparent flexible electronic devices. The future research directions of FETs are as follows:

1. Discovering a method that can lower the annealing temperature, so that not only can transparent preparation be achieved, but also flexible electronic devices can be produced by large-scale printed electronic circuitry;
2. Designing a geometry of metal oxide nanofibers to realize storage or logic circuits, so the integration into electronic circuits increases;

3. Studying the growth mechanism of NWs, with the goal of controlling the surface morphology, and the concentration of defects, to obtain higher performance optical detectors, gas sensors and other electronic devices;
4. Develop p-type metal oxides with excellent performance. CMOS circuits based on n-type and p-type one-dimensional metal oxide semiconductors have broad prospects.

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