High Speed Bipolar ICs Using Super Self-Aligned Process Technology

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High Speed Bipolar ICs Using Super Self-Aligned Process Technology

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We have developed a new bipolar process technology, called SST. The emitter region, base p region, base p^+ region, base p^+ polysilicon electrode and emitter contact window of NPN transistor are formed by one mask photolithography process. The transistor active regions are all self-aligned. Therefore, small-size transistors can be realized and high performance is achieved by the decreased collector-base junction capacitance. A new bipolar integrated circuit using SST gave a 63 ps/gate propagation delay time and 0.043 pJ/gate speed-power product.

§1. Introduction

At present, silicon semiconductor technology is advancing rapidly and is being used in computers, communications, consumer applications and other electronics area. For these systems, high-speed bipolar logic integrated circuits with small power dissipation are urgently required. Realization of such high-speed bipolar logic integrated circuits largely depends upon the development of circuit design, device structure and process technology. Several authors have already reported high-speed logic integrated circuits with new device structure and process technology, which have minimum propagation delay time of 85 ps/gate and speed-power product of 0.19 pJ/gate.[1-3]

This paper reports development of a new bipolar integrated circuit structure which gives a 63 ps/gate propagation delay time and 0.043 pJ/gate speed-power product.

The new bipolar integrated circuit structure is fabricated by a new process technology, called Super Self-aligned process Technology (SST). The main feature of the SST is that active regions of the transistor are formed by one mask photolithography process. The transistor active regions are all self-aligned.

This paper describes the SST structure, fabrication process and experimental results.

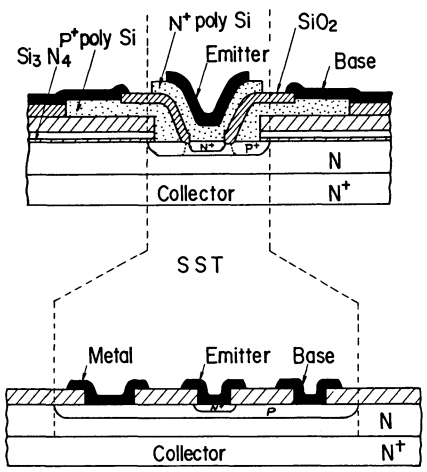
§2. SST Structure and Characteristic

Bipolar transistor structure using SST is shown in Fig. 1 with comparison to that of conventional planar transistor.

The submicron width base p^+ polysilicon electrode contacts the base p^+ region around the emitter diffusion region.

The base p^+ polysilicon electrode is electrically isolated from the n^+ polysilicon emitter electrode by the SiO_2. The spacing between the emitter diffused layer and the base contact is extremely small, less than 0.5 μm. The metal base electrode contacts the base p^+ polysilicon electrode on the field SiO_2 film. SST characteristics are as follow.

1) The emitter n^+ region, the base p region, the p^+ base region, the base p^+ polysilicon electrode and the spacing between the emitter n^+ region and base contact are formed by one



conventional

Fig. 1. Bipolar transistor structure using SST together with that of conventional planar transistor.

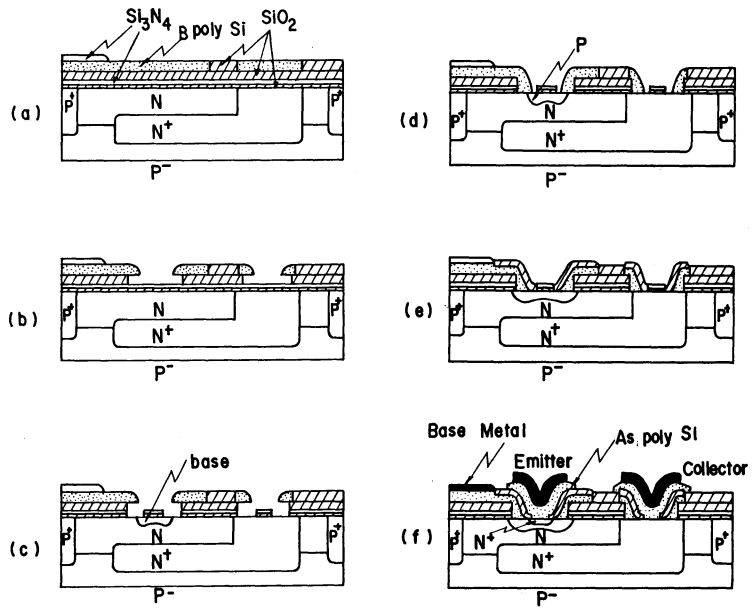


Fig. 2. SST fabrication steps for integrated transistor.

mask process. The processes for forming the transistor active region are all self-aligned.

2) Therefore, small-size transistors can be realized and high performance is achieved by the decreased collector-base junction capacitance as well as collector to substrate capacitance, because the base area in the SST is about 1/6–1/3 the area of a conventional transistor with the same emitter area size.

3) High performance is achieved by the decreased base resistance, because the spacing between the emitter region and the base contact region is less than about 0.5 μm.

§3. SST Fabrication Processes

3.1 *Main process sequence*

SST fabrication steps are shown in Fig. 2. They are also the same as the conventional bipolar IC process until the p^+ isolation layer is formed. Subsequent steps are as follow.

1) Multilayers of SiO_2, Si_3N_4, CVD SiO_2, the boron doped polysilicon and Si_3N_4 are consecutively formed. The boron doped polysilicon layer was deposited by SiH_4 and BCl_3 in H_2 and N_2 in a lampheated horizontal reactor. Typical deposition condition is shown in Table I. Unnecessary polysilicon layer is oxidized selectively. Then, Si_3N_4 is partially preserved at the areas corresponding to the base contact window and resistor window.

Table I. Typical deposition condition of boron doped polysilicon.

Temperature (°C)	640	
SiH_4 (cc/min)	100	
H_2 (cc/min)	1900	
Carrier gas N_2 (l/min)	60	
BCl_3 (2050 ppm) (cc/min)	260 5	$(4\times10^{20}/cm^3)$ $(1\times10^{19}/cm^3)$
Deposition rate (Å/sec)	9 5	$(4\times10^{20}/cm^3)$ $(1\times10^{19}/cm^3)$

2) The windows for the emitter and the collector are opened by using plasma etching. Plasma etching rate of the boron doped polysilicon $(4\times10^{20}/cm^3)$ was about 840 Å/min. Then, CVD SiO_2 is side etched.

3) The shadowed Si_3N_4 film by the overhanging edge of the boron doped polysilicon layer is removed selectively. The base area is formed by B^+ ion implantation.

4) The boron doped polysilicon layer is deposited again and removed by ion milling.

5) The 0.5 μm thick thermal oxidized film is formed.

6) Arsenic is diffused through As doped polysilicon emitter electrode. The depth of the emitter-base junction is about 0.08 μm. Then, metal (Al-Si 2%) is evaporated and unnecessary

layer portions are etched away. These are the main fabrication steps of SST.

In the next sections, details of some typical processes are described.

3.2 *The process of opening the emitter and base window*

Boron doped polysilicon layer is plasma etched by using a photoresist as an etching mask. Then, the CVD SiO_2 film is 50% over-etched. Side etching is about 0.7–0.8 μm. In order to open extrinsic base windows without any photolithographic process, Al (2000 Å) is evaporated from a vertical direction to the entire surface. At this time, the overhanging edge of the boron doped polysilicon prevents Al deposition on the Si_3N_4 shadowed. Then, Si_3N_4 is plasma etched. Al is removed by the etching solution of H_2SO_4: H_2O_2=4: 1. The extrinsic base window is opened in the shadow simply by etching SiO_2 (500 Å).

3.3 *The process of forming the base area*

Born is implanted into both the extrinsic base region through SiO_2 (500 Å) and the intrinsic base region through SiO_2 (500 Å) and Si_3N_4 (1200 Å) at the same time.

The reason why base ion implantation is carried out at this step is that region I shown in Fig. 3 prevents separating from the intrinsic base region (region III as shown Fig. 3). Boron of 1.95×10^{13} atms/cm^2 was implanted into the base region at 55 keV. Boron concentration, calculated by the LSS theory and by that including thermal diffusion, is shown in Fig. 4.

The annealing condition is 700 minutes at 800°C and 130 minutes at 900°C. Boron diffusion coefficient[4] used in this calculation is 3.6×10^{-17} cm^2/sec at 800°C and 8.6×10^{-16} cm^2/sec at 900°C. The depth of the base-collector junction is estimated to about 0.15–0.2 μm.

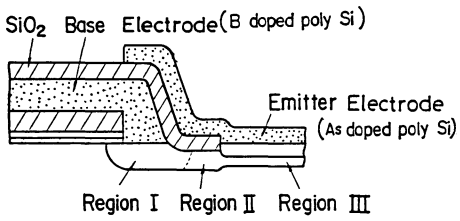


Fig. 3. A cross-sectional view of a transistor at emitter diffusion.

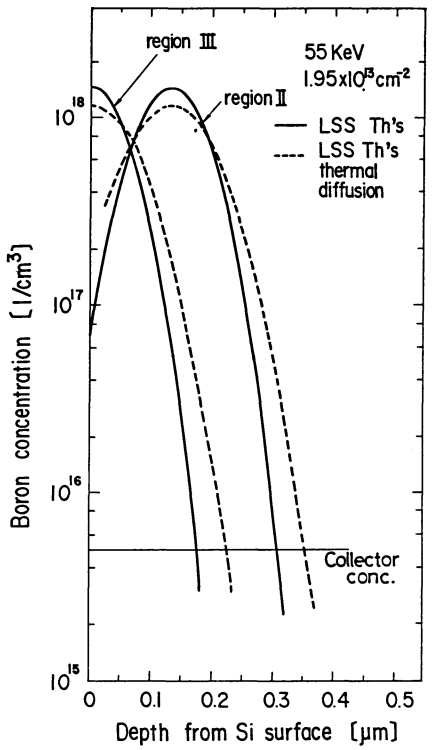


Fig. 4. Boron concentration profile.

3.4 *The process of forming the base p^+ polysilicon layer*

In order to preserve the shadowed portion by the boron doped polysilicon layer, 0.6 μm thick doped polysilicon containing 1×10^{19} atms/cm^3 borons is deposited. Boron is less than 1×10^{19} atms/cm^3 in this polysilicon, because it prevents the junction depth of p^+ extrinsic base region from being deep. To remove this layer, except the shadowed portion, ion milling technique is used on account of its ability of vertical etching which is necessary in this case. The 1×10^{19} atms/cm^3 boron doped polysilicon etching rate for ion milling is about 300 Å/min. The ion milling is done with Ar gas at 1.5×10^{-4} Torr, 800 V acceleration voltage and 0.36 mA/cm^2 ion current density.

Note that the vertical etching results in the preservation of the doped polysilicon at the shadowed portion but not at the portion exposed initially. The base p^+ polysilicon electrode is thus formed as shown in Fig. 5.

3.5 *Boron doped polysilicon oxidation*

The process of oxidizing the boron doped

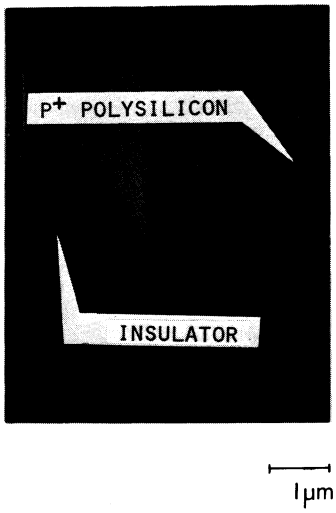


Fig. 5. Photomicrograph of a cross-sectional view after the ion milling process.

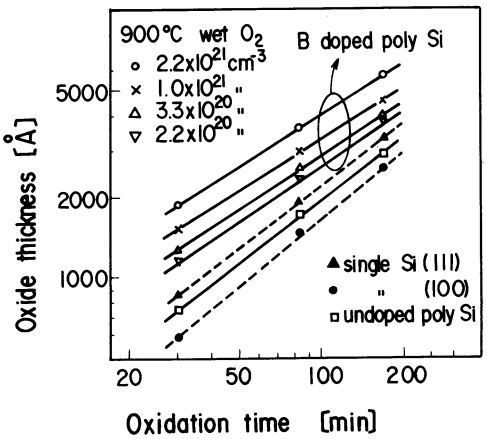


Fig. 6. Oxide thickness vs oxidation time at 900°C.

polysilicon layer is necessary in order to isolate the emitter from the base. Plots of oxide thickness vs. oxidation time at 900°C are shown in Fig. 6. They show that oxidation rate becomes higher as boron concentration becomes higher. The oxide thickness formed in order to isolate the emitter from the base is about 5000 Å. After the boron doped polysilicon oxidized, the As doped polysilicon of 1×10^{21} atms/cm^3 is deposited. A cross-sectional view of the fabricated SST transistor is shown in Fig. 7.

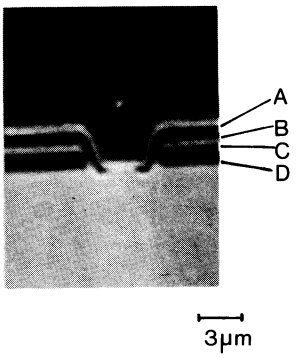


Fig. 7. A cross sectional view of SST transistor after 30° angle lapping, A: As doped polysilicon, B: SiO_2, C: Boron doped polysilicon, D: Insulator.

§4. Device Characteristics

To evaluate switching characteristics of the SST transistors 51-stage ring oscillators with nonthreshold logic[5] (NTL) have been fabricated in case of 3 kinds of operation current. A part of the experimental ring oscillators is shown in Fig. 8. Following dimentions for the SST transistors used in the ring oscillator are designed.

Emitter area: 2×3 μm^2
Base area: 4×5 μm^2
Isolation area: 459 μm^2

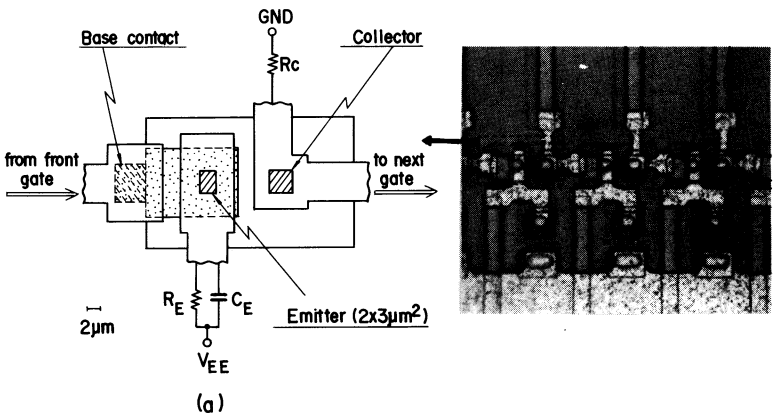


Fig. 8. A part of the experimental NTL 51 stage ring oscillator.

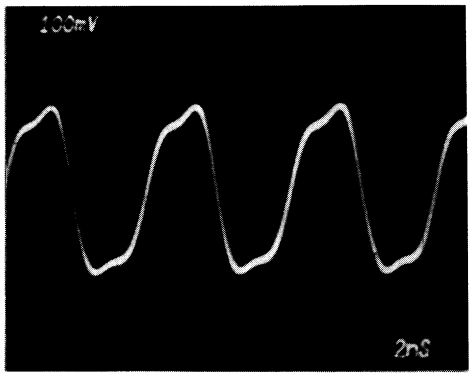


Fig. 9. Oscillation waveforms for high speed ring oscillator.

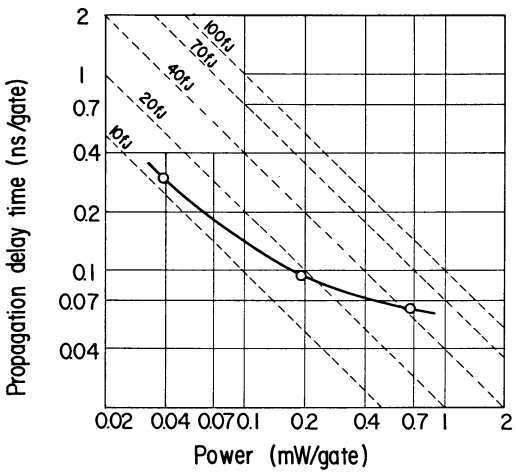


Fig. 10. Power delay curves of the NTL ring oscillators using SST.

The oscillation waveform of the oscillator designed for high speed is shown in Fig. 9. The observed logic amplitude is about 400 mV and the period is 6.3 ns at $I_c=0.68$ mA. Figure 10 shows the power-delay curve obtained from the experimental results of the above ring oscillators. Dissipation powers are calculated by $V_{EE}=-2$ V.

For the high speed gate, 63 ps/gate propagation delay time was achieved at $I_c=0.68$ mA. This is the fastest value which has been realized in all Si devices so far. For the gate designed for low power, the propagation delay time was about 300 ps/gate at $I_c=39$ μA. Then, power-delay product was only 12 fJ/gate. In the case of $I_c=0.19$ mA/gate, propagation delay time and power-delay product were 94 ps/gate and 19 fJ/gate, respectively.

The main reasons for these remarkable results obtained are as follow.

1) The extremely small base-collector junction capacitance, based on SST structure ($C_{TC}=$ 9 fF).

2) High cut off frequency, based on shallow emitter-base and base-collector junctions ($f_T=7$ GHz at $V_{CE}=1$ V).

3) The remarkable decrease in isolation capacitance, based on the fine size transistor using SST ($C_{TS}=82$ fF).

4) Relatively small extrinsic base resistance, compared with planar transistor (280 Ω).

This SST ring oscillator is isolated by using a p-n junction. Much higher performance in speed and power dissipation will be achieved by utilizing local oxidation isolation technology.

§5. Summary

A bipolar integrated circuit technology with high performance and low power has been achieved. The small size bipolar transistor active region has been realized by one mask process using SST.

The unique structure using SST has resulted in the realization of small size transistor and high speed, low power integrated circuits.

The devices provide the following excellent characteristics.

1) Propagation delay time is as small as 63 ps/gate with NTL circuits.

2) Power dissipation is as low as 0.68 mW/gate.

3) Power-delay product is as small as 43 fJ/gate.

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