(Invited) Static Induction Transistor Logic

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(Invited) Static Induction Transistor Logic

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Static induction transistor (SIT) seems to correspond to field effect transistor (FET) and bipolar transistor (BPT) in backward biased and forward biased mode, respectively. In each mode, characteristics are much superior both theoretically and experimentally. Integrating SIT into IIL structure, operation with very low power, very low energy and fast speed is shown even when very primitive and easy processing has applied, as the first stage. Future of this kind of integrated circuit, including memory circuit, which shows very high packing density, very high speed and very low energy operation, is discussed.

§1. Introduction

Static induction transistor (SIT) is a new transistor which shows nearly exponential I-V characteristic in lower current region and the main mechanism of operation is the control of the potential or its distribution for the source at the injection control point (intrinsic gate point) surrounded by gate electrode through static induction effect from gate voltage and from drain voltage,[1] therefore, there is no effect caused from base resistance. It makes possible to increase the resistivity of the channel materials.

In the forward biased mode,[2] SIT is in somewhat similar operation to the punching through situation of the bipolar transistor, except the intrinsic gate potential is controlled through the static induction. Therefore, the cut-off frequency is ultimately high and the storage effect is eventually small because of the no neutral or storage region in co-operation with relatively low carrier concentration of the intrinsic gate material as shown in Figs. 1 and 2.[3–5] In this region, I-V characteristic shows a slightly saturating tendency as shown in Fig. 3(a) and (b)[4,5] limited from the effective base width in the intrinsic gate point approaching the thermal emission equation beyond the potential barrier qV_G^* at the intrinsic gate; $[qn_s(kT)^{1/2}/(2\pi m^*)^{1/2} \exp\{-qV_G^*/(kT)\}]$, where n_s is the density of carrier in source region.

Forward mode seems mostly important when it is applied as normally-off mode of operation especially as switches.[2] When the sum of the diffusion potential between channel and gate; V_{dG}, and the applied voltage is not enough to pinch-off the channel, ohmic current flows following the classical theory by Shockley;[6] however, because of the small negative feedback resistance, there occur no current saturating phenomena. Recently Mitsui *et al.*[7] reported about the realization of GaAs SIT, which suggests us that, even in the case of GaAs, current saturation is caused from negative feedback effect through series resistance from source to pinch-off point; r_s, not from carrier velocity saturation.

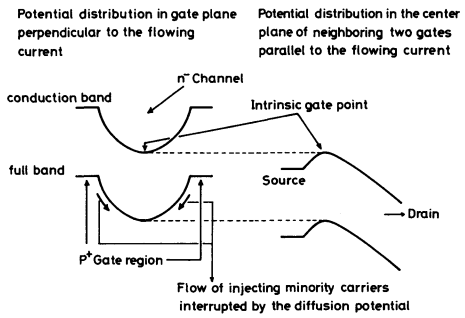


Fig. 1. Schematic diagram showing potential distribution: intrinsic gate point, which controls the injecting current from source toward drain, corresponds to a saddle point and the flowing electron current from gate p^+ region into channel is interrupted by the gate diffusion potential with channel V_{dG} and this makes storage capacitance small even in forward biased condition.

In normal operation of SIT, gate is biased in backward and usually it gives exponential I-V characteristics.[1] In this mode, first deviation from exponential character occurred by the negative feedback effect induced from series resistance between source and intrinsic gate point;[8] r_s, contradicting to the analog transistor[6] or to the gridistor[4,10] which follow the space charge conduction laws.[11–13]

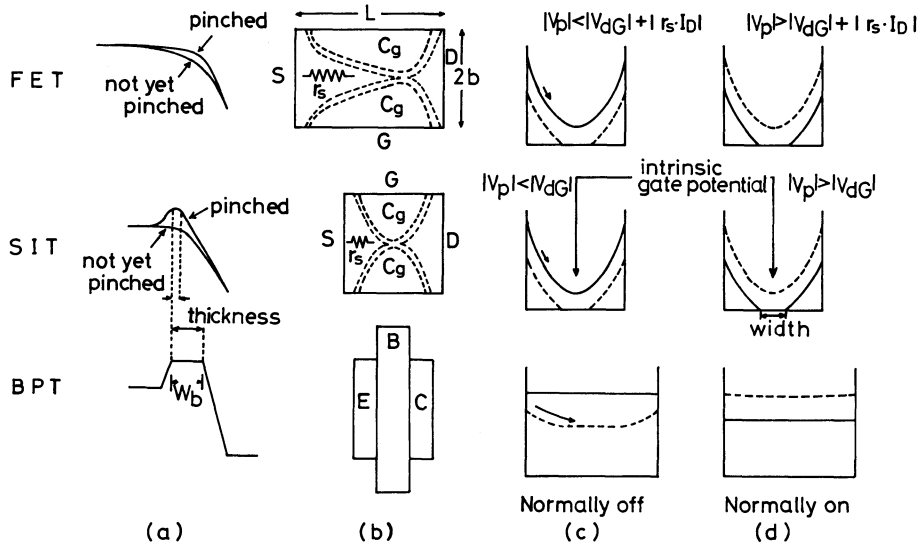


Fig. 2. Schematic diagram showing potential distribution: (a) in the center plane of neighboring two gates or of base layer parallel to the flowing current. Pinched SIT gives a similar distribution with BPT, however, extremely thin effective base thickness. Similar pinched off condition for FET with only gate voltage, not by the negative feedback action through channel resistance; r_s, corresponds to current cutoff, (b) schematic diagram of the structure and the distributions of the depletion layer, and potential distribution in the gate or base plane perpendicular to the flowing current, (c) in normally-off mode and (d) in normally-on mode; solid line gives the unbiased condition, dotted line gives the biased condition and small arrows give the carrier injection from gate or base electrode; V_p is the pinch-off voltage.

Effect of the negative feedback which becomes unnegligible in higher current condition inverts the temperature coefficient into negative, which increases the area of safety operation, and finally I-V characteristic becomes to be saturating.[8] Anyhow, smaller series resistance distributing along the channel compared to usual field effect transistor (FET) generates smaller noise and the observation of the shot noise is becoming possible.[14]

Smaller series resistance; r_s, and the smaller gate capacitance; C_g, which is caused from the diffusion limited minimum size compared with that in FET, which has longer gate along the channel as shown in Fig. 2(b), give rise to the cut-off frequency; f_c as is given by $f_c \simeq (\pi \cdot r_s \cdot C_g)^{-1}$.

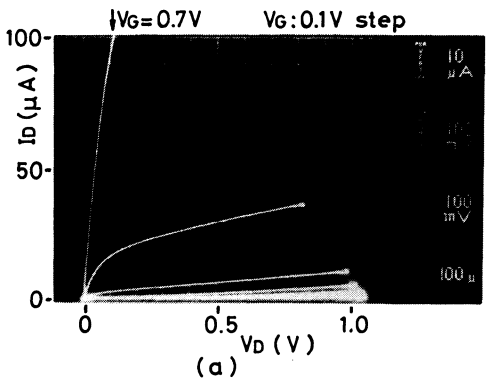
Moreover, the serially connected negative feedback resistance r_s in FET as shown in Fig. 4(b), decreases the gain and increases the response time as an active device, and also it makes difficult to settle the bias condition because the voltage drop in series resistance increases the bias voltage. Then it can be said that the SIT is most promising as a high speed device[13] compared with BPT and FET. This means that, even as normally-off high speed switching device, SIT is reasonably estimated to show much faster operation in lower energy supply compared to that realized by FET.[15–19]

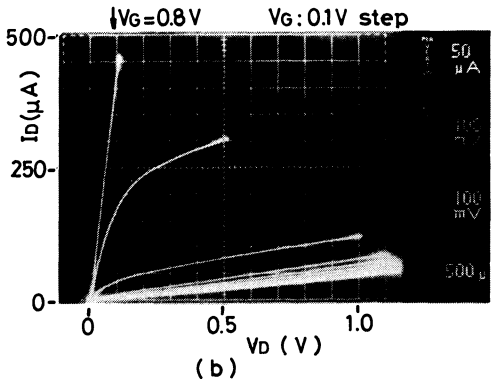
§2. Integration of SIT as a Logic Circuit (SITL)

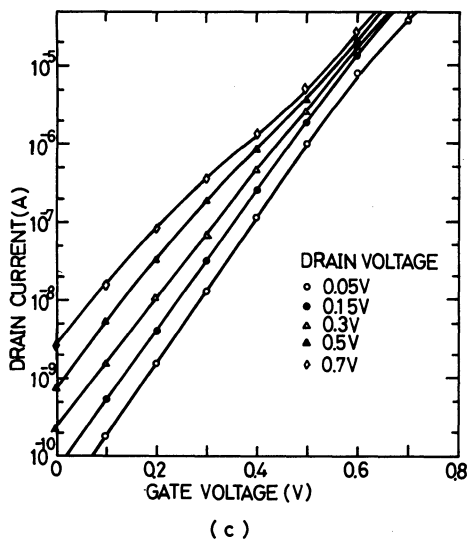
As has been clearly understood, integration of SIT into logic circuit can expect to realize the higher speed, higher gain and lower power operation compared with BPT and FET.

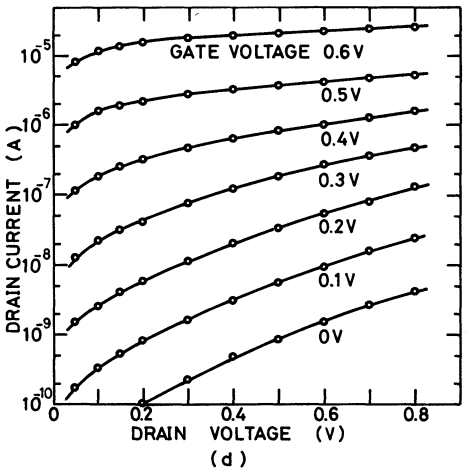
Another merit expected is the possibility of many configurations. In SIT, channel is surrounded by the backward biased gate, because gate has not a little diffusion potential. This makes easy to keep the transport factor β close to 1 in every configurations, vertical, inverted and even lateral as shown in Figs. 5 and 10.

In the case of logic circuit, normally-off mode seems more suitable to make the polarities of input and of output applied voltage in the same direction and to reduce the power for









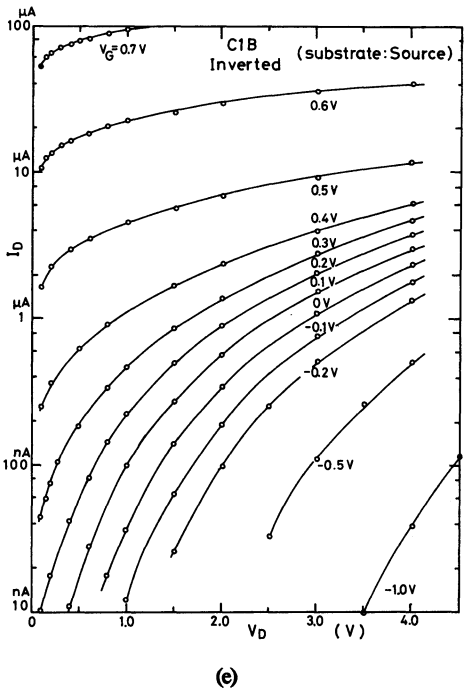


Fig. 3. Examples of the V–I characteristic of normally-off forward biased mode in (a) low energy and low speed device; vertical scale; 10 μA/unit, horizontal scale 100 mV/unit, and bias steps are 100 mV, and (b) high speed and higher energy device, vertical scale 50 μA/unit, horizontal scale 100 mV/unit, and bias step 100 mV, and dc characteristics as function of (c) gate voltage and (d) and (e) drain voltage which easily shows very high cut-off frequency as high as GHz range as shown in Fig. 9.

operation. A time delay for operation is mainly dependent on the charging time for the input capacitance; C_{in}, till a certain swing voltage; V_{sw}, then the total charging is $C_{in} \cdot V_{sw}$. When I^2L with two drains is prepared, $C_{in} \doteqdot C_{SG} + 2C_{GD}(k+1)$, where k is a voltage amplification factor as an amplifier, which can be approximated as about 1, then $C_{in} \doteqdot C_{SG} + 4C_{GD}$. The charging time is $C_{in} \cdot V_{sw}/I_i$, and the supplied power is the product of a supplied voltage; V_{su}, and supplied current I_{su}. Then the figure

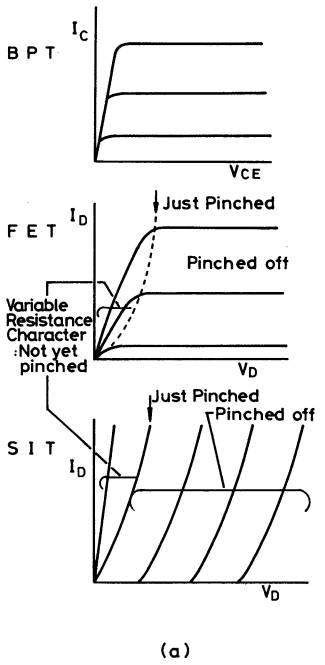


Fig. 4. (a) Schematic V–I characteristics in BPT, FET and SIT; Normal pinching in FET occurred by negative feedback through r_s and in SIT by gate voltage. Pinching off by gate voltage in FET, not by negative feedback action, gives drain current cut-off, unable to be drawn in the figure. (b) Symbol marks for BPT, SIT and for FET, which can be said as negative feedback SIT or extrinsic SIT and the negative feedback gives the energy loss and time delay. SIT can be said as intrinsic FET.

of merit as a logic circuit represented by a product of supplied power; P_{su}, and time delay for operation; τ_d, can be represented as[2]

$$\tau_d \cdot P_{su} \simeq I_{su} \cdot V_{su} \frac{C_{in} \cdot V_{sw}}{I_i} = \frac{V_{su} \cdot C_{in} \cdot V_{sw}}{\beta}.$$

If the capacitance is assumed to be mainly composed of the depletion layer capacitance,

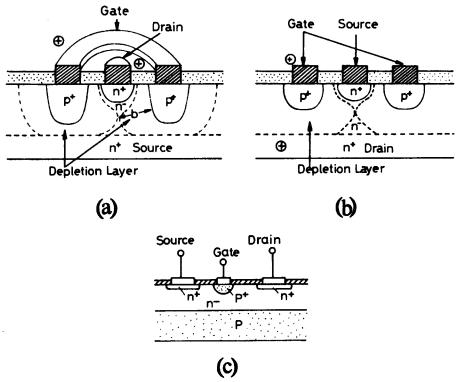


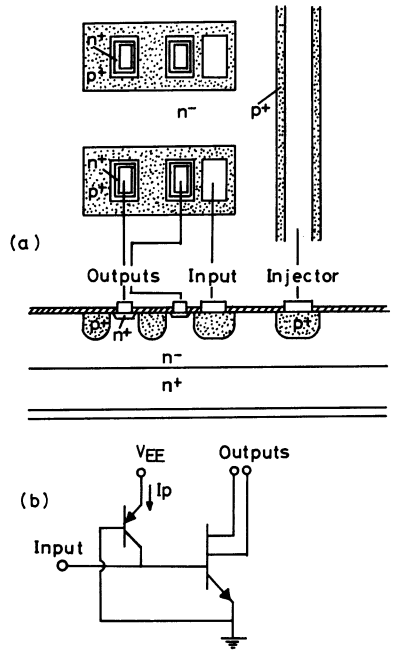
Fig. 5. Configuration of SIT in (a) normal vertical, (b) inverted vertical and (c) lateral structure. Channel is surrounded by backward biased gate depletion layer with diffusion potential as shown (a) in normal vertical, and (b) in inverted vertical, and the inverted vertical configuration has the same polarity for voltages applied for two electrodes on the surface. Fig. 9 shows the large transport factor and gives high frequency cut-off in both direction; normal and inverted.

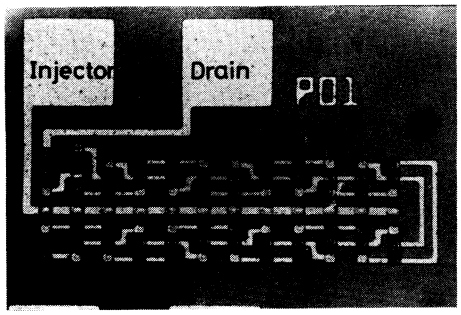
C_{in} is easily as small as one tenth of that in the case of usual I^2L–the $P_{su} \cdot \tau_d$ product can be 10 fJ. But the capacitance is at least composed of storage capacitance, too, not only of depletion layer capacitance. Therefore, the $P_{su} \cdot \tau_d$ product in IIL composed by SIT is expected to be much less than 10 fJ even based on the experimental value of IIL by BPT.[20,21]

Simplicity of the processing is the most important factor for integration; then, as the first project, planar structure is prepared.[4,5] Figure 6 shows the structure of IIL prepared by a *p*-type diffusion and an *n*-type diffusion, followed by the hole making process through oxide film for the metal contact and metal film shaping as wiring. This process needs only 4 masks to finish the ring oscillating circuit to measure $P_{su} \cdot \tau_d$ product.

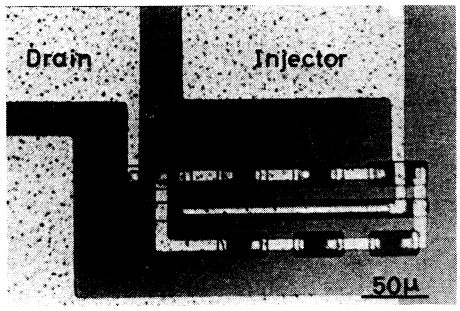
The result shown in Fig. 7 is the transfer characteristic of the circuit.[4] In Fig. 8[4,5,22] is shown the relation between supply power and time delay measured on the specimen shown in Fig. 6, compared with other published data.

The transfer characteristic is rather better compared to usual IIL prepared even with much more complicated process, the bias range for operation is extremely wide, and the minimum power for operation is as small as 30 pW in some cases, which seems to base on the low





(c)



(d)

Fig. 6. Example of 2-drain IIL prepared with twice diffusion processes.

noise properties of SIT. In some cases $P_{su} \cdot \tau_d$ product is as small as 2 fJ, and the operation as fast as 4 nsec was realized,[22] even with such simple structure and with 500 μW power supply, which is about the same with the value

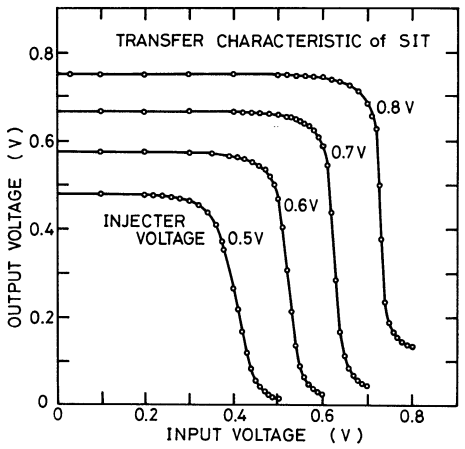


Fig. 7. An example of transfer characteristics of planar SITL shown in Fig. 6.

obtained in best IIL by BPT with complicated structure.

Figure 3(c) and (d) give examples of the static characteristics in forward operation mode.[4,5] Figure 9 is an example of the measured result of the cut-off frequency in this mode, which shows the very fast operation is realized as is expected[22] from the fact that the effective base thickness at the intrinsic gate point should be extremely thin.

Realization of the 2 fJ operation even with this very simple structure, much better than the theoretically expected value, shows that the input capacitance is mostly concerned about storage capacitance.[4] Therefore, if we introduce improved structure as shown in Fig. 10, which is prepared as the GHz high power oscillator,[23] to decrease the depletion capacitance between source and gate in the useless region for the control of the drain current and also to decrease the storage effect, much faster and much lower energy operation should be expected, because SIT with similar structure has already generate about 20 W at 2 GHz.[23]

Another improvement to realize the 10 psec operation is the application of floating gate as shown in Fig. 11. Operating gate region is nearly surrounded by the drain, and controls intrinsic gate formed by the connection with the depletion layer by the floating gate, which has fixed potential, namely by the diffusion potential or by the supplied biased voltage. An external floating gate protects the flow out of drain current without any increase of the input capacitance and also shields the signal

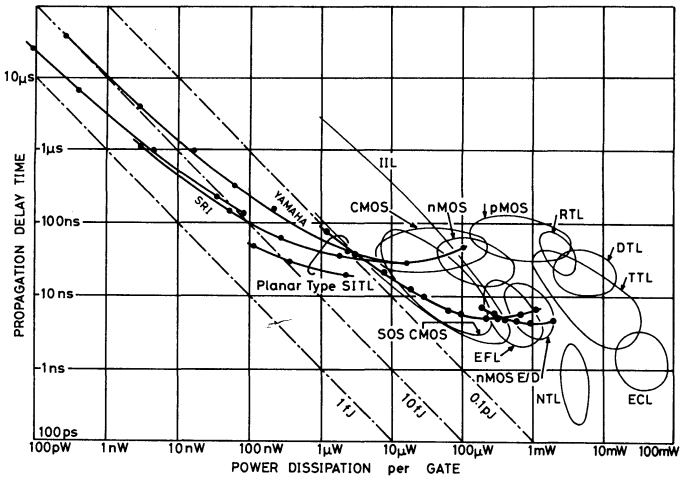


Fig. 8. Relation between energy dissipation and switch delay in various kind of integrated circuit. Even with simplest planar structure, SITL can be prepared to operate with 2 fJ at low speed range, till 4 nsec at 1 mW range and with till 30 pW as the lowest energy operation.

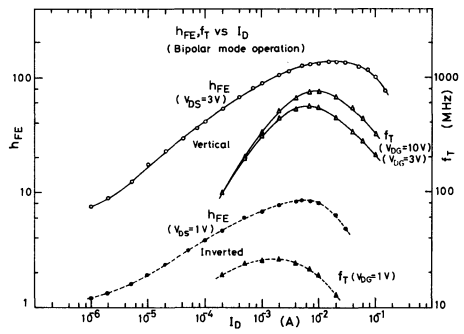


Fig. 9. Cut-off frequency in normally-off forward biased mode, which gives very high speed operation and transport factor because of the very thin effective base layer and guarded backward biased diffusion potential as shown in Fig. 5 in both direction.

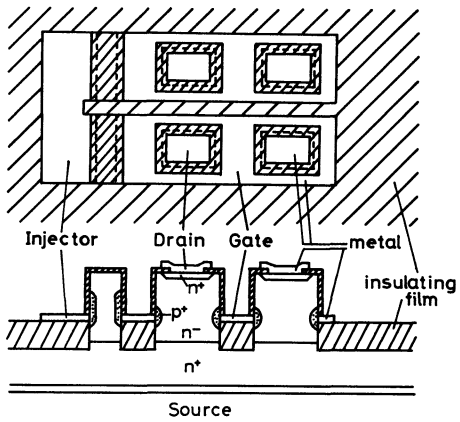


Fig. 10. Schematic diagram of SITL with improved step structure; the injector can be lateral SIT to reduces the storage effect. The insulation reduces the gate depletion layer and storage capacitances with source, and also increases the isolation between drains.

processing in the next region, because the floating gate is also doped with relatively highly concentrated impurities. And the operating gate can reduce the area of useless region which is not faced to the intrinsic gate point.

There are so many integrated circuits; those are expected to be improved by the replacement of BPT and of FET by SIT. Figure 12 shows an example of such replacement in ECL, which is also expected to be improved as a result of the reduction of storage effect and of depletion layer capacitance, for very fast speed operation.[4]

About the torelance, control of the integrated circuit of SIT is mainly the control of the gate dimensions. In the case of integration of FET, deviation of gate structure changes both the pinch-off voltage and ohmic resistance, which results V and I scatter; however, in SIT integrated circuit, only pinch-off voltage is changed and only values in voltage is scattered. As a result of experience, it has been understood much easier.

§3. Integration of SIT as a Memory Circuit (SITM)

The integrated circuit shown in Fig. 13, is an example of SITM and is named as pin-pong

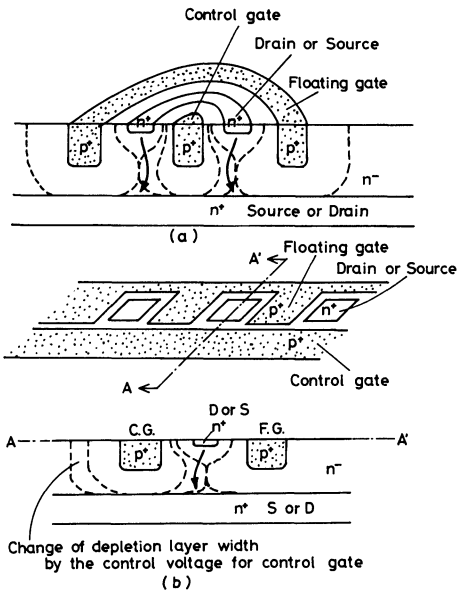


Fig. 11. High speed SITL with floating gate.

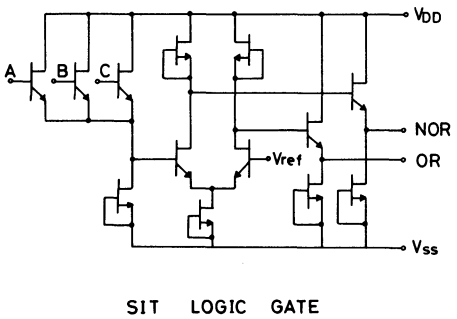


Fig. 12. An example of the replacement of BPT by SIT to reduce the time delay for switching in ECL.

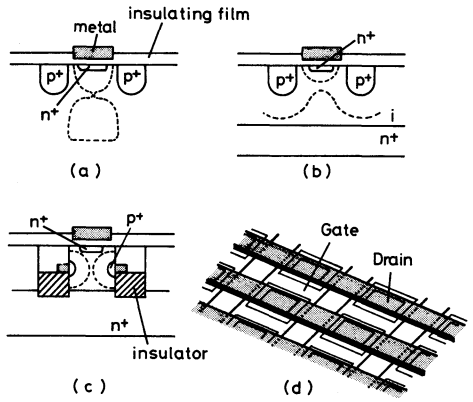


Fig. 13. SITM; Ping-Pong memory: (a) isolated Ping-Pong memory (b) common base Ping-Pong memory and purse memory: (c) three electrode high speed purse memory with insulator similar to Fig. 10 and (d) arranged high density purse memory: Diffused gate composes the address-line and bit line is wired to complete the capacitor with drain covered with thin insulating film.

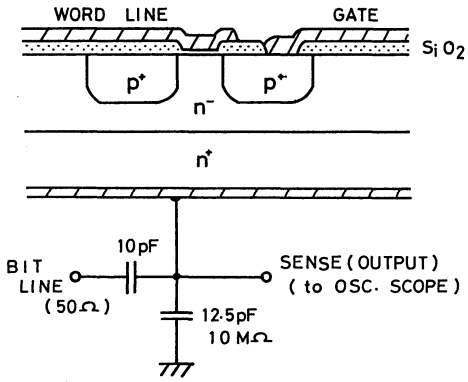


Fig. 14. Cross-sectional view of the SIT memory cell used in this experiment and circuit for the observation of output signal.

memory.[24] Source and drain is separated by the normally-off intrinsic gate point or by the BPT mode of SIT which is similar to a nearly punched-through base. The word line is connected to the gates to address the input bit signal which is applied to the bit line connected orthogonally to the drains through insulating film to form a storage capacitor between bit line and each drain as shown in Fig. 13(d), which is corresponding to the single-transistor cell RAM; it can be named as purse memory, because the purse cell surrounded by the backward biased diffusion potential is switched by a purse-string formed by gate. And the put-in or put-out is performed by the loose of the string, when the write or read voltage are applied at the same time. It can be prepared by only one or two diffusions followed by hole making and wiring. Various structures are possible for the SITM, too, which are characterized by three dimensional structures, but not by the planer structure, so that the carrier transport is in the bulk conduction but not in the surface conduction. The bulk conduction of carriers in the SIT memory operations leads to the high speed operation.

In these kinds of structure with the area of $10 \times 10\ \mu m$, primary stage of the experiment has already been performed.[24] And the results show very promising features. Fundamental operations of *n*-channel RAM are observed by using the sample shown in Fig. 14, where the output signal of the storage charge is directly

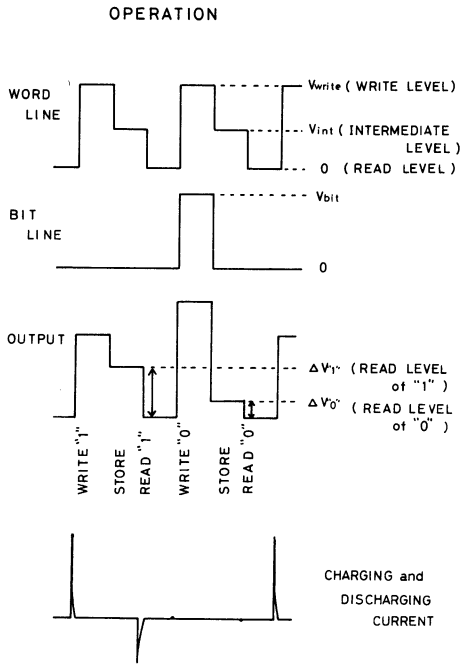


Fig. 15. Basic operational waveforms and the structure of SITM in the experiment shown in Fig. 16.

displayed on the oscilloscope. Basic operational waveforms in this experiment are shown in Fig. 15. Capacitively coupled output signals are displayed on the oscilloscope so that the waveforms seem rather complicated. Corresponding to data 1 and 0 signals, ΔV_1 and ΔV_2 are functions of the applied voltage on the word line on the bit line, and on the gate as shown in Fig. 16(a), (b) and (c). According to Fig. 16, descrimination margin between data 1 and 0 signals increases with the increases of the word line voltage V_{WRITE} and the bit line voltage V_{BIT}, while the maximum discrimination of them is obtained at the gate voltage of -6 V in this sample. In this experiment, the gate spacing of the memory cell used is not narrow enough to completely pinch-off the channel, so that the gate bias voltage is applied in order to obtain a moderate potential barrier height to establish the complete pinch-off. Therefore, dimension and the diffusion potential should be arranged to correspond to the situation with -6 V without any external voltage for the ideal design in normally off mode. Carrier transport in the SIT memory cell is very fast because of the high mobility and small capacitance, so that response times corresponding to write and read of data are too short to observe ex-

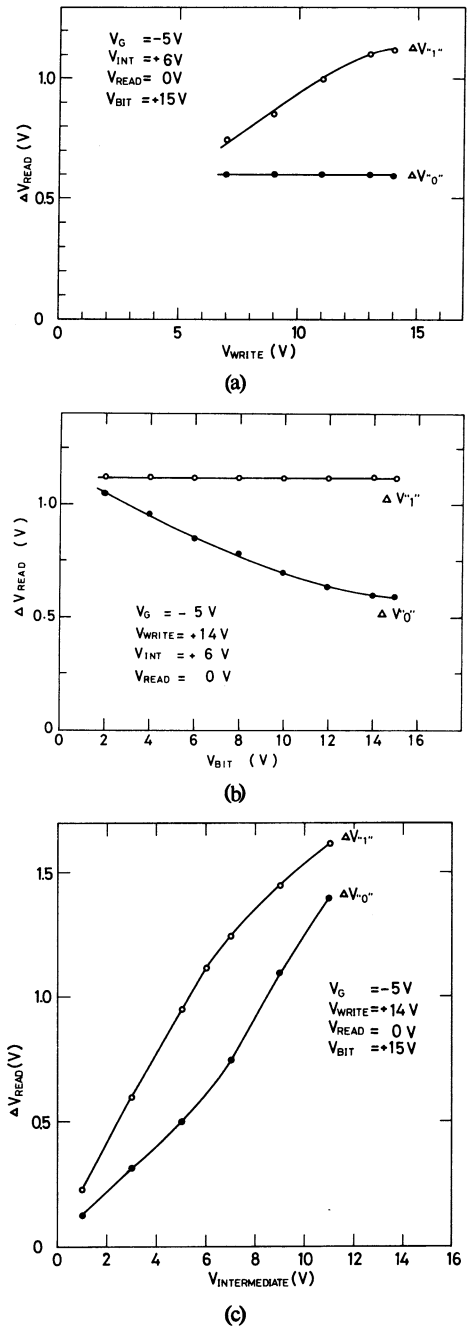


Fig. 16. Variation of data 1 and 0 signals
(a) ΔV_{READ} vs. V_{WRITE}
(b) ΔV_{READ} vs. V_{BIT}
(c) ΔV_{READ} vs. $V_{\mathrm{INTERMEDIATE}}$.

perimentally in this experiment. Observed response time is determined by the time constant of the circuit used and the output should be descriminated by the voltage step not by the pulse height, because the output circuit is capacitively

coupled to the cell in this experiment.

In this sort of structure, the transistor can be as small as 5×5 μm and can be nearly equal to the width of the word and bit lines. Then, the packing density higher than $10^6/cm^2$ may be realized with the thickness less than 1 μm as an insulating region, with even much faster speed and much lower energy for operation, compared to other integrated circuit prepared with equivalent complexity of processing.

§4. Conclusion

Integration of SIT into solid circuit is surely expectable to break through the figure of merit of today in energy, speed, packing density and even complexity of processing.

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