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Japanese Journal of Applied Physics **55**, 1202A1 (2016)
http://doi.org/10.7567/JJAP.55.1202A1

Current status of Ga_2O_3 power devices

Masataka Higashiwaki[1]*, Hisashi Murakami[2], Yoshinao Kumagai[2], and Akito Kuramata[3]

[1]*National Institute of Information and Communications Technology, Koganei, Tokyo 184-8795, Japan*
[2]*Department of Applied Chemistry, Tokyo University of Agriculture and Technology, Koganei, Tokyo 184-8588, Japan*
[3]*Tamura Corporation, Sayama, Saitama 350-1328, Japan*

*E-mail: mhigashi@nict.go.jp

Received May 27, 2016; accepted August 23, 2016; published online November 15, 2016

Gallium oxide (Ga_2O_3) is an emerging wide-bandgap semiconductor for high-power, low-loss transistors and diodes by virtue of its excellent material properties and suitability for mass production. In this paper, we begin by discussing the material properties of Ga_2O_3 that make it an attractive alternative to not only Si but also other wide-bandgap materials such as SiC and GaN. State-of-the-art Ga_2O_3-based devices that have been fabricated to date demonstrate the performance potential for power electronics applications. © 2016 The Japan Society of Applied Physics

1. Introduction

High-efficiency semiconductor power switching devices are strongly demanded by the society, because they can directly contribute to worldwide energy conservation and reduction of greenhouse gas emissions. Si-based technology has been the mainstream in power electronics as well as in communications and digital signal processing; however, it is also recognized that Si power devices are approaching their theoretical performance limits from the viewpoint of material properties.[1)] Wide-bandgap semiconductors represented by SiC and GaN possess attractive material properties for power device applications, such as much larger bandgap energies (E_g) and breakdown electric fields (E_{br}) than Si, and are thus expected to overcome the limitation of Si devices. Driven by these social and technological demands, much effort has been devoted to research and development (R&D) of SiC and GaN power devices. Recently, another wide-bandgap semiconductor material — gallium oxide (Ga_2O_3) — has emerged as a new competitor to SiC and GaN in the race toward next-generation power devices. Ga_2O_3 has some great attributes represented by its even larger E_g than those of SiC and GaN.[2–5)] One of the weaknesses of SiC and GaN devices constraining their industrialization and commercial applications is the lack of affordable native substrates. In contrast, Ga_2O_3 wafers can be fabricated in large volumes from bulk single crystals synthesized by melt-growth techniques such as floating-zone (FZ),[6,7)] Czochralski,[8,9)] edge-defined film-fed growth (EFG),[10,11)] and vertical Bridgman methods.[12)] Therefore, the production costs and thus market prices of commercial Ga_2O_3 products would be reasonably low.

In 2010, we started pioneering R&D of Ga_2O_3-based transistors and diodes to convert the promise into a reality and have since achieved several key technological milestones. Following a short introduction of material properties and features of Ga_2O_3, in this paper, we summarize the Ga_2O_3-based field-effect transistor (FET) and Schottky barrier diode (SBD) technologies developed by our group.

2. Overview of material properties and features of Ga_2O_3

Ga_2O_3 exists in five different polytypes denoted by α, β, γ, δ, and ϵ.[13)] The β-polytype with the monoclinic β-gallia structure is the most stable and the only crystal structure available for Ga_2O_3 melt growth, whereas the other phases are metastable. We have therefore been focusing our work on β-Ga_2O_3. The reported E_g values of β-Ga_2O_3 are widely distributed in the range of 4.4–4.9 eV,[2–5)] which could be due to the complexity of optical processes in Ga_2O_3. Electron densities (n) in Ga_2O_3 bulk crystals and thin films can be precisely controlled in the wide range of 10^{15}–10^{19} cm^{-3} by donor impurity doping as in the case of other semiconductors.[3,6,14,15)] Si and Sn are the most commonly used donor dopants for Ga_2O_3 with small activation energies of 30–80 meV. The room-temperature (RT) electron mobility (μ) in Ga_2O_3 melt-grown bulk crystals and homoepitaxial thin films monotonically increases from 30–60 $cm^2 V^{-1} s^{-1}$ to about 200 $cm^2 V^{-1} s^{-1}$ with decreasing n from 10^{19} to 10^{16} cm^{-3}.[15)] With further reduction in n and improvement in the crystal quality of Ga_2O_3 epitaxial thin films, the μ in the drift layers of vertical unipolar Ga_2O_3 devices can be expected to reach 250–300 $cm^2 V^{-1} s^{-1}$ for the typical n range on the order of 10^{15}–10^{16} cm^{-3}. In contrast to n-type materials, there has been no report on p-type doping and effective hole conduction in Ga_2O_3. Furthermore, self-trapping of holes in bulk Ga_2O_3, which decreases effective p-type conductivity owing to the resultant low μ, is expected from the first-principles calculation of the Ga_2O_3 band structure.[16)] The static relative dielectric constant of Ga_2O_3 films is experimentally evaluated to be approximately 10.[17,18)] Poor thermal conductivity is a potential bottleneck for Ga_2O_3; the experimental values fall in the range of 0.1–0.3 $W cm^{-1} K^{-1}$ at RT[19–22)] and are one or two orders of magnitude smaller than those of other wide-bandgap semiconductors.

The common analysis relating power device performance to basic material properties of semiconductors is discussed with values generally referred to as Baliga's figure of merit (BFOM), namely, $BFOM = \epsilon\mu E_{br}^3$ (ϵ: relative dielectric constant).[1)] The BFOMs benchmark the potential improvement in the drift region resistance of unipolar transistors and diodes by using materials with wider bandgaps than Si under ideal conditions. The estimated BFOM for Ga_2O_3 is several times larger than those for SiC and GaN and thus provides strong impetus for development of Ga_2O_3 unipolar devices. The important material properties and BFOMs of Ga_2O_3 and other major semiconductors for power devices are summarized in Table I.

3. Ga_2O_3 FETs

Our first R&D target on Ga_2O_3 devices was the fabrication

Table I. Material properties of β-Ga_2O_3 and other major semiconductors for power devices.

	Si	4H-SiC	GaN	β-Ga_2O_3
Bandgap E_g (eV)	1.1	3.3	3.4	4.5–4.9
Electron mobility μ ($cm^2 V^{-1} s^{-1}$)	1,400	1,000	1,200	200–300
Breakdown field E_{br} ($MV cm^{-1}$)	0.3	2.5	3.3	7–8
Relative dielectric constant ϵ	11.8	9.7	9.0	10
BFOM $\epsilon\mu E_{br}^3$	1	340	870	2,000–3,400
Thermal conductivity ($W cm^{-1} K^{-1}$)	1.5	2.7	2.1	0.27 [010]
				0.11 [100]

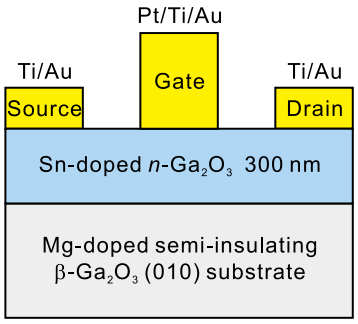

Fig. 1. (Color online) Schematic cross section of Ga_2O_3 MESFET structure.[23)]

of single-crystal Ga_2O_3 transistors to verify the viability of Ga_2O_3 as an electron device material. In this section, we summarize the technological milestones that have been achieved for Ga_2O_3 FETs to date.

3.1 Ga_2O_3 MESFETs

The first single-crystal Ga_2O_3 transistors that we successfully fabricated were metal-semiconductor FETs (MESFETs) in 2011.[23)] Figure 1 shows a cross-sectional schematic illustration of the Ga_2O_3 MESFET structure. A Sn-doped n-type Ga_2O_3 channel layer with a thickness of 300 nm was grown by molecular-beam epitaxy (MBE) on a Mg-doped semi-insulating β-Ga_2O_3 (010) substrate fabricated by the FZ method. The MESFETs showed excellent device characteristics such as a sharp drain current (I_d) pinch-off, a three-terminal off-state breakdown voltage (V_{br}) of 250 V, and an I_d on/off ratio of about four orders of magnitude at a drain voltage (V_d) of 40 V (Fig. 2). However, the devices suffered from high contact resistances (R_c) of the source and drain electrodes. In addition, its I_d on/off ratio was limited by a small leakage current through the unpassivated Ga_2O_3 surface.

3.2 Depletion-mode Ga_2O_3 MOSFETs

Next, we fabricated depletion-mode Ga_2O_3 metal–oxide–semiconductor FETs (MOSFETs) with a Sn-doped n-Ga_2O_3 channel layer grown by MBE.[24)] A schematic cross section and an optical micrograph of the device structure are shown in Figs. 3(a) and 3(b), respectively. Two novel process technologies were developed for the MOSFETs to address the shortcomings of the MESFETs. One technology was Si-ion (Si^+) implantation doping to reduce the R_c,[25)] and the other was atomic layer deposition (ALD) of an Al_2O_3 dielectric film as a gate insulator as well as surface passivation

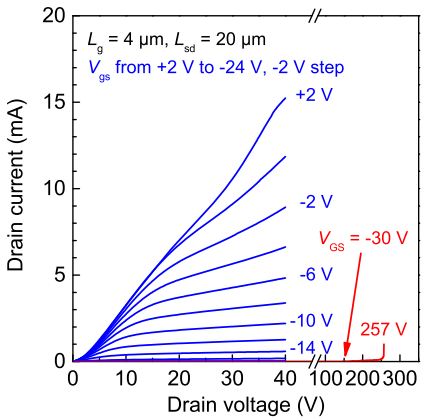

Fig. 2. (Color online) DC I_d–V_d characteristics of Ga_2O_3 MESFET.[23)]

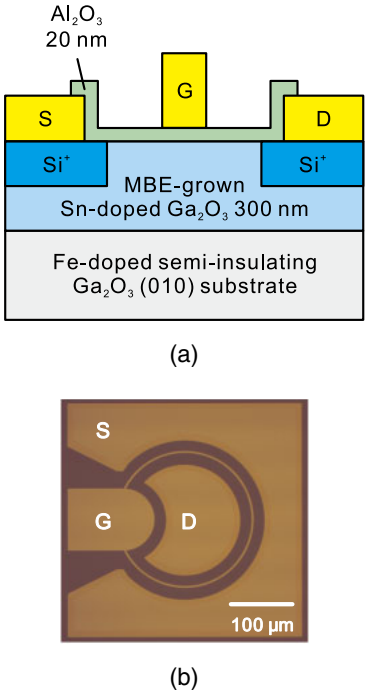

Fig. 3. (Color online) (a) Schematic cross section and (b) optical micrograph of Ga_2O_3 MOSFET structure.[24)]

layer to reduce leakage current.[26)] The Si^+ implanted ohmic contacts had a specific R_c of less than $1 \times 10^{-5}\,\Omega\,cm^2$, which was comparable to typical values for conventional Ti/Al-based alloyed contacts on n-GaN and/or AlGaN/GaN heterostructures. The Al_2O_3 gate dielectric and passivation films significantly reduced the off-state leakage current. The fabricated Ga_2O_3 MOSFETs successfully demonstrated improved device characteristics from those of the MESFETs. The maximum I_d was 39 mA/mm, and an off-state V_{br} of 370 V was achieved [Fig. 4(a)]. Furthermore, the I_d on/off ratio was higher than ten orders of magnitude [Fig. 4(b)]. Stable transistor operation was sustained at temperatures up to 250 °C; however, a significantly larger gate leakage current was measured at 300 °C. The excessive leakage was probably due to an insufficient barrier height attributed to a relatively small conduction band offset of about 1.5 eV at the ALD-Al_2O_3/Ga_2O_3 interface.

We also fabricated another type of depletion-mode Ga_2O_3 MOSFET, which had an n-type channel formed by Si^+

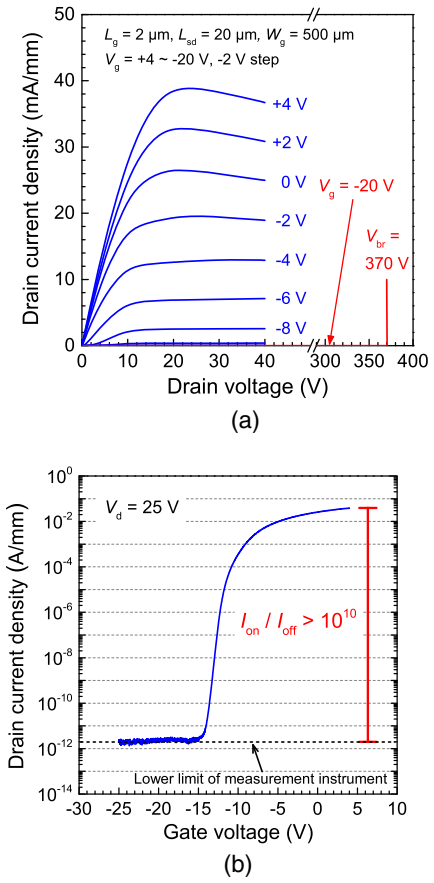

Fig. 4. (Color online) (a) DC I_d–V_d and (b) transfer characteristics of Ga_2O_3 MOSFET with MBE-grown Sn-doped channel.[24)]

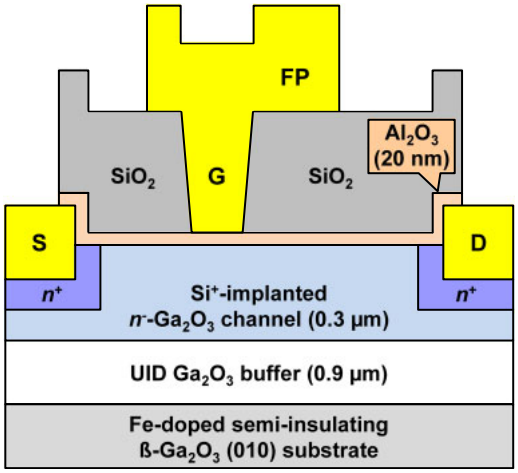

Fig. 5. (Color online) Cross-sectional schematic illustration of Ga_2O_3 FP-MOSFET structure.[28)]

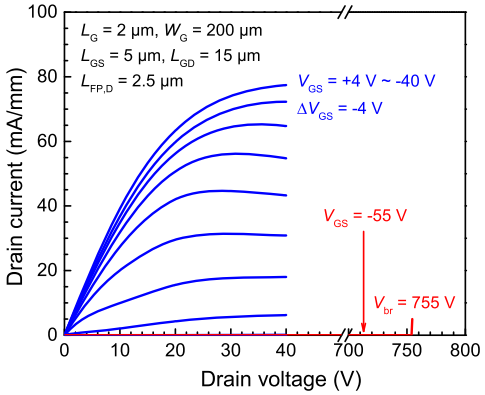

Fig. 6. (Color online) DC I_d–V_d characteristics of Ga_2O_3 FP-MOSFET.[28)]

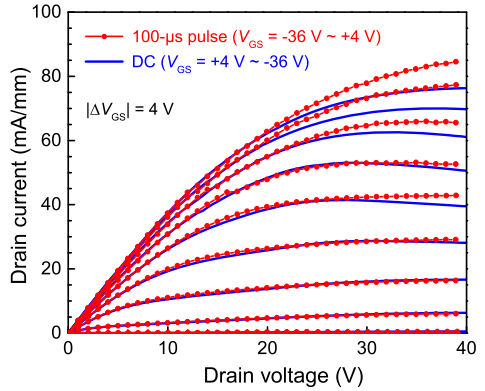

Fig. 7. (Color online) DC and pulsed I_d–V_d characteristics of Ga_2O_3 FP-MOSFET.[28)]

implantation doping of an unintentionally doped (UID) MBE-grown layer.[27)] The Ga_2O_3 MOSFETs with a Sn-doped n-Ga_2O_3 channel showed irreproducible doping profiles as a result of delayed Sn incorporation into the Ga_2O_3 epitaxial layer at the initial stage of MBE growth, leading to both poor channel thickness control and non-uniform in-plane n. To bypass the stringent requirement of precise growth temperature control within a narrow window to maintain high crystal quality and promote Sn incorporation into n-Ga_2O_3 layers, we applied Si^+ implantation doping to not only the source and drain electrodes but also the channel layer for reliable doping. All the device characteristics of the Si^+-implanted-channel MOSFETs were almost the same as or slightly better than those of the Sn-doped-channel Ga_2O_3 MOSFETs. Despite their simple structure, the MOSFETs demonstrated excellent characteristics represented by a maximum I_d of 65 mA/mm, an off-state V_{br} of 415 V, and an I_d on/off ratio of over ten orders of magnitude.

3.3 Ga_2O_3 field-plated MOSFETs

Here, we introduce the device characteristics of Ga_2O_3 field-plated MOSFETs (FP-MOSFETs), which were most recently fabricated by our group and demonstrated a record V_{br} at the time of writing this paper.[28)] Figure 5 shows a cross-sectional schematic of the Ga_2O_3 FP-MOSFET structure. The RT maximum I_d was 78 mA/mm at a gate voltage (V_g) of +4 V (Fig. 6). Successful field-plate engineering resulted in an off-state V_{br} of 755 V, which corresponded to an improvement of more than 80% over the value for the Ga_2O_3 MOSFETs without a field plate. To characterize the dynamic behavior of the FP-MOSFET, pulsed I_d–V_d measurements were performed at an off-state quiescent V_d/V_g condition of $(V_{dq}, V_{gq}) = (40\,V, -36\,V)$. V_d was swept from 0 to 40 V, while V_g was stepped from −36 to +4 V. For a pulse width of 100 μs with 0.1% duty cycle, the pulsed I_d of the FP-MOSFET matched or exceeded the corresponding DC values with no apparent degradation in on-resistance (R_{on}) (Fig. 7). Figure 8 shows the temperature-dependent transfer characteristics of the FP-MOSFET at $V_d = 30$ V. The I_d on/off ratio was higher than nine orders of magnitude at RT. The I_d–V_d characteristics

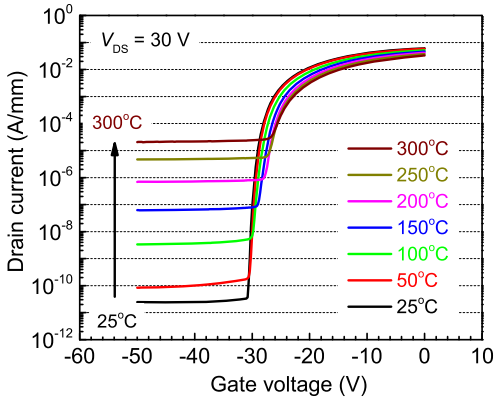

Fig. 8. (Color online) Transfer characteristics of Ga_2O_3 FP-MOSFET as a function of operating temperature.[28)]

evolved smoothly with increasing device operating temperature with no kinks or abrupt changes in behavior, indicating stable operation against thermal stress up to at least 300 °C.

4. Ga_2O_3 SBDs

SBDs constitute another important component in power conversion systems, and we have been developing Ga_2O_3 SBDs concurrently with the FETs. In early years, the SBDs lagged behind the FETs in technological progress owing mainly to the lack of suitable epitaxial growth techniques for thick n^--Ga_2O_3 layers. Since 2015, we have been able to conduct full-scale development of vertical Ga_2O_3 SBDs owing to the advancement of halide vapor phase epitaxy (HVPE) technology — a growth technique expected to be critical to the future commercialization of Ga_2O_3 devices.

4.1 Ga_2O_3 SBDs fabricated on UID Ga_2O_3 native substrates

To assess the basic device performance of Ga_2O_3 SBDs, we first fabricated simple SBD structures on a UID Ga_2O_3 (010) FZ substrate with a thickness of 600 µm.[29)] Note that n was uniform along the thickness of the substrate but showed in-plane variation from 3×10^{16}–1×10^{17} cm^{-3}, as evaluated by capacitance–voltage (C–V) measurements. The in-plane distribution of n was caused by the non-uniform density of Si atoms in the FZ bulk. Note that Si was incorporated in the five-nines-grade Ga_2O_3 powder source used for the FZ growth as an impurity. We evaluated the device characteristics of two SBDs with $n = 3 \times 10^{16}$ and 5×10^{16} cm^{-3}, which were fabricated at different locations on the same substrate. Figures 9(a) and 9(b) show the forward and reverse current density–voltage (J–V) characteristics of the SBDs, respectively. An effective Schottky barrier height at zero bias ($q\phi_{b,0}$) was extracted to be 1.3–1.5 eV for the Pt/Ga_2O_3(010) interface from both J–V and $1/C^2$–V characteristics. The specific R_{on} of the Ga_2O_3 SBDs, which were determined from the slopes of the linear regions in Fig. 9(a), were relatively high at 7.9 mΩ cm^2 for $n = 3 \times 10^{16}$ cm^{-3} and 4.3 mΩ cm^2 for $n = 5 \times 10^{16}$ cm^{-3} due to the low conductivity of the bulk substrate. Near-unity ideality factors (η) of 1.04–1.06 were estimated for both devices, which indicated the high crystal quality of the Ga_2O_3 substrate and good Schottky interface property. The reverse V_{br} values were 150 and 115 V for $n = 3 \times 10^{16}$ and 5×10^{16} cm^{-3}, respectively [Fig. 9(b)].

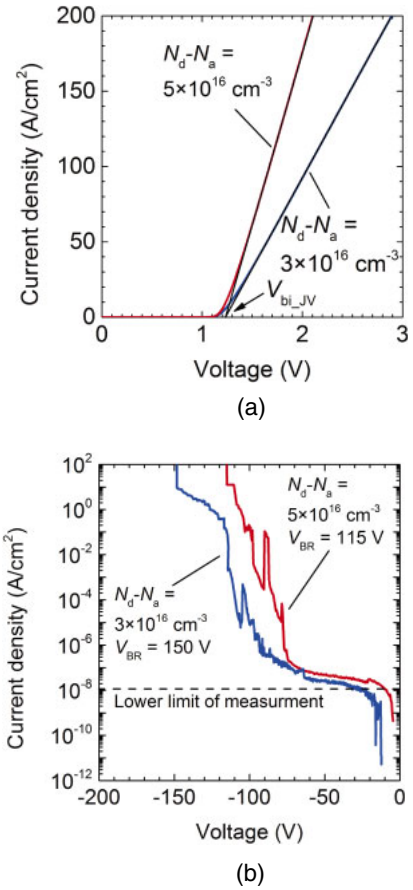

Fig. 9. (Color online) (a) Forward and (b) reverse J–V characteristics of two different Ga_2O_3 SBDs with $n = 3 \times 10^{16}$ and 5×10^{16} cm^{-3}, respectively, fabricated at different locations on the same native Ga_2O_3 substrate.[29)]

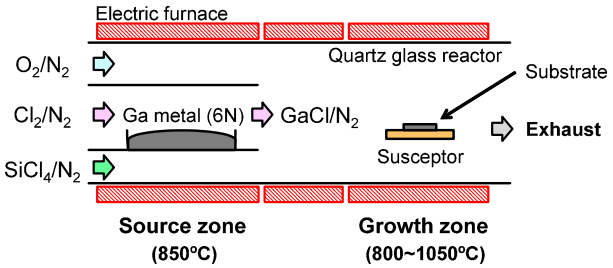

Fig. 10. (Color online) Schematic diagram of in-house-built atmospheric-pressure HVPE system for Ga_2O_3 growth.

4.2 Ga_2O_3 SBDs with an HVPE-grown drift layer

An atmospheric-pressure horizontal hot-wall HVPE system developed by our group is schematically illustrated in Fig. 10.[30)] GaCl and O_2 are source gases for the Ga_2O_3 HVPE growth. In the HVPE system, GaCl is generated by reaction between high-purity Ga metal and Cl_2 gas at 850 °C in an upstream region of the reactor. The source gases are separately introduced into a growth zone where a Ga_2O_3 substrate is placed on a quartz glass susceptor. The typical substrate temperature for Ga_2O_3 thin film growth is 1000 °C. $SiCl_4$ is simultaneously supplied during the growth for n-type doping. n can be controlled to be in the range of 10^{15}–10^{19} cm^{-3} simply by adjusting the $SiCl_4$ flow rate. The growth rate can be increased up to about 20 µm/h without compromising material quality. UID Ga_2O_3 thin films grown by HVPE possessed excellent structural and electrical properties,

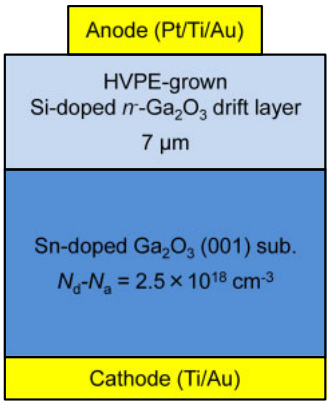

Fig. 11. (Color online) Schematic cross section of Ga_2O_3 SBD structure with HVPE-grown n^--Ga_2O_3 drift layer.[33)]

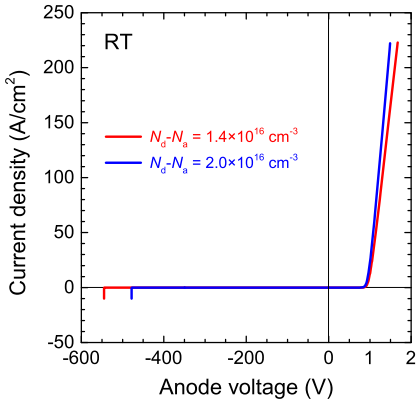

Fig. 12. (Color online) RT J–V characteristics of Ga_2O_3 SBDs with HVPE-grown n^--Ga_2O_3 drift layer.

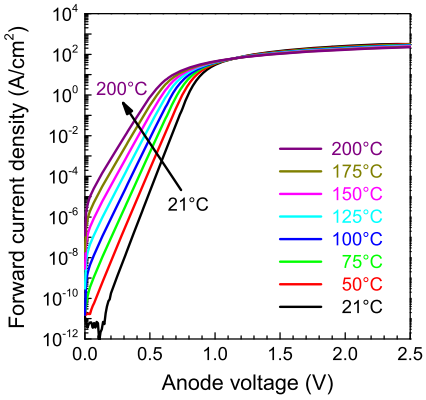

Fig. 13. (Color online) Forward J–V–T characteristics of Ga_2O_3 SBD with HVPE-grown n^--Ga_2O_3 drift layer in a temperature range of 21–200 °C.[33)]

evidenced by an X-ray rocking curve peak that is as narrow as that of a melt-grown FZ/EFG bulk crystal and an extremely low residual net carrier concentration of less than $1 \times 10^{13}\,\mathrm{cm}^{-3}$.[31)] Note that typical values of RT electron μ in HVPE-grown Si-doped Ga_2O_3 thin films were 100–150 $\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ in the n range of 10^{15}–$10^{17}\,\mathrm{cm}^{-3}$, which were comparable to the data for melt-grown bulks and MBE-grown thin films.

Figure 11 shows a schematic cross section of the SBD structure with an HVPE n^--Ga_2O_3 drift layer on a Sn-doped n^+-Ga_2O_3(001) substrate.[32,33)] Note that presently, Ga_2O_3 layers grown by HVPE have a rough surface and many pits. Therefore, the fabrication of SBDs was started with chemical mechanical polishing of the front epitaxial surface. After flattening the epitaxial layers, BCl_3-based reactive ion etching of the back side of the substrate was performed, followed by evaporation of a Ti/Au ohmic metal stack. Then, circular Schottky anode electrodes with a diameter of 200 μm were fabricated on the HVPE-grown Ga_2O_3 layers by standard photolithographic patterning, evaporation of a Pt/Ti/Au stack, and lift off. No dielectric passivation was applied to the surfaces of the epitaxial layers.

Figure 12 shows the RT J–V characteristics of the SBDs. From linear fits to the forward J–V curves within the range of $J = 100$–$200\,\mathrm{A/cm}^2$, the specific R_{on} values were estimated to be $3.0\,\mathrm{m\Omega\,cm}^2$ for the device with $n = 1.4 \times 10^{16}\,\mathrm{cm}^{-3}$ in the drift layer and $2.4\,\mathrm{m\Omega\,cm}^2$ for that with $n = 2.0 \times 10^{16}\,\mathrm{cm}^{-3}$. The reverse J–V characteristics revealed a high V_{br} of approximately −500 V for both SBDs. Note that hard breakdown events occurred with catastrophic damage in both devices due to electric-field concentration at the edge of the anode electrodes.

The performance of the Ga_2O_3 SBDs at elevated temperatures was investigated to identify fundamental diode parameters and gain insight into the properties of Pt/Ga_2O_3(001) Schottky contacts. Figure 13 shows plots of the forward temperature-dependent J–V (J–V–T) characteristics of a typical Ga_2O_3 SBD with $n = 1.2 \times 10^{16}\,\mathrm{cm}^{-3}$ in the semilogarithmic scale. These characteristics evolved smoothly with increasing operating temperature from 21 to 200 °C. The forward J–V data well fitted to the thermionic emission (TE) model:[34,35)]

$$J = A^{**}T^2 \exp\left(-\frac{q\phi_b}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right], \quad (1)$$

$$J_0 = A^{**}T^2 \exp\left(-\frac{q\phi_{b,0}}{kT}\right), \quad (2)$$

where A^{**} is the reduced effective Richardson's constant, T is the absolute temperature, $q\phi_b$ is the V-dependent Schottky barrier height, k is the Boltzmann constant, q is the electron charge, and J_0 is the saturation current density. Note that $q\phi_b$ and $q\phi_{b,0}$ include the effect of image force barrier lowering, and that $q\phi_b$ depends linearly on V for small V values. The η values extracted from the slopes of linear fits to the forward J–V curves were 1.03 ± 0.01 over the temperature range.

Figure 14 shows the reverse J–V–T characteristics measured on the same device as that for the forward J–V–T characteristics over the same temperature range, together with the theoretical curves based on the thermionic field emission (TFE) model that took into account tunneling current across the Schottky junction.[34,36)] The TFE reverse leakage current density (J_{TFE}) was calculated using the following simplified equation proposed by Hatakeyama and Shinohe:[37)]

$$J_{TFE} = \frac{A^*Tq\hbar\mathcal{E}}{k}\sqrt{\frac{\pi}{2m^*kT}} \times \exp\left\{-\frac{1}{kT}\left[\phi_{b,0} + \Delta\phi_{ifbl,0} - \frac{(q\hbar\mathcal{E})^2}{24m^*(kT)^2}\right]\right\}, \quad (3)$$

where A^* is the theoretical Richardson's constant, $\hbar$ is the reduced Planck constant, and m^* is the electron effective mass in Ga_2O_3. The term $q\Delta\phi_{ifbl,0}$ represents the potential barrier

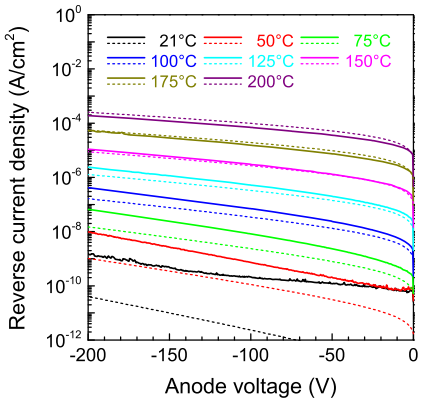

Fig. 14. (Color online) Reverse J–V–T characteristics of Ga_2O_3 SBD with HVPE-grown n^--Ga_2O_3 drift layer at 21–200 °C. Solid and dotted lines correspond to experimental and calculated values, respectively.[33)]

lowering due to the image charge induced in the Schottky metal under zero-bias condition,[34,38)] and $\mathcal{E}$ is the electric field at the Schottky interface expressed as

$$\mathcal{E} = \sqrt{\frac{2q(N_d - N_a)(V_{bi,0} - V)}{\epsilon_s \epsilon_0}}, \quad (4)$$

where ϵ_s is the relative dielectric constant of Ga_2O_3, and ϵ_0 is the vacuum permittivity. As plotted in Fig. 14, the calculated J_{TFE} are in good agreement with the experimental data especially at temperatures above 100 °C. The small discrepancies between calculation and experiment at temperatures below 100 °C could be due to leakage through the unpassivated Ga_2O_3 surface.[39)] These SBD characteristics indicated that the Pt/Ga_2O_3(001) interface was a nearly ideal Schottky contact with excellent spatial homogeneity.

5. Conclusions

Ga_2O_3 is a promising wide-bandgap semiconductor, especially for future power electronics. In this paper, we reviewed the remarkable progress on Ga_2O_3 material growth and device process technologies that has been achieved by our R&D efforts over the past five years. To further improve the performance of Ga_2O_3 devices for future commercial applications, we must address a series of technological challenges such as the production of large-size wafers with diameters of more than 6 inches, device processing, and epitaxial growth with associated doping techniques. Some basic material properties of Ga_2O_3 remain to be clarified.

We believe that Ga_2O_3 device technologies and applications will continue to be some of the most challenging and exciting topics in the compound semiconductor community and have potentials in the power electronics of current semiconductors. As a consequence, Ga_2O_3 transistors and diodes may herald a new era of high-performance and high-efficiency power electronics and help reduce global energy consumption as indispensable power switching systems.

Acknowledgments

The authors are deeply grateful to the following individuals for their dedication to the R&D project on Ga_2O_3 power devices: T. Kamimura, M. H. Wong, and K. Konishi of National Institute of Information and Communications Technology; S. Yamakoshi, T. Masui, K. Goto, and K. Sasaki of Tamura Corporation; and R. Togashi, Q. T. Thieu, and K. Nomura of Tokyo University of Agriculture and Technology. They are also grateful to Professor A. Koukitu of Tokyo University of Agriculture and Technology and Professor B. Monemar of Linköping University for fruitful discussions. This work was partially supported by Council for Science, Technology and Innovation (CSTI), Cross-ministerial Strategic Innovation Promotion Program (SIP), "Next-generation power electronics" (funding agency: NEDO).

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Masataka Higashiwaki received his B.S., M.S., and Ph.D. degrees in solid-state physics from Osaka University, Osaka, Japan, in 1994, 1996, and 1998, respectively. From 1998 to 2000, he was a Postdoctoral fellow at Osaka University. In 2000, he joined National Institute of Information and Communications Technology (NICT), Tokyo, Japan, as a Researcher. From 2007 to 2010, he took a temporary leave from NICT and joined University of California, Santa Barbara as a Project Scientist. He returned to NICT in 2010 and started a pioneering work on Ga_2O_3-based electronics. He is now a Director at Green ICT Device Advanced Development Center.

Hisashi Murakami received the doctorate in 2005 from Tokyo University of Agriculture and Technology (TUAT). He became a Research Associate at the Institute of Symbiotic Science and Technology of TUAT in 2005 and is currently an Associate Professor at the Institute of Engineering of TUAT. His research focus is on the growth of III-oxide and the bulk crystal growth of III–nitride semiconductors including their alloys.

Yoshinao Kumagai received the doctorate in 1996 from University of Tsukuba. From 1996 to 1999, he joined Texas Instruments Tsukuba Research & Development Center Ltd. He became a Research Associate at the Faculty of Technology of Tokyo University of Agriculture and Technology (TUAT) in 1999 and is currently a Professor of TUAT. His research focus is on the vapor phase epitaxy and characterization of group-III nitrides and oxides.

Akito Kuramata was born in Itoigawa, Japan, in 1963. He received the B.E. degrees from Kyoto University, Kyoto, Japan, in 1986. He joined Fujitsu Laboratories Ltd., Atsugi, Japan. He moved to Tamura Corporation, Sayama, Japan, in 2008. He established Novel Crystal Technology, Inc. in 2016. He has been engaged in research and development of crystal growth and device process for compound semiconductor devices such as laser diodes, optical detectors, diodes, transistors and so on.