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Multiple negative differential resistance devices with ultra-high peak-to-valley current ratio for practical multi-valued logic and memory applications

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In this paper, we propose a novel multiple negative differential resistance (NDR) device with ultra-high peak-to-valley current ratio (PVCR) over 10^6 by combining tunnel diode with a conventional MOSFET, which suppresses the valley current with transistor off-leakage level. Band-to-band tunneling (BTBT) in tunnel junction provides the first peak, and the second peak and valley are generated from the suppression of diffusion current in tunnel diode by the off-state MOSFET. The multiple NDR curves can be controlled by doping concentration of tunnel junction and the threshold voltage of MOSFET. By using complementary multiple NDR devices, five-state memory is demonstrated only with six transistors.

1. Introduction

The negative differential resistance (NDR) devices are promising alternative device performing multifunctional operation based on its nonmonotonic behavior.[1–5] Since the tunnel diode with NDR characteristics has been discovered by Esaki,[6] there have been in problems for practical applications owing to low peak-to-valley current ratio (PVCR) below 10 by trap-assisted tunneling (TAT) current through forbidden band-gap and CMOS incompatible process or compound materials.[7–9] For the improvement of PVCR over 100 based on CMOS compatible process, many research works have been reported focusing on the metal–oxide–semiconductor field-effect transistor (MOSFET) structures. Enhanced surface generation in SiGe-based gate diode is exploited for PVCR of 300 around at 3 V,[10] and the breakdown mechanism of gated bipolar device shows PVCR of 10^3 at 2.5 V.[11] Other researches succeed to obtain high PVCR at relatively low operation voltage by suppressing transistor's on current at the off-leakage level with another depletion mode MOSFET or inverter circuit.[12,13] In terms of multiple NDR characteristics for multi-valued logic (MVL) and memory (MVM) applications, however, it needs more complicated circuit for three-state logic at 3 V.[14] In other multiple NDR-based MVL and MVM applications, tri-state latch circuit has been demonstrated by using the series connection of resonant interband tunneling diodes (RITDs) with double-peak based on InAs/AlSb/GaSb at 1.5 V (PVCR = 17) or Si/SiGe with at 3 V (PVCR = 3.25).[15,16] For the multiple NDR device satisfying both ultra-high PVCR and low operation voltage, the pn tunnel junction-embedded silicon (Si) nanowire (NW) structure has been presented with ultra-high PVCR over 10^4 at 1 V under the two independent input biases in our previous works.[17,18]

In this paper, we propose further improved and practical NDR device based on pn tunnel junction-embedded conventional Si MOSFET structure having a single input bias and compatibility with CMOS process, which still maintains its outstanding characteristics of multiple peak and ultra-high PVCR over 10^6 at 1 V. In Sect. 2, the device operation principle and multiple switching characteristics will be explained based on the energy band diagram. Subsequently, the effects of device design parameters on the multiple NDR characteristics are investigated in Sect. 3. In addition, using only six devices, the five-state latch circuit simulation is demonstrated for MVL/MVM applications.

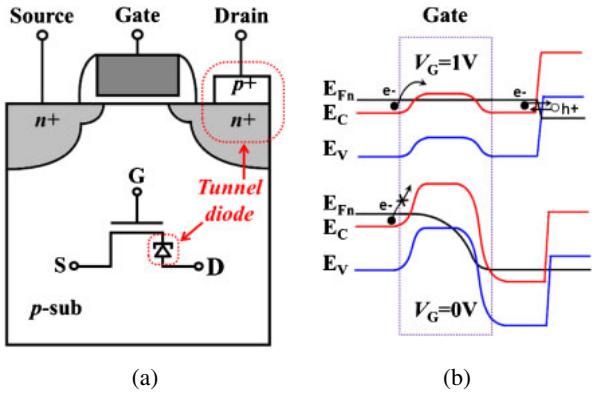

Fig. 1. (Color online) (a) Device structure and circuit symbol of the proposed nNDR device combining pn tunnel diode with n-MOSFET (b) energy-band diagrams with the carrier (electron) injection mechanism at the on-state (upper one) and the off-state (lower one) of n-MOSFET. The pNDR based on p-MOSFET can be implemented in a complementary way.

2. Operation principle of multiple NDR device

Figure 1(a) shows the two-dimensional (2D) cross-sectional view and circuit symbol of the proposed n-type NDR (nNDR) device based on the simple n-MOSFET structure with a degenerately doped pn tunnel junction at the drain side. In our simulation work, complementary p-type NDR (pNDR) device also can be implemented based on p-MOSFET with the tunnel diode, which has been designed with both n+ and p+ doping concentration of $1 \times 10^{20}\,\mathrm{cm}^{-3}$ and a typical junction contact area of $100 \times 100\,\mathrm{nm}^2$. Figure 1(b) explains the key role of tunnel junction-embedded MOSFET for the multiple NDR with ultrahigh PVCR by using each energy band diagram at the different gate voltages. When the tunnel junction-embedded MOSFET operates at the on-state (upper one), it supplies the channel electrons to tunnel diode and then, the first NDR curve by the current owing to band-to-band tunneling (BTBT), TAT, and diffusion as in a normal tunnel diode can be obtained. In the off-state (lower one) case, high channel potential barrier of tunnel junction-embedded MOSFET inhibits the flow of electrons so that the device current can be suppressed at MOSFET off-current level.

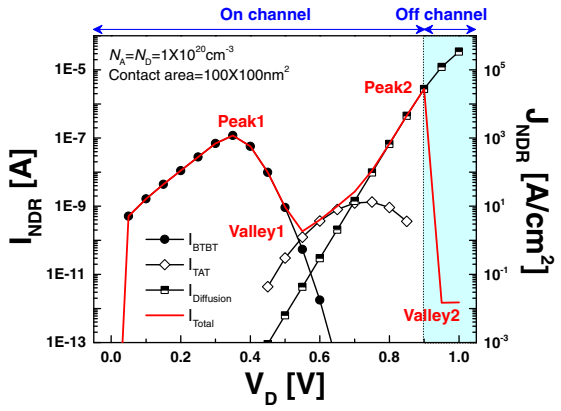

Fig. 2. (Color online) Simulated multiple NDR *I–V* characteristics with PVCR over 10^6 at 1 V. Peak1 and valley1 is governed by I_{BTBT} and I_{TAT} at on channel MOFSET, and peak2 and valley2 is formed by suppressing $I_{Diffusion}$ at off channel MOSFET.

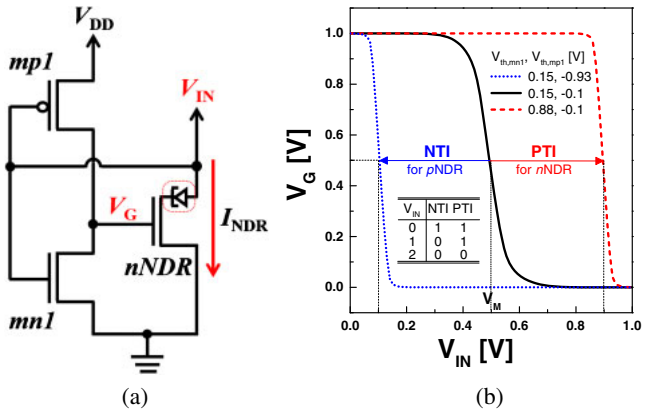

Fig. 3. (Color online) (a) Circuit scheme of CMOS inverter-incorporated nNDR for multiple NDR curves with a single input biasing (V_{IN}) (b) VTC of CMOS inverter with various $V_{th,mn1}$ and $V_{th,mp1}$. The PTI and NTI are used for nNDR and pNDR, respectively.

Figure 2 shows the simulated multiple NDR current–voltage (*I–V*) characteristic with ultra-high second PVCR over 10^6 at $V_{DD} = 1$ V based on the proposed operation principle where the first peak (peak1) and first valley (valley1) are generated by typical tunnel diode behavior having BTBT and TAT current (I_{BTBT} and I_{TAT}) under the on channel MOSFET and the subsequent second peak (peak2) and second valley (valley2) can be formed from the suppression of diffusion current ($I_{Diffusion}$) by intentionally making MOSFET the off channel state. Device simulation was performed using a Sentaurus™ 3D TCAD device simulator with our numerical BTBT model in order to describe BTBT mechanism (peak1) in forward bias of tunnel diode.[19,20] For the valley1 current through a forbidden band-gap, field-enhanced TAT model is used.[21]

To obtain multiple NDR characteristics with the single input bias (V_{IN}), the circuit composition of CMOS inverter (mn1 and mp1) is introduced between the gate and drain of proposed NDR device as shown in Fig. 3(a).[22,23] Figure 3(b) shows the various voltage transfer curves (VTCs: V_G–V_{IN}) of the inverter according to the threshold voltage of mn1 and mp1 ($V_{th,mn1}$ and $V_{th,mp1}$). When the $V_{th,mn1}$ is increased from 0.15 to 0.88 V, the transition voltage (V_M) is increased from 0.5 V (black-solid line) to 0.9 V (red-dashed line) in

Table I. Second NDR characteristics according to transition voltage (V_M) of inverter.

V_M (V)	I_{peak2}	$I_{valley2}$	2nd PVCR
<0.6[a)]	Second NDR does not make		
0.7	2.7×10^{-9}	1.4×10^{-12}	1.9×10^3
0.8	4.4×10^{-8}	1.4×10^{-12}	3.1×10^4
0.9	1.8×10^{-6}	1.4×10^{-12}	1.3×10^6
1.00	2.5×10^{-5}	3.5×10^{-6}	7.1

a) $V_{valley1}$

companied with faster switching characteristic owing to transition at the subthreshold region, which lead to high second PVCR and NDR gain. When the V_M of inverter is much higher/lower than half of V_{DD}, it is conventionally referred to the positive/negative ternary inverter (PTI/NTI) with a truth table in the inset of Fig. 3(b), and each PTI and NTI is practical for nNDR and pNDR in a complementary way.[24] Table I represents the currents of peak2 (I_{peak2}) and valley2 ($I_{valley2}$) and second PVCR according to the various V_M. By increasing the V_M up to 0.9 V, the second PVCR over 10^6 can be obtained with exponentially increased I_{peak2}. On the other hand, when the V_M is larger than 0.9 V, the $I_{valley2}$ is increased since the low (GND)-state could not be transferred to V_G and tunnel junction-embedded MOSFET still supplies the channel electrons to pn tunnel diode.

3. Results and discussion

The multiple NDR characteristics can be controlled by design parameters such as doping concentration of tunnel junction and the gate workfunction (WF) of the tunnel junction-embedded MOSFET as shown in the Figs. 4(a) and 4(b), respectively. Figure 4(a) shows that the currents of peak1 (I_{peak1}) and valley1 ($I_{valley1}$) by BTBT and TAT increased by field enhancement when the doping concentration of pn tunnel junction increased from 1×10^{20} to 5×10^{20} cm^{-3} without changing second NDR characteristics with I_{peak2} and $I_{valley2}$ in this degenerately doping range. These simulated doping-dependent I_{peak1} have been compared to experimental data of Si tunnel junction based on BTBT mechanism.[20] Figure 4(b) indicates that the second PVCR can be determined by the off-current of the tunnel junction-embedded MOSFET at $V_G = 0$ V, under the condition that the on-current of the MOSFET is larger than I_{peak1} for first NDR in order to allow the tunneling in the embedded junction. When the threshold voltage of tunnel junction-embedded MOSFET (V_T) increases by changing the gate WF with 150 meV, second PVCR increases from 10^3 to 10^6 since the MOSFET off-current (valley2) exponentially decrease by $\exp(-\Delta V_T/mk_BT)$ where $m = 1.1$–1.4 at T = 300 K.[25] Therefore, we can control each first and second NDR by using design parameter of pn tunnel junction and its embedded MOSFET, respectively.

The complementary *I–V* characteristics of nNDR with PTI and pNDR with NTI are demonstrated by both well-matched device (symbol) and circuit (line) simulation as shown in Fig. 5. HSPICE circuit simulation was performed using the BSIM4 model (level 54) and piecewise linear current source for peak1 and valley1.[26] The MVM applications could be demonstrated based on the NDR-SRAM circuits consisted of two nonmonotonic NDR devices as shown in the inset

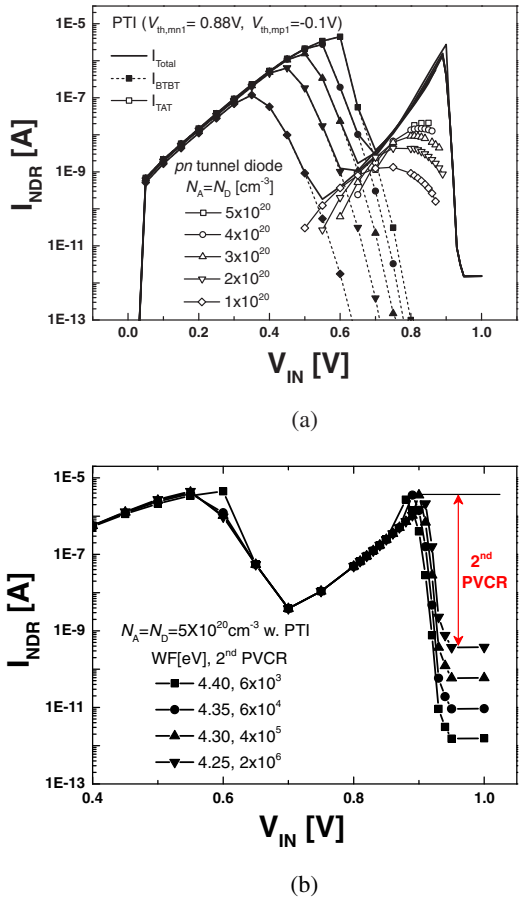

Fig. 4. (Color online) Simulation results of *I–V* characteristics with various design parameters: (a) pn doping concentrations of tunnel junction and (b) the gate WF of MOSFET in NDR device. The first and second NDR can be controlled by using design parameters of pn tunnel junction and MOSFET, respectively.

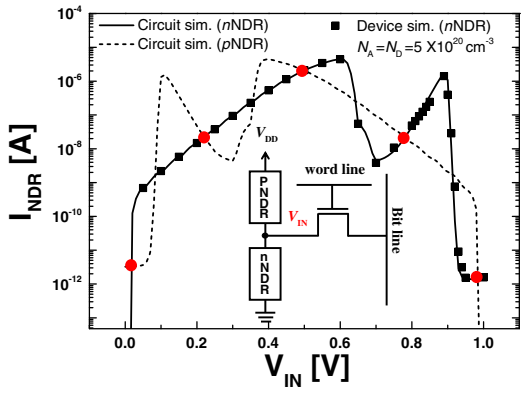

Fig. 5. (Color online) Simulated multiple NDR *I–V* characteristics of nNDR and pNDR from the device and circuit simulations. Inset shows the NDR-SRAM circuit configuration with complementary nNDR and pNDR.

of Fig. 5, which has strength on the bit density carrying maximum $2l+1$ states with l-peak NDR devices comparing with maximum $l+1$ states of monotonic load elements such as resistance, capacitance, or current source.[27,28] The serially connected double-peak n/pNDRs have nine-crossing points in the *I–V* characteristics. Among them, only the five-crossing points in the positive differential resistance (PDR) region go into stable operating points which are represented

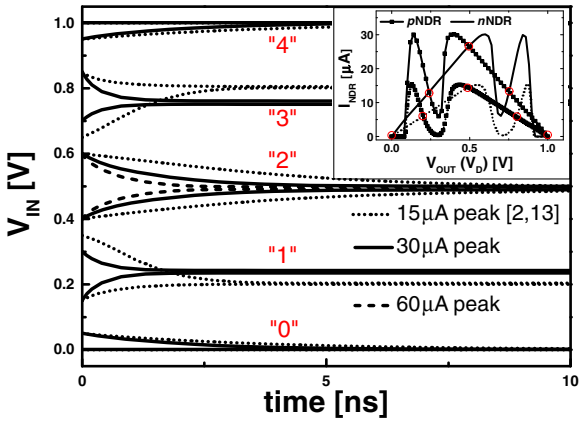

Fig. 6. (Color online) Transient simulation results of the latch circuit. Initial states of V_{IN} with variations of ±100 mV are converged to five-states. The dotted line's first peaks and PVCR are referenced by experimental data.[7,30]

as red circuits in Fig. 5. The voltages of stable operating points become logic or memory states, and the converging range of each state is subdivided by the criteria of the other unstable operating points.[29]

Figure 6 shows the transient simulation results of the latch circuit demonstrating five-state latch with only six transistors. Initial state of V_{IN} with variation of ±100 mV are converted to five-state, and its final stable voltages are determined by crossing points. By obtained the voltage of peak1 (V_{peak1}) above $V_{DD}/2$ as in Fig. 5, the delay for the "2" state can be comparable with other states since the stable operating point is crossing around the high peak current not the low valley's one. Moreover, the first PVCR becomes less important than second PVCR in this operating condition. For the realistic delay estimation, Si tunnel diode experimental data have been referenced as the peak current level of 15 μA[30] and first PVCR of 5[7] in the dotted line results, and the inset of Fig. 6 shows the *I–V* characteristics used for transient simulation. As shown in the simulation results with solid and dashed line, delay can be more reduced below 5 ns by increasing the peak currents up to 60 μA. Thus, it can be expected that the speed of five-state MVL/MVM operating can be enhanced further by developing the tunnel junction technology with high peak current density. In terms of power consumption, it should be noted that the MVL/MVM with N states takes the reduced number of bits with $m = \log_N(2^n)$ in comparison with n-bit binary logic for the same amount of data processing ($N^m = 2^n$).[31,32] Thus, in our case of 5-state MVL/MVM, the 57% reduced number of bit can be obtained from $m = n\log_5(2) = 0.43n$ and thus, the 35.5% reduced power consumption can be expected as $P_{5\text{-state}} = (6/4) \times 0.43 \times P_{binary}$ since m-bit processing requires six transistors in our device while four transistors process n-bit in conventional latch circuit.

4. Conclusions

We propose the novel NDR device with ultra-high PVCR over 10^6 having complementary multiple NDR characteristics at 1 V operation based on pn tunnel junction-embedded MOSFET structure and PTI/NTI circuit composition. Multiple NDR characteristics have been investigated with the analysis of each current component according to the device

design parameters. The five-state memory can be obtained with 6 transistors in a complementary NDR-based latch circuit.

Acknowledgments

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