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## Thin channel $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFETs with self-aligned refractory metal gates

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We report the first demonstration of self-aligned gate (SAG)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> metal-oxide-semiconductor field-effect transistors (MOSFETs) as a path toward eliminating source access resistance for low-loss power applications. The SAG process is implemented with a subtractively defined and etched refractory metal, such as Tungsten, combined with ion-implantation. We report experimental and modeled DC performance of a representative SAG device that achieved a maximum transconductance of 35 mS mm<sup>-1</sup> and an on-resistance of  $\sim 30 \Omega$  mm with a 2.5  $\mu$ m gate length. These results highlight the advantage of implant technology for SAG  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFETs enabling future power switching and RF devices with low parasitic resistance. Not subject to copyright in the USA. Contribution of Wright-Patterson AFB

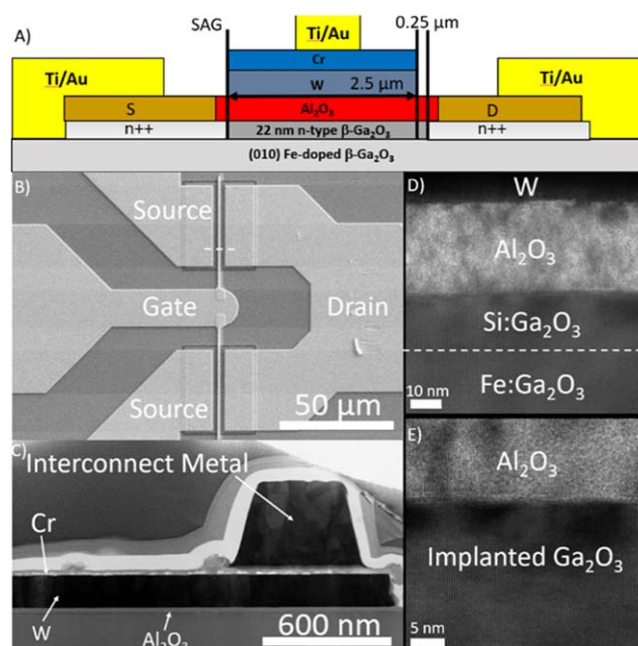
Interest in beta-phase Gallium Oxide ( $\beta$ -Ga<sub>2</sub>O<sub>3</sub>) as a next-generation ultra-wide bandgap semiconductor is due to its potential for use in high efficiency power applications.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> possesses a bandgap of  $\sim 4.8$  eV with an estimated critical field strength ( $E_c$ ) of  $\sim 8$  MV cm<sup>-1</sup> which is 2–3  $\times$  higher than GaN and SiC.<sup>1,2)</sup> Power switching conduction losses, defined by Baliga's figure of Merit,<sup>3)</sup> are a cubic function of  $E_c$ , and empirical  $E_c$  values for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> have already surpassed the theoretical limits for GaN and SiC.<sup>4)</sup>  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> metal-oxide-semiconductor field-effect transistors (MOSFETs) have demonstrated the ability to block high voltages near and surpassing 1 kV in depletion<sup>5–9)</sup> and enhancement<sup>10,11)</sup> mode operation. For  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> RF devices, the Johnson's figure of Merit<sup>12)</sup> compares favorably to GaN as reports of modeled saturation velocity reach as high as  $\sim 2 \times 10^7$  cm s<sup>-1</sup>.<sup>13)</sup> Low-GHz  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> RF power devices have been reported<sup>14)</sup> as well as high frequency small signal results with T-gates.<sup>15,16)</sup>

Most early device results, however, suffer heavily from resistive parasitic losses both in the drift ( $R_{\text{drift}}$ ) and source access ( $R_s$ ) regions. The  $R_s$  is a critical device parameter that limits device transconductance ( $G_M$ ) expressed as:

$$G_{M,\text{ext}} \approx G_{M,\text{int}} \cdot (1 + R_s \cdot G_{M,\text{int}})^{-1}. \quad (1)$$

$G_{M,\text{ext}}$  is the extrinsic  $G_M$  measured in saturation with parasitic losses and  $G_{M,\text{int}}$  is the intrinsic value. Removal of parasitic resistance such as access resistance ( $R_{s,\text{access}}$ ) is imperative for lateral device scaling due to  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>'s low mobility relative to other materials. For example, the sheet resistance of GaN HEMTs are typically at least an order of magnitude lower than previously reported  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channels.

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> is amenable to Si ion-implant; therefore, it is the only semiconductor material with a band gap larger than SiC that can be designed with a self-aligned gate (SAG) process. A SAG process was previously reported for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> that eliminated  $R_{s,\text{access}}$  with better DC performance compared to non-SAG devices.<sup>17)</sup> Here, we expand on the SAG process, device characterization and benchmark the results. The measured  $G_{M,\text{ext}}$  and  $I_{\text{DS}}$  is among the highest measured for Ga<sub>2</sub>O<sub>3</sub> MOSFETs. A Sentaurus TCAD device simulation is

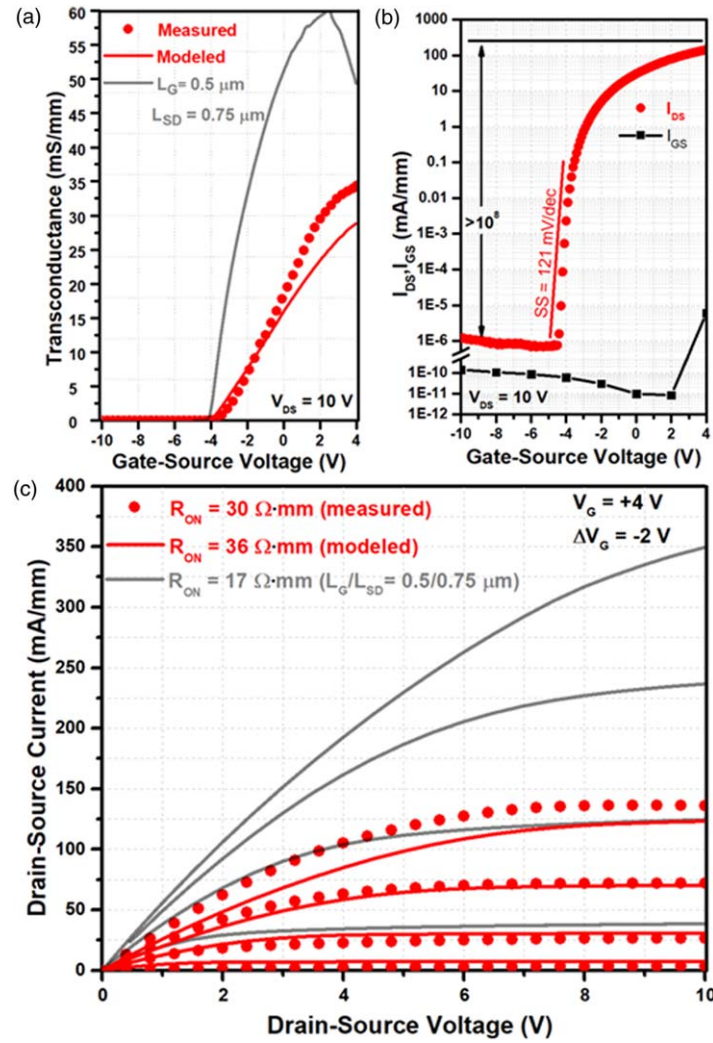


**Fig. 1.** (Color online) (a) Schematic of a SAG  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFET, (b) top-down SEM image of a representative  $2 \times 50$  SAG MOSFET with a dashed line indicating the cross-sectioned region, (c) TEM image of gated region showing gate metals and Al<sub>2</sub>O<sub>3</sub>/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> interface, (d) HR-TEM image of the W gate electrode, gate oxide and  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate, and (e) HR-TEM of the gate oxide and implanted  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channel.

included to support the measured data and predict performance with deep sub-micron gate length scaling.

The device sample was prepared with a single 22 nm thick Si-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> homoepitaxial channel layer grown by metal organic vapor phase epitaxy directly on a semi-insulating (010) Fe-doped substrate at Leibniz-Institut für Kristallzüchtung -Berlin, Germany.<sup>18)</sup> The device fabrication process began by depositing  $\sim 30$  nm of Al<sub>2</sub>O<sub>3</sub> by plasma-enhanced atomic layer deposition to serve as the gate dielectric as well as an implant cap. Next, a W refractory metal layer was sputtered and patterned with a Cr hard mask to subtractively define a 2.5  $\mu$ m W/Cr gate electrode with SF<sub>6</sub> reactive ion etch (RIE) chemistry. A refractory metal gate is





**Fig. 2.** (Color online) Linear transfer (a), log transfer (b) and output (c) characteristics of an experimental and modeled SAG  $\beta\text{-Ga}_2\text{O}_3$  MOSFET with  $L_G = 2.5 \mu\text{m}$  and  $L_{SD} = 2.75 \mu\text{m}$ , as well as the projected electrical performance of a SAG MOSFET with  $L_G = 0.5 \mu\text{m}$  and  $L_{SD} = 0.75 \mu\text{m}$  to show expected effect of device scaling.

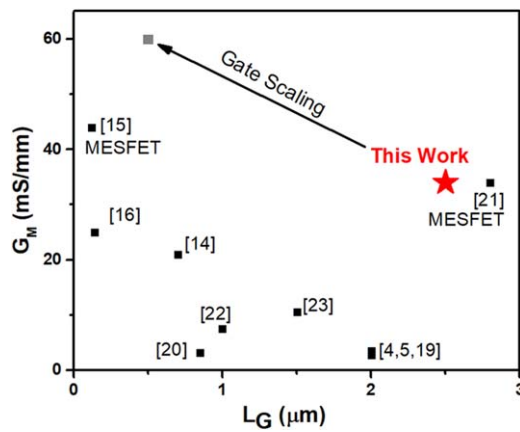
vital to a self-aligned process because an Au-based gate metal stack would not remain intact at the required implant activation temperature. Si-implant regions were then patterned with the source-side of the W/Cr gate exposed to eliminate the gate-source region ( $L_{GS} = 0 \mu\text{m}$ ), while the gate-drain distance ( $L_{GD}$ ) remained, measuring  $0.25 \mu\text{m}$ . A shallow Si-implant profile was designed with 10 and 35 keV energies with a total dose of  $1 \times 10^{15} \text{ ions cm}^{-2}$  to achieve a target  $1 \times 10^{20} \text{ cm}^{-3}$  doping concentration. The Si-implant was activated at  $900^\circ\text{C}$  for 120 s using rapid thermal annealing (RTA) in a  $\text{N}_2$  ambient. Ohmic contact to the implanted regions was achieved with a Ti/Al/Ni/Au evaporated metal stack followed by a  $470^\circ\text{C}$  RTA process for 1 min in a  $\text{N}_2$  ambient after removing the implant cap with RIE. Electrical isolation was achieved with inductively coupled plasma/reactive ion etching. Finally, additional Ti/Au gate and interconnect metal was added for device characterization.

Displayed in Fig. 1(a) is a schematic of a representative  $\beta\text{-Ga}_2\text{O}_3$  SAG MOSFET. The source-drain distance ( $L_{SD}$ ) between the implanted regions is  $\sim 2.75 \mu\text{m}$  and the gate length ( $L_G$ ) is  $\sim 2.5 \mu\text{m}$ . Van der Pauw test structures were measured after fabrication to track sheet charge density ( $n_{sh}$ ), sheet resistance ( $R_{sh}$ ) and mobility ( $\mu$ ) with average

values of  $n_{sh} = 4.96 \times 10^{12} \text{ cm}^{-2}$ ,  $R_{sh} = 2.6 \times 10^4 \Omega \text{ sq}^{-1}$ , and  $\mu = 48.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , respectively. The  $R_{sh}$  and  $R_C$  of the implanted regions are on the order of  $2.0 \times 10^3 \Omega \text{ sq}^{-1}$  and  $1.5 \Omega \text{ mm}$  respectively based on measurements from samples with a similar doping profile.

A scanning electron microscope image of the  $2 \times 50$  SAG MOSFET is shown in Fig. 1(b). High-resolution transmission electron microscopy (HR-TEM) inspection images of the SAG MOSFET were prepared in the regions under the gate and on the source-side of the gate with Si ion-implantation [see Figs. 1(c)–1(e)]. Lattice planes of (010)  $\beta\text{-Ga}_2\text{O}_3$  are visible in the implanted region showing no structural defect following the implant activation anneal. Similarly, the gate dielectric appears preserved after  $900^\circ\text{C}$  implant activation with no indication of polycrystalline domains, and the W gate electrode maintains a sharp interface with the gate dielectric layer.

The DC  $I$ - $V$  characteristics of the SAG MOSFET are shown in Figs. 2(a)–2(c). The transfer curve is shown in Fig. 2(a) indicating a maximum  $G_M = 35 \text{ mS mm}^{-1}$  measured at  $V_{DS} = 10 \text{ V}$ . The maximum current density ( $I_{DS}$ ) is  $\sim 140 \text{ mA mm}^{-1}$  at  $V_{DS} = 10 \text{ V}$ , while the device demonstrates good pinch-off characteristics with an  $I_{ON}/I_{OFF}$  greater than  $10^8$ . An excellent subthreshold swing of  $121 \text{ mV dec}^{-1}$



**Fig. 3.** (Color online)  $G_M$  versus  $L_G$  Benchmarking of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FETs from this work (red), historical (black) and a projection applying this process with sub- $\mu$ m gate scaling (gray).

was extracted from the log  $I_{DS}$ - $V_{GS}$  curve in Fig. 2(b) which is indicative of the strong channel control expected from a large  $L_G$  and ultra-thin MOSFET channel. Additionally, no adverse effects of implant activation on gate leakage were observed at  $-10$  V gate bias [see Fig. 2(b)]. The output family of curves is displayed in Fig. 2(c) obtained over a range of  $V_{GS}$  from  $+4$  to  $-2$  V including an on-resistance ( $R_{ON}$ ) of  $30 \Omega \text{ mm}$  at  $V_{GS} = 4$  V calculated from a linear fit at small  $V_{DS}$ . The  $R_{ON}$  near the ideal flat-band voltage ( $V_G = 0$ ) was calculated with a series resistance model based on the sum of contact resistance ( $R_C$ ), access resistance ( $R_{access}$ ), channel resistance ( $R_{channel}$ ), and drift region ( $R_{drift}$ ) to be  $\sim 73 \Omega \text{ mm}$  which is in good agreement with  $\sim 70 \Omega \text{ mm}$  extracted from the model and measurement in Fig. 2(c).

The modeled results in Figs. 2(a)–2(c) (solid lines) were constructed by solving the drift-diffusion electron transport equation in ISE Sentaurus Device of the same SAG MOSFET. The model uses dimensions extracted from TEM measurements, as well as material properties ( $n_{sh}$ ,  $\mu$ ,  $R_{sh}$ ) from the measured device or nearest test structure. The Al<sub>2</sub>O<sub>3</sub> thickness was also extracted from the HR-TEM image, and the dielectric constant was assumed to be 9.6. The model is in excellent agreement with the measured results with only some deviation at forward gate bias. The discrepancy is likely due to ideal assumptions concerning electron accumulation, channel doping uniformity, and trapping effects. Thermal effects were not considered but are expected to have an impact at higher  $V_{DS}$  and  $V_G$  bias and especially for an aggressively scaled device (e.g. where dissipated power is greater). Modeling of the same device with  $L_G = 0.5 \mu\text{m}$  is included (gray) here to observe the benefits of  $L_G$  scaling under the assumption that temperature will be effectively managed, such as by pulsed operation. With a reduced gate length, a significant improvement in  $G_M$ ,  $I_{DS}$ , and  $R_{ON}$  to  $60 \text{ mS mm}^{-1}$ ,  $350 \text{ mA mm}^{-1}$  and  $17 \Omega \text{ mm}$  respectively, is expected. This illustrates the potential for future high-performance Ga<sub>2</sub>O<sub>3</sub> devices with deep sub-micron gate length and vertically scaled epitaxial device designs.

Benchmarking of these results in Fig. 3 shows a plot of  $G_M$  versus  $L_G$  for SAG  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFETs in this work compared to  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices reported in the literature.<sup>19–23</sup> With the exception of vertically scaled delta-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MESFETs, the  $G_M$  results are state-of-the-art and achieved with a large

gate length. Significant improvements are expected with deep sub-micron gate length scaling following the  $G_{M,ext} \approx v_{ext} C_{GS}/L_G$  relationship where  $v_{ext}$  and  $C_{GS}$  are extrinsic electron velocity and gate-source capacitance, respectively. Further reduction in access resistance can occur by optimizing implant sheet and contact resistance. For example, in our reported MOSFET, the implant  $R_{SH}$  accounts for approximately 15% of the total device resistance.

We have presented the first SAG  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFET using a refractory metal gate-first design with Si ion-implantation. The SAG process eliminates source access resistance with among the highest  $G_M$  values reported for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFETs. The data was compared with a physics-based device simulation which shows strong agreement with the measured results. Additionally, the potential of this process was shown via a device model with gate scaling applied. The SAG process will be essential for future  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device engineering to achieve high-performance, ultra-low power loss devices.

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