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$L_g = 25$ nm InGaAs/InAlAs high-electron mobility transistors with both f_T and f_{max} in excess of 700 GHz

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In this paper, we report an $L_g = 25$ nm InGaAs/InAlAs HEMT on InP substrate that delivers excellent high-frequency characteristics. The device exhibited a value of maximum transconductance (g_{m_max}) = 2.8 mS μm^{-1} at $V_{DS} = 0.8$ V and on-resistance (R_{ON}) = 279 Ω μm. At $I_D = 0.56$ mA μm^{-1} and $V_{DS} = 0.5$ V, the same device displayed an excellent combination of $f_T = 703$ GHz and $f_{max} = 820$ GHz. To the best of the authors' knowledge, this is the first demonstration of a transistor with both f_T and f_{max} over 700 GHz on any material system. © 2019 The Japan Society of Applied Physics

The development of terahertz (THz) microelectronics has yielded new areas of research and applications in the sub-millimeter-wave regime (sub-MMW; 300 GHz–3 THz), such as security/medical imaging systems, collision avoidance radars, next-generation transport communications, and wireless-local-area-networks.[1–6] In order to fully exploit the sub-MMW band, it is crucial to develop semiconductor transistor technologies with both current-gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) close to 1 THz simultaneously. In this regard, both InGaAs-based high-electron mobility transistors (HEMTs) and double-heterojunction-bipolar-transistors (DHBTs) on an InP substrate are strong candidates. To date, there have been many impressive accomplishments regarding the high-frequency response of both device technologies, delivering an f_T of 710 GHz in the InGaAs HEMTs[1], an f_T of 695 GHz in the DHBTs[2], and an f_{max} in excess of 1 THz for both.[3,4,7,8)]

Historically, a path to improve f_T in InGaAs HEMTs was to reduce the physical gate length (L_g) down to sub-30 nm, while minimizing all of the parasitic components such as series resistance and gate-fringing capacitance. On the contrary, it was found to be essential to minimize gate resistance (R_g), gate-to-drain feedback capacitance (C_{gd}) and output conductance (g_o) in order to boost f_{max} in those devices. However, this yielded significantly unbalanced high-frequency characteristics, limiting their usage. As a result, it is imperative to boost both f_T and f_{max} in a harmonious way, since this enables a wide variation of applications such as low-noise-amplifiers (LNAs) and various THz integrated circuits using a single device technology.[9–16)]

In our previous report,[17)] we demonstrated a significant potential of using an indium-rich channel design with Hall mobility close to 13 000 $cm^2 V^{-1} s^{-1}$, which resulted in outstanding DC and high-frequency characteristics with $L_g = 87$ nm InGaAs HEMTs. In this paper, we demonstrate aggressively scaled down InGaAs/InAlAs HEMTs on a 3 inch InP substrate with both f_T and f_{max} in excess of 700 GHz at the same bias condition. Key aspect was a successful reduction of L_g down to 25 nm with an optimized unit process, while mitigating short-channel effects.

The epitaxial layer structure used in this work was grown on a 3 inch semi-insulating InP substrate using metal-organic chemical-vapor-deposition. From top to bottom, the epitaxial layer structure consisted of a 30 nm thick heavily-doped multi-layer cap ($In_{0.53}Ga_{0.47}As$/ $In_{0.52}Al_{0.48}As$), a 3 nm thick InP etch-stopper, a 9 nm thick $In_{0.52}Al_{0.48}As$ barrier/spacer with Si δ-doping, a 9 nm thick indium-rich InGaAs quantum-well channel, and a 200-nm $In_{0.52}Al_{0.48}As$ buffer on the InP substrate. Details on the material growth were reported in Ref. 18. Key aspects are as follows: (i) a multi-layer cap to lower S/D ohmic contact resistance, and (ii) an $In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ (1/5/3 nm) composite-channel to improve carrier transport properties. As reported previously,[18)] the Hall mobility (μ_{n_Hall}) was measured to be 13 500 $cm^2 V^{-1} s^{-1}$ with a two-dimensional electron gas density of approximately 3×10^{12} cm^{-2} at 300 K.

The device fabrication was nearly the same as in previous report from our group.[17)] This is a two-step recess process with a gate-to-channel distance, t_{ins}, of approximately 5 nm. Source-to-drain spacing (L_{SD}) was scaled down to 0.8 μm, and a non-alloyed metal stack of Ti/Mo/Ti/Pt/Au (5/10/10/10/200 nm) was used to form S/D ohmic contact. After a gate recess process, a SiO_2-assisted T-gate with a metal stack of Pt/Ti/Pt/Au was formed. Figure 1(a) shows a cross-sectional scanning-electron-microscope image prior to the gate metallization process. Figure 1(b) shows a cross-sectional transmission-electron-microscope (TEM) image after the gate process. The inset of Fig. 1 (b) is an enlarged TEM image of the gate foot region, indicating that the gate length (L_g) was as small as 25 nm.

Figure 2(a) shows the DC output characteristics of our representative InGaAs/InAlAs HEMTs with $L_g = 25$ nm. The devices possessed a small value of $R_{ON} = 279$ Ω μm, which was due to the combination of the capping layer design and the optimized ohmic process. The contact resistance (R_C) of approximately 40 Ω μm was measured from the transmission-line-method measurement. As shown in Fig. 2(b), the same device delivered the maximum transconductance (g_{m_max}) of 2.8 mS μm^{-1} at $V_{DS} = 0.8$ V. More importantly, reasonable subthreshold characteristics, such as subthreshold-swing (S)

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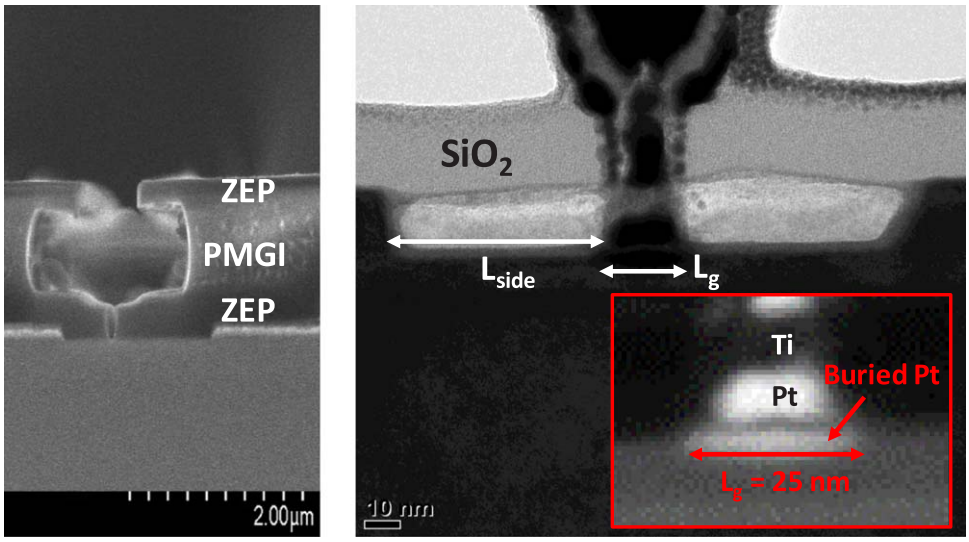

Fig. 1. (Color online) (a) Cross-sectional SEM image after a T-gate e-beam lithography process and (b) cross-sectional TEM image of a fabricated device with $L_g = 25$ nm. The inset of Fig. 1(b) is the enlarged TEM image near the gate foot region.

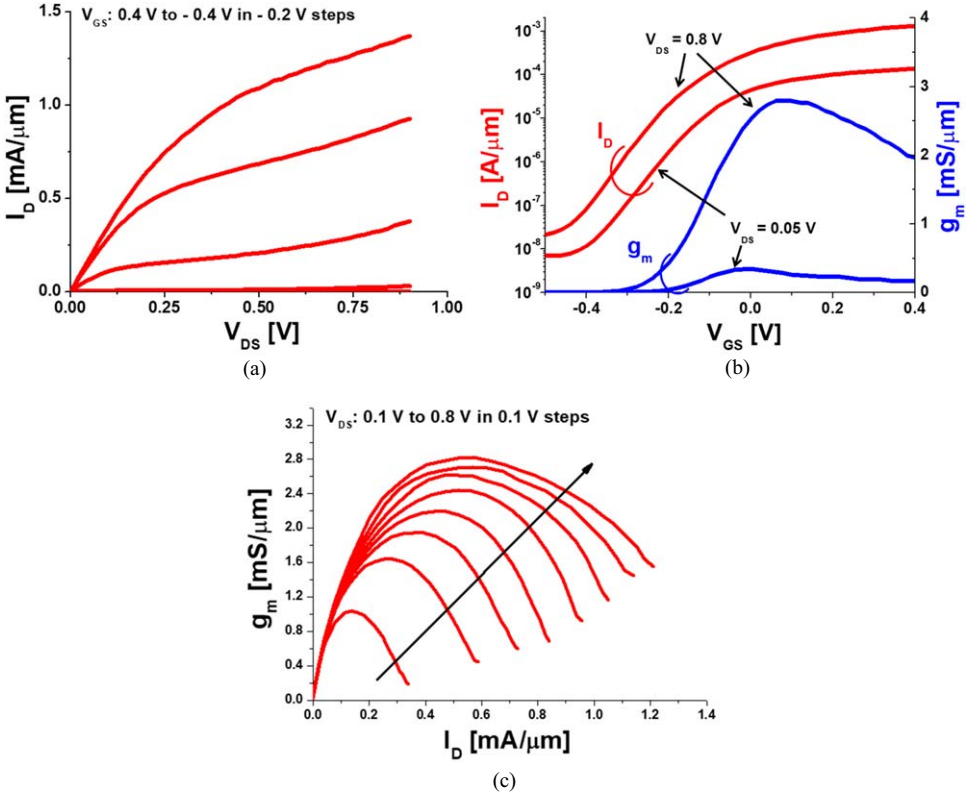

Fig. 2. (Color online) (a) Output characteristics, (b) subthreshold and transconductance (g_m) characteristics at $V_{DS} = 0.05/0.8$ V, and (c) g_m against drain current density (I_D) of the fabricated InGaAs/InAlAs HEMT with $L_g = 25$ nm with various values of V_{DS}.

of 100 mV/decade and drain-induced-barrier-lowering (DIBL) of 120 mV V^{-1}, were demonstrated even in such a short-L_g device. Figure 2(c) shows the measured g_m of the same device as a function of drain current density (I_D) for various values of V_{DS}. Notice that the device possessed a fairly broad range of high g_m over I_D, which would be highly beneficial to a diversity of applications.

The microwave characteristics of our representative InGaAs/InAlAs HEMTs were characterized from 1–50 GHz using an Agilent PNA system with off-wafer calibration. On-wafer open and short patterns were utilized to subtract pad-related capacitance and inductance components from measured scattering parameters (S-parameters).[19] Figure 3(a) plots a measured short-circuit current-gain ($|h_{21}|^2$), a Mason's unilateral gain (U_g), and a maximum stable gain (*MSG*) after de-embedding pad-related parasitic components for the device with $L_g = 25$ nm and $W_g = 2 \times 20$ μm at $V_{DS} = 0.5$ V and $V_{GS} = 0.15$ V near the peak g_m bias condition. We

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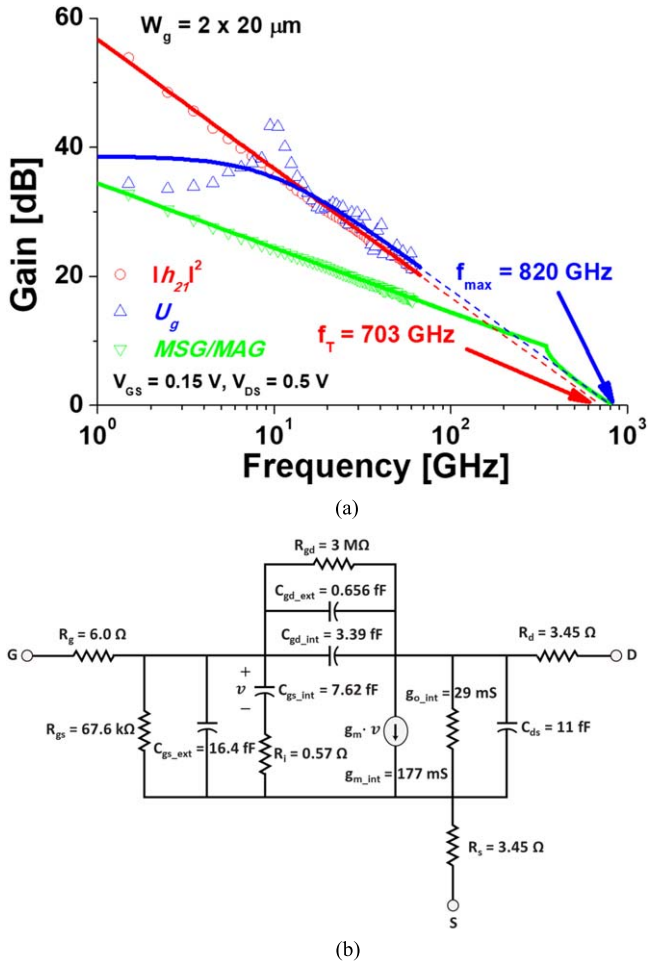

Fig. 3. (Color online) (a) Measured (symbols) and modeled RF gains (Solid lines) ($|h_{21}|^2$, U_g, *MSG and MAG*) for the $L_g = 25$ nm InGaAs/InAlAs HEMT at $V_{DS} = 0.5$ V and $V_{GS} = 0.15$ V, and (b) small-signal equivalent circuit model used in this work for the $L_g = 25$ nm InGaAs/InAlAs HEMTs at $V_{DS} = 0.5$ V and $V_{GS} = 0.15$ V. Dashed lines in Fig. 3(a) represent a projection from the modeled $|h_{21}|^2$ and U_g with −20 dB/decade using a least-squares fit.

obtained a value of $f_T = 703$ GHz by extrapolating the measured $|h_{21}|^2$ with a slope of −20 dB/decade using a least-squares fit. As shown in Fig. 3(a), the measured U_g did exhibit a sharp peaky behavior which was also seen in other groups' results.[3,7,8,20–22] As a consequence, f_{max} could not be directly extracted from the measured U_g. Instead, we constructed a small-signal model shown in Fig. 3(b), in order to estimate f_{max} accurately from a well-behaved U_g with a single-pole system.[17,23–25] It is true that there exists inconsistency between the measured and the modeled U_g especially in the low-frequency regime. This is due to the fact that our small-signal model did not take the effect of impact-ionizations in the InGaAs QW channel into account. Nevertheless, this kind of the small-signal model has provided a reasonable estimate on f_{max}, since the effect of the impact-ionizations diminishes as the measured frequency goes over 10 GHz. In this way, a value of $f_{max} = 820$ GHz was obtained, which is identical to one from the modeled MSG/MAG. It is remarkable that the device delivered both f_T and f_{max} above 700 GHz at the same bias condition.

Table I shows small-signal model parameters, together with each delay time component as defined in Ref. 24. Here, transit time (τ_t) is the carrier's transit time under the gate from the edge of the source to the edge of the drain, while extrinsic delay (τ_{ext}) is related to the parasitic charging delay due to extrinsic gate capacitances (C_{gs_ext} and C_{gd_ext}) and parasitic delay (τ_{par}) to the RC time delay due to the series resistances (R_S and R_D). Note that both extrinsic gate capacitances came mostly from the T-shaped gate structure. First of all, note that the excellent high-frequency response was due to a very high value of an intrinsic transconductance (g_{m_int}) of 4.425 mS μm^{-1} even in the device with $L_g = 25$ nm, as shown in Table I. However, it should be emphasized that the portion of τ_t constitutes only by 20%, indicating that a majority portion of the device's intrinsic high-frequency characteristics was contaminated with unwanted parasitic components, such as series resistances and extrinsic gate capacitances. Unless decreasing a majority portion of both τ_{ext} and τ_{par}, a further reduction of L_g would lead to a marginal improvement in f_T. Figure 4 plots the extracted f_T as a function of I_D for the same device with various values of V_{DS}. Consistent with the g_m against I_D in Fig. 2(c), the device yielded a wide range of I_D that provided f_T in excess of 600 GHz. At I_D of around 0.1 mA μm^{-1} which is a typical choice of the bias condition for most of LNA designs, our device already displays f_T over 400 GHz. Finally, Table II summarizes the historical evolution of HEMT technologies, together with key results (g_m, R_{ON}, f_T and f_{max}). Since GaAs pseudomorphic-HEMTs (PHEMTs) exhibited the first demonstration of both f_T and f_{max} over 100 GHz,[26] $In_xGa_{1-x}As$ HEMTs with $x > 0.53$ have provided a record combination of f_T and f_{max},[7,8,20–22,26–30] and our results represent the first demonstration of both f_T and f_{max} over 700 GHz.

In this paper, we demonstrated an $L_g = 25$ nm InGaAs/InAlAs HEMT with an outstanding combination of DC and high-frequency characteristics. At its heart, the indium-rich InGaAs channel was utilized with superior Hall mobility of 13 500 $cm^2 V^{-1} s^{-1}$ at 300 K, and the gate length (L_g) was successfully scaled down to 25 nm while maintaining the electrostatic integrity of the device. In particular, the device with $L_g = 25$ nm exhibited $R_{ON} = 279$ Ω μm, $g_m = 2.44$ ms μm^{-1}, $f_T = 703$ GHz and $f_{max} = 820$ GHz at $V_{DS} = 0.5$ V, respectively. To the best of our knowledge, this is the first demonstration of both f_T and f_{max} in excess of 700 GHz on any transistor on any material system.

Table I. Small-signal model parameters of the $L_g = 25$ nm InGaAs/InAlAs HEMT at $V_{DS} = 0.5$ V and $V_{GS} = 0.15$ V, together with delay time components.

C_{gs_ext} [fF μm^{-1}]	C_{gs_int} [fF μm^{-1}]	C_{gd_ext} [fF μm^{-1}]	C_{gd_int} [fF μm^{-1}]	C_{ds} [fF μm^{-1}]	R_i [Ω μm]	g_{m_int} [mS μm^{-1}]	g_{o_int} [mS μm^{-1}]
0.4106	0.1904	0.0848	0.0164	0.275	22.8	4.425	0.7353
R_g [Ω μm^{-1}]	R_s [Ω μm^{-1}]	R_d [Ω μm^{-1}]	τ_t [fs]	τ_{par} [fs]	τ_{ext} [fs]	f_{T_model} [GHz]	f_T [GHz]
0.15	138	138	46.7	112	66.2	707	703

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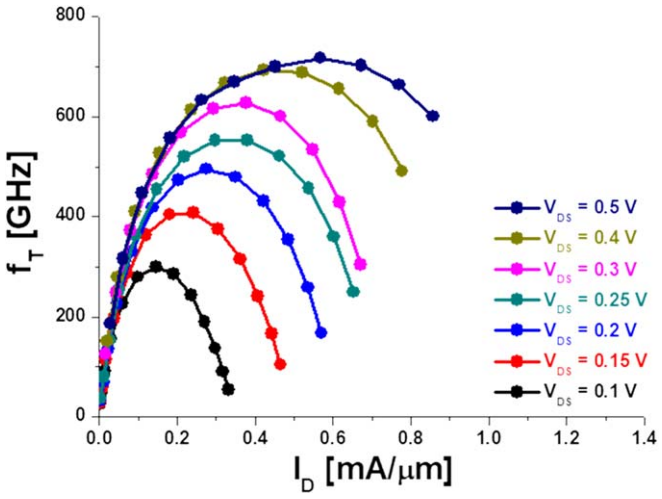

Fig. 4. (Color online) Measured f_T against I_D of the $L_g = 25$ nm InGaAs/InAlAs HEMT with various values of V_{DS}.

Table II. Summary of the historical evolution of HEMT technologies together with key device parameters.

References	Year reported	L_g [nm]	Channel/Substrate	R_{ON} [Ω μm] (V_{GS} [V])	g_{m_max} [mS μm^{-1}] (V_{DS} [V])	f_T [GHz] (V_{DS} [V])	f_{max} [GHz] (V_{DS} [V])
26	1988	150	$In_{0.25}Ga_{0.75}As/GaAs$	1428 (0.8)	0.65 (1.0)	152 (1.0)	230 (2.0)
27	1992	50	$In_{0.8}Ga_{0.2}As/InP$	625 (0.2)	1.69 (0.8)	343 (0.8)	250 (0.8)
28	1994	100	$In_{0.8}Ga_{0.2}As/InP$	N/A	1.55 (1.0)	305 (1.0)	340 (1.0)
20	2001	45	$In_{0.7}Ga_{0.3}As/InP$	1300 (0.4)	1.0 (N/A)	400 (1.0)	469 (1.0)
21	2008	50	InAs/InP	750 (0.4)	1.62 (0.6)	557 (0.6)	718 (0.6)
22	2008	30	InAs/InP	600 (0.5)	1.83 (0.5)	601 (0.5)	609 (0.5)
29, 30	2013	25	InAs/InP	270 (0.4)	3.05 (1.0)	610 (1.2)	1500 (1.2)
1	2013	60	InAs/InP	400 (0.3)	2.11 (0.5)	710 (0.5)	478 (0.5)
7, 8	2017	75	$In_{0.7}Ga_{0.3}As/InP$ (Asymmetric recess)	500 (0.2)	1.9 (1.0)	250 (1.0)	1300 (1.0)
This work	2019	25	$In_{0.8}Ga_{0.2}As/InP$	279 (0.4)	2.8 (0.8)	703 (0.5)	820 (0.5)

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