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PROGRESS REVIEW

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Mask innovations on the eve of high NA EUV lithography

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We are on the eve of the next big step in lithography technology with the introduction of high numerical aperture EUV. The change from NA 0.33–0.55 in EUV lithography is an increase of 67%, which is the largest jump in the last decades, and puts tight requirements on focus and edge placement. Moreover, the lithography system has changed from fully isomorphic, i.e. same demagnification in all directions, to an anamorphic system, i.e. the demagnification in scan direction has doubled with respect to the slit direction. At imec we are fostering the ecosystem surrounding the lithography tool. In this paper we focus on the imaging and mask innovations supporting the EUV ecosystem, which are categorized into four areas: novel absorber masks, stitching, mask variability, and innovative imaging solutions. The current drivers of IC manufacturers implementing (high NA) EUV lithography (EUVL) are reduction of the EUV exposure dose and decrease in wafer stochastics. We discuss how these four areas have the potential to deliver in EUVL an increase in productivity, an improvement in the process window and a reduction in stochasticity at wafer level. © 2024 The Japan Society of Applied Physics

1. Introduction

Moore's law of increasing the number of transistors on a chip has governed our industry for decades. At imec we envision that Moore's law will not stop and we will be able to extend the roadmap for future technology generations.[1] We will continue to shrink through a combination of techniques: we will achieve this by dimensional scaling, by the introduction of new devices and materials, and by using more and more the third dimension with context aware interconnect. In this paper we zoom in on the dimensional scaling, which is enabled by the lithography roadmap, driven by the resolution equation Eq. (1), where the smallest pitch ($P_{\min}$) can be reduced by reducing the lithography wavelength (λ), increasing the numerical aperture (NA), and reducing the processing factor (k_1).

$$\frac{P_{\min}}{2} = k_1 \frac{\lambda}{\mathrm{NA}} \quad (1)$$

Per lithography wavelength the lithography process complexity increases until the point where it is beneficial to switch to a smaller lithography wavelength. Now we are at the point where within the EUV wavelength the progression of Moore's law requires an increase in the numerical aperture to keep the lithography complexity attainable. The change from NA 0.33–0.55 is an increase of 67% and ASML started shipment of the first NA0.55 system to a chipmaker at the end of 2023. At imec we are fostering the ecosystem surrounding the lithography tool.

Patterning innovations on the eve of High NA EUV lithography are situated in three areas of the ecosystem in which imec is advancing with innovative solutions.
- Mask and illumination: the interplay between mask and illuminator is responsible for the aerial image at wafer level.[2]
- Materials and processes at wafer level influence the final pattern.
- Dedicated metrology and inspection are needed to characterize these final wafer patterns.

In this paper we give an overview of the imaging and mask innovations supporting the EUV ecosystem. In Sect. 2 we discuss the EUVL potential of novel absorber masks. Section 3 provides details on enabling stitching towards High NA EUVL. Mask variability impact on wafer variability is assessed in Sect. 4. In Sect. 5 innovative imaging solutions are presented to push patterning by decreasing k_1 and increasing NA. Section 6 summarizes this work and provides an outlook.

2. Novel absorber mask

In the past years, masks with low-n absorber have been evaluated for their dose and contrast benefit.[3–6] Figure 1(a) plots the experimental exposure latitude through pitch for equal lines/spaces (LS) at NA0.33 of a low-n mask versus a Ta-based reference mask with their respective optimized illumination pupil for pitch 28 nm LS. The exposure dose at each pitch was selected to print equal LS on mask to equal LS on wafer, as shown in Fig. 1(b). Even at a lower dose-to-size the low-n mask results in higher exposure latitude over the shown pitch range compared to the Ta-based reference mask. In addition, the higher contrast (or simulated normalized image log slope, NILS) achieved with the low-n mask leads to lower unbiased line-edge roughness (uLER) measured on wafer for pitch 28 nm LS compared to the Ta-based reference mask and this for different illumination pupils [see Fig. 1(c)].

In our earlier work we reported on imaging with low-n mask requiring mask 3D (M3D) mitigation in case of patterning pitch 28 nm logic metal design.[3,4,6] We observe large best focus shifts through LS pitch with the low-n mask, which can be mitigated by insertion of sub-resolution assist features (SRAF), as presented in Fig. 2(a). However, low-n mask imaging is sensitive to SRAF printability in defocus as shown in Ref. 3. Moreover, within reasonable mask bias ranges through pitch for the low-n mask, it was demonstrated that retargeting of the wafer critical dimension (CD) for the more isolated pitches is insufficient to compensate the best focus shifts.[4] Another M3D effect is the CD asymmetry through focus for horizontal two-bar features. The slope of the CD difference of upper and lower trench through focus is a measure of the phase mismatch with vacuum. Figure 2(b)

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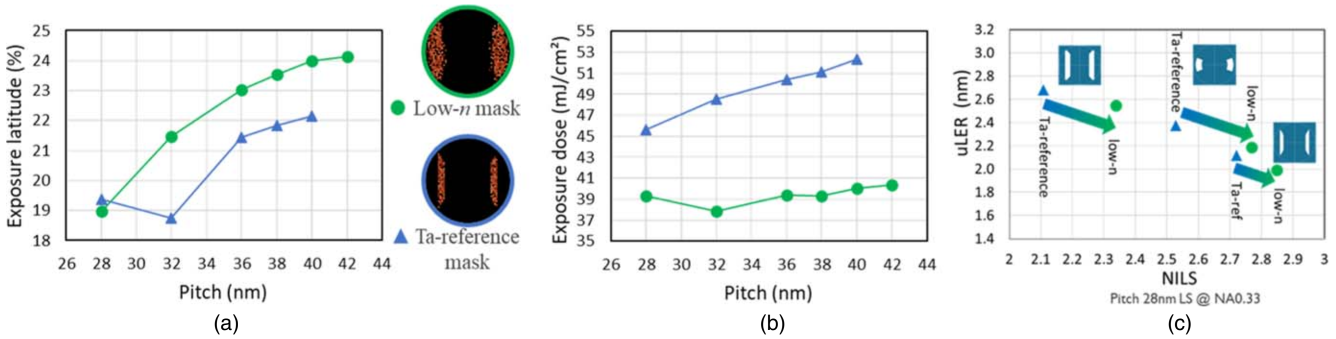

Fig. 1. (a) Experimental exposure latitude (in %) through pitch equal LS for low-*n* and Ta-based absorber mask exposed at NA0.33 with the corresponding illumination pupil. Target CD on wafer is half-pitch CD for all depicted pitches. Exposure latitude is calculated based on $+/-10$ target CD variation.[4] (b) Corresponding exposure dose through pitch to print equal LS on mask to equal LS on wafer. (c) Measured unbiased line edge roughness for pitch 28 nm LS exposed at NA0.33 using the three shown illumination pupils and the corresponding simulated normalized image log slope (NILS) between low-*n* and Ta-based absorber mask.[5]

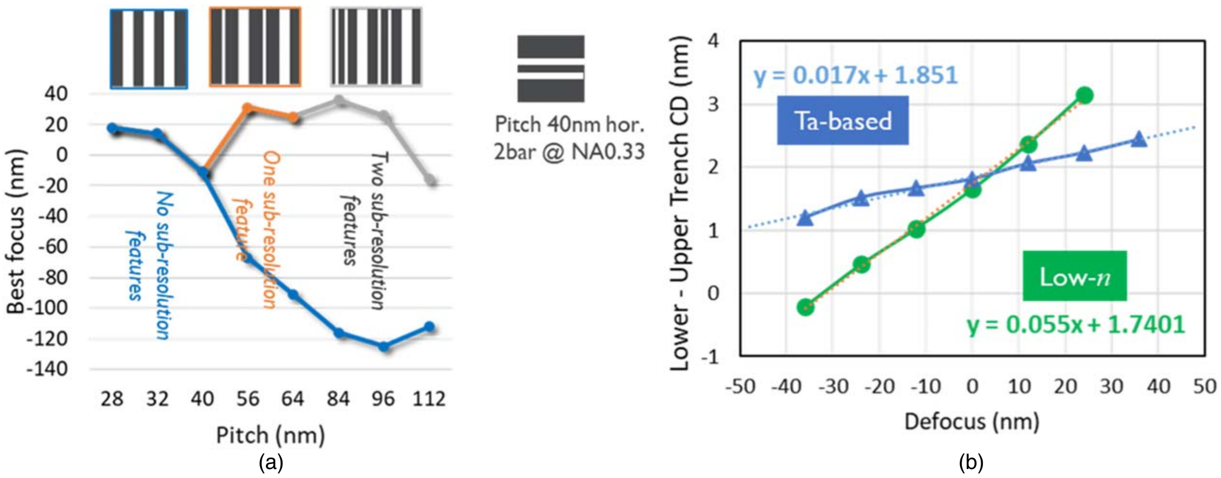

Fig. 2. (a) Measured best focus through vertical LS pitch for low-*n* mask using no SRAF, one single and double SRAF.[4] (b) Measured CD asymmetry through focus for a horizontal 40 nm pitch two-bar for low-*n* and Ta-based mask.[6]

shows a stronger slope for the low-*n* than for the Ta-based mask.

To find the sweet spot in mask absorber material for High NA EUVL we perform rigorous imaging simulations with following ingredients: EUV optical material properties *n*&*k* and thickness covering the mask absorber space, designs representative for the logic and DRAM nodes from N2 down to A5 technology node, and their optimized illumination pupils. We evaluate the following imaging metrics: high NILS for reduced wafer stochasticity, low exposure dose for increased throughput, small best focus shifts between the technology LS pitch and twice this pitch for maximized overlapping process window. Figure 3 summarizes the simulation results for horizontal LS per technology pitch at NA 0.55 and five different mask absorber flavors. Each technology pitch is targeted to half-pitch wafer CD using its respective optimized leaf shape dipole illumination. Figure 3(b) shows that the low-*n* masks can achieve larger maximum NILS for all technology nodes by using smaller mask absorber width bias (see sub-plot). However, around 20 nm pitch the NILS for the low-*n*, low-*k* mask drops strongly, while the high-*k* mask improves NILS compared to the Ta-based reference mask. Figure 3(c) plots the dose-to-size relative to the Ta-based reference mask required to achieve the same NILS per technology pitch for the novel absorber mask as for the Ta-based reference mask. The NILS matching per technology pitch is realized by mask absorber width biasing as represented in the sub-plot. In this way we can look for the potential of exposure dose reduction of different absorber masks at the same NILS. Also for exposure dose we see the benefit for low-*n* masks. Looking at the M3D effect of best focus shift between the technology pitch and twice this pitch in Figs. 3(d)–3(e), we note for the bright field mask, i.e. when the mask absorber width is much smaller than the mask space width for twice the technology pitch, only small best focus variations, while huge best focus shifts are predicted for dark field masks, i.e. when the mask space width is much smaller than the mask absorber width for twice the technology pitch. In the latter case, the high-*k* mask exhibits the smallest best focus variation compared to the low-n mask flavors. These initial simulation results indicate that horizontal LS pitch 20 nm seems an inflection point for mask type selection: the high reflectivity mask loses steam, while the low reflectivity masks gain in power. This is in line with our novel absorber engineering where we propose absorber material combinations in this EUV low reflectivity area.[7–9]

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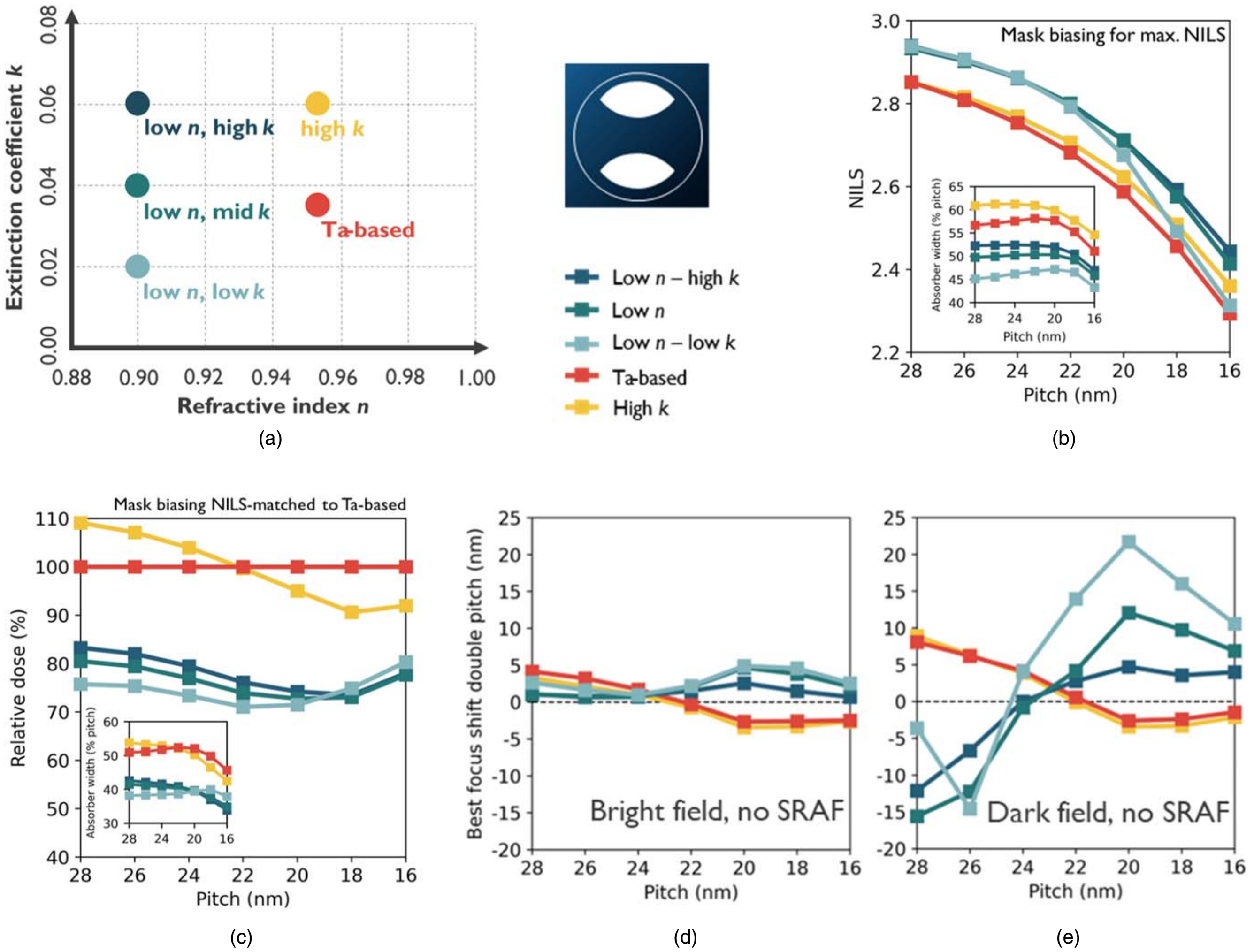

Fig. 3. (a) Selected EUV optical properties of absorber *n&k*, horizontal leaf shape dipole illumination at NA 0.55, (b) Maximum NILS per technology LS pitch (horizontal) and mask type. (c) Dose-to-size relative to the Ta-based reference mask per technology LS pitch, (d) best focus shift between the technology pitch and twice this pitch for bright field and (e) dark field mask without SRAF per technology LS pitch (horizontal) and mask type.

3. Stitching

High NA EUV anamorphic imaging implies in-die stitching where two masks will need to be exposed to form one wafer die. One approach is to avoid critical designs around the stitching line,[10] which is a design solution with no critical patterns stitched, but a design change at system level is required to move IP blocks around. To minimize the zone around the stitching line without mask patterns, the registration of mask patterns close to the mask edge needs to be well controlled. To achieve this the mask black border stress relaxation needs to be minimized. We measured on wafer less than 1.5 nm shift in contact hole placement over a distance from 5 to 10 μm to the black border on this specific mask, as displayed in Fig. 4. Masks with an adequate mask making process that does not impact the pattern placement at the black border edge are available.

Another approach is to enable at-resolution stitching, where the combined exposures of both masks will lead to continuous LS at critical pitch running over the stitching area. This process solution has no area penalty, but additional sources of process variations need to be controlled. Imec together with ASML has experimentally demonstrated the stitching feasibility at NA0.33.[11,12]

The main interactions in the stitching area are specified in Fig. 5. The zone where the black border and absorber of one mask overlap with the trench on the other mask will cause wafer CD changes. Optical proximity correction (OPC) is required on the mask trench under the absorber of the other mask to suppress the absorber reflectivity. In case of low-*n* mask additional sub-resolution grating on the other mask is needed for background intensity reduction.[12] Additionally, the wafer SEM image and CD plot in Fig. 5 show the transition zone where the wafer CD gradually changes over a range of 50 nm at wafer. This transition zone on wafer is determined by the mask absorber to black border profile and position through slit. State-of-the-art control of this mask profile will be a key enabler for the success of OPC in the stitching area. Secondly on Fig. 5 the zone of aerial image interaction between the two trench ends on both masks is indicated and a wafer SEM image of the resulting stitched trenches is included. The close-to-optimum stitching was found by varying the tip overlap in the scanner exposure recipe by means of the image field shift in the *Y* direction. These wafer results demonstrate the stitching feasibility experimentally at NA 0.33 on the EUV exposure tool (NXE:3400B) at imec. To further optimize this stitching result a dedicated OPC strategy at the stitch needs to be developed, as well as continued mask quality and resolution of the mask line ends at the mask edge.

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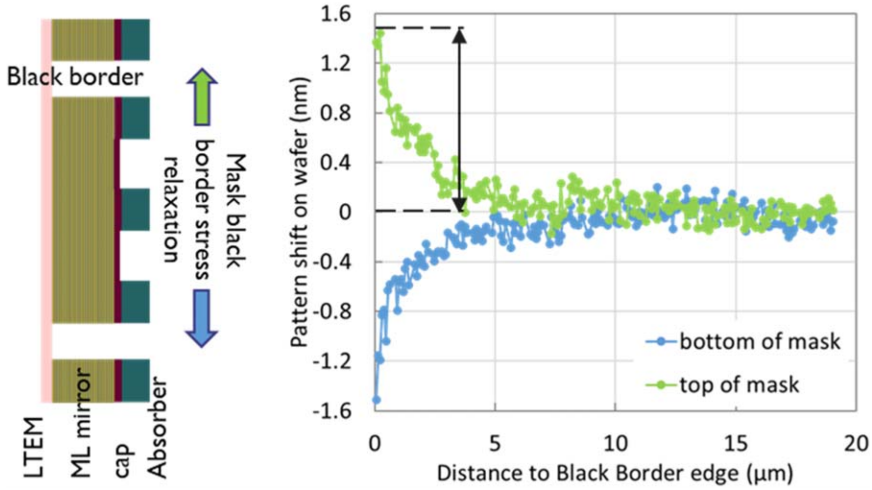

Fig. 4. Schematic mask cross section (not to scale) showing the absorber pattern on the cap and multilayer (ML) mirror and the etched black border on a low thermal expansion material (LTEM) substrate. Mask black border stress relaxation, indicated by the arrows in the mask schematic, is measured as pattern shift on wafer as a function of distance to the mask black border edge.[10].

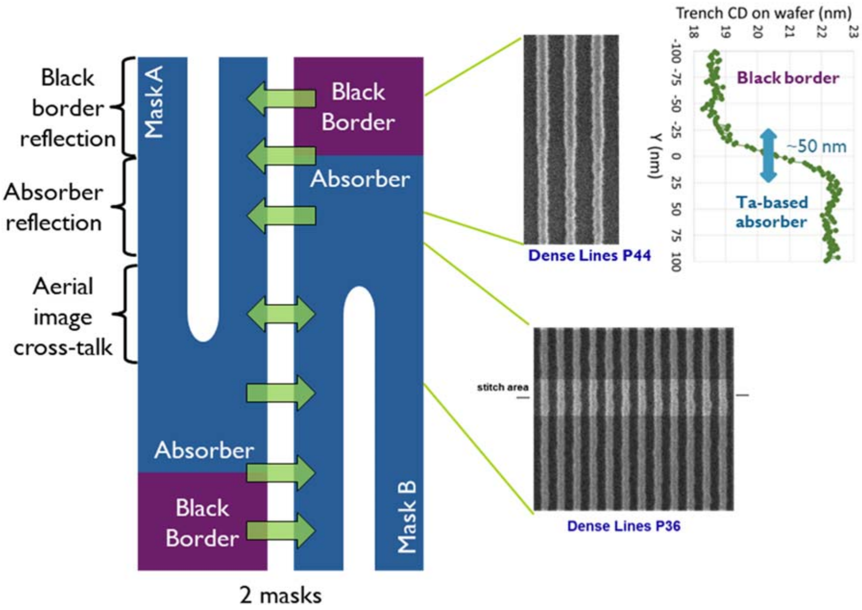

Fig. 5. Left: concept of the main interactions in stitching area in the case of vertical trenches stitching.[11] Upper right: Experimental data of absorber/black border transition obtained on NXE:3400B on pitch 44 nm LS.[11] Bottom right: stitching of pitch 36 nm LS on NXE:3400B using a dark field mask (no specific OPC), chemically amplified resist and manually optimized tip overlap in exposure recipe.[12]

4. Mask variability

Mask local variability impacts the wafer local variability through mask local CD uniformities, mask pattern fidelity and mask stack uniformity.[13] The general understanding is that the background intensity in the diffraction spectrum caused by this mask local variability and transferred through the lens depends on the illumination pupil.[14]

We touch upon two cases of mask local variability and their contribution to wafer local variability at NA0.33 and provide some outlook to its impact at NA0.55 imaging.

Starting from the mask local CD variability, a detailed study was reported in Ref. 15 on its transfer to wafer systematic local CD uniformity (LCDU) or local mask error enhancement factor (MEEF) using programmed mask CD variability on a pitch 40 nm hexagonal contact hole (CH) array (see Fig. 6 left) and its dependence on the illumination condition. The diffraction pupil in Fig. 6 originating from an on-axis single point source on the mask CH array combines the diffraction peaks from regular CH array (red dots) with the background diffraction intensity from the mask local CD variability. Depending on the illumination pupil used, low or high σ in Fig. 6, this diffraction pupil is transferred to a different extent on to the wafer. This can be measured by the wafer systematic LCDU, which is comprised of the mask LCDU enhanced by the local MEEF. The local MEEF represents the slope of the individual wafer CH CDs versus the corresponding measured mask CDs in the array. It was found in experiments and confirmed by simulation that local MEEF gives a stronger response to the measured mask variability for a low-σ pupil compared to a high-σ pupil (see Fig. 6).[15,16] Therefore, local MEEF should be considered when optimizing illumination pupils.

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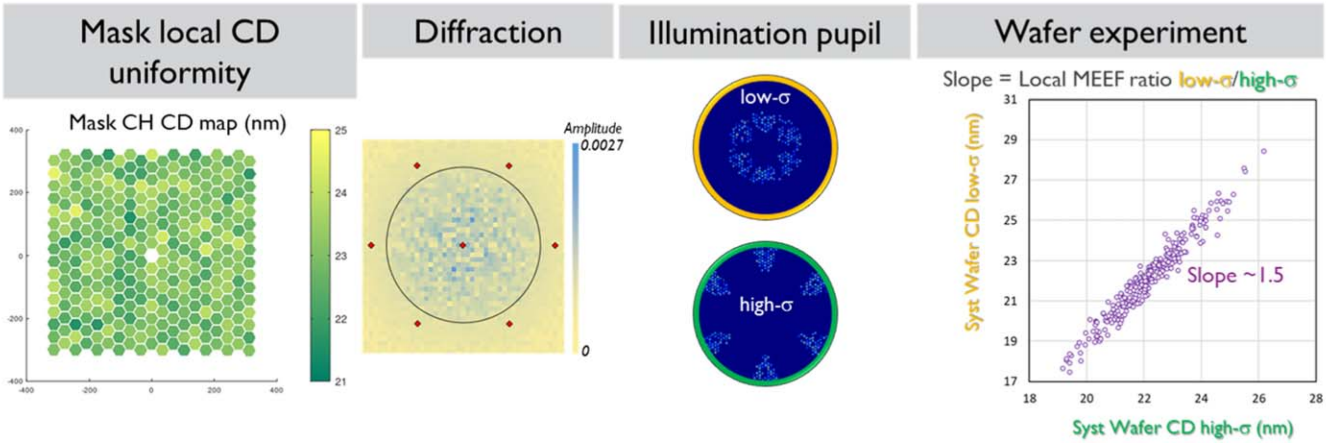

Fig. 6. Schematic flow of how mask local CD variability transfers from diffraction background and in combination with the illumination pupil to systematic wafer CD and local MEEF ratio depending on the illumination pupils.[15]

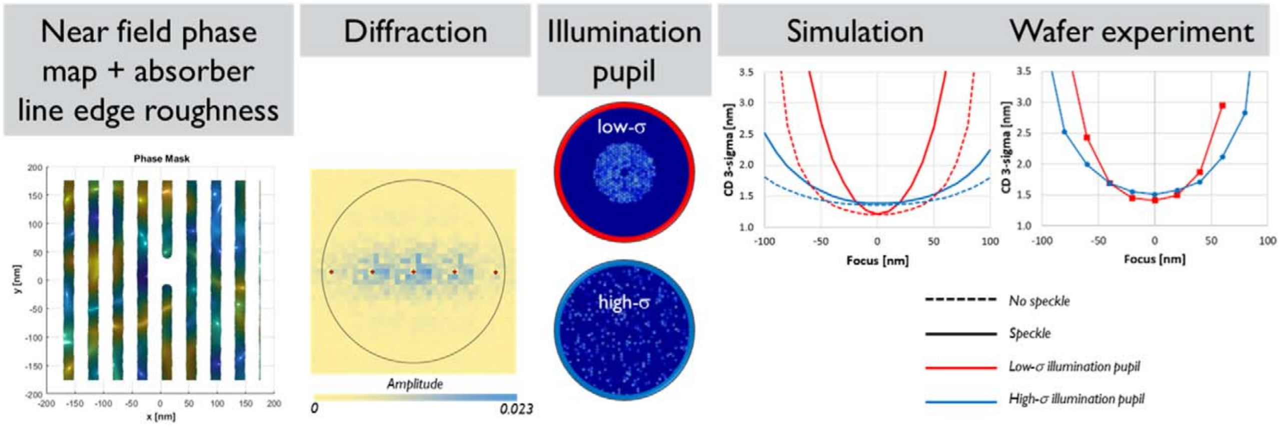

Fig. 7. Schematic flow of how mask local phase variability and mask line edge roughness transfer from diffraction background and in combination with the illumination pupil to wafer CD and edge placement errors in defocus.[17]

The second case of mask local variability considers phase variability in the diffraction spectrum induced by roughness in the mask stack, so-called speckle effect, in combination with absorber line edge roughness on a pitch 44 nm LS pattern.[17] The diffraction pupil in Fig. 7 originating from an on-axis single point source on the mask LS grating consists of the diffraction peaks from the regular LS pitch (red dots) and the background diffraction intensity from the mask speckle and absorber line edge roughness. The impact of the mask roughness on the 3-sigma standard deviation of the wafer CD is simulated through focus for two different illumination pupils (low and high σ in Fig. 7). It was found that the wafer CD variability in defocus gives a stronger response to the speckle versus no speckle for a low-σ pupil compared to a high-σ pupil. This sensitivity to the illumination pupil is confirmed by the wafer experiment, where speckle is always present on the actual mask.

At high NA EUV lithography the same level of speckle on the mask leads to much larger wafer variability in defocus.[17] Figure 8 compares the simulated local placement error through focus at NA0.33 and NA0.55 at the same k_1 by scaling the CH pattern for the given illumination pupil. Therefore, mask roughness variability is expected to become a larger part of the overall variability budget on the wafer.

The central obscuration in the projection optics of the High NA EUV system can be used to reduce the transfer of the

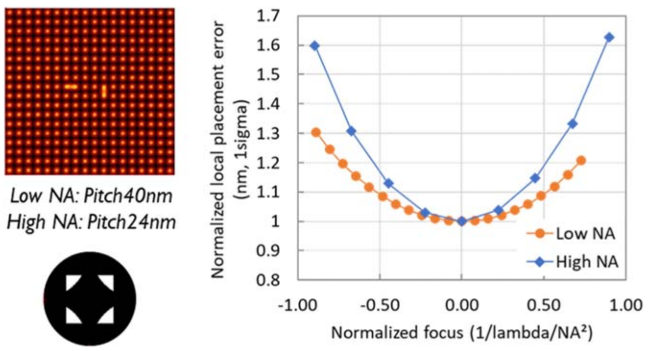

Fig. 8. Simulated local placement error through focus on a CH pattern at same k_1 at NA0.33 (low NA) and at NA0.55 (high NA) in the presence of same speckle level on mask.

mask variability. For a hexapole illumination pupil the integrated transmitted background intensity in the diffraction spectrum as a function of the sigma center of the hexapoles is shown in Fig. 9. As discussed, the higher sigma source points transmit less background intensity (about half) through the lens than the low sigma source points.[16] Adding the typical central obscuration of 0.2 sigma (i.e. 4% area) shows that this obscuration blocks some background intensity (about 8%) for the low-σ pupils. Therefore, at NA0.55 the low-σ pupils have a tradeoff between NILS and transmitted background intensity (impacting wafer LCDU).

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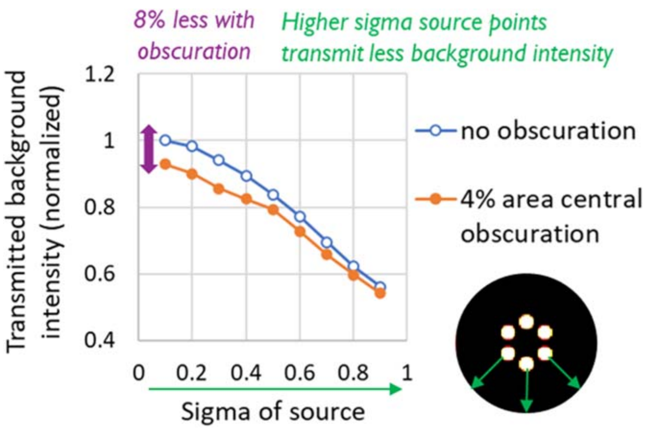

Fig. 9. Integrated transmitted background intensity for a hexapole illumination pupil as a function of the hexapole's sigma in case of no obscuration versus 4% area central obscuration in the projection optics.[16]

5. Innovative imaging solutions

Through innovative imaging solutions we push the resolution patterning to smaller technology nodes with the available NA by correcting the root causes of image degradation at the smallest dimensions. The printability of challenging structures will be enhanced by considering mask tone switch from dark field to bright field, injection of controlled aberrations in the illumination, careful selection of the illumination pixels, and smart mask design corrections. This co-optimization of mask stack, mask design, source (or illumination pupil) goes hand in hand with optimization of the wafer stack.

Figure 10 illustrates the different stages for a logic metal direct print at NA0.33. Starting from the historically dark field mask tone in combination with positive tone development (PTD), chemically amplified resist (CAR) on wafer the source-mask optimization (SMO) software proposes for a pitch 32 nm metal logic clip a four-leaf illumination pupil to provide the largest overlapping process window for all features in the clip (LS dense and semi-dense, tip-to-tips). However, Franke et al. showed how M3D effects (image fading, best focus variation through pitch and telecentricity errors) can be compensated by an illumination pupil with controlled aberration injection.[18] For the specific pitch 32 nm metal logic clip a dipole illumination with injected Zernike 6 aberration (see Fig. 10) outperformed the conventional SMO pupil and resulted in an alignment of best focus through pitch, an increase in exposure latitude through pitch and enhanced tip-to-tip printability.

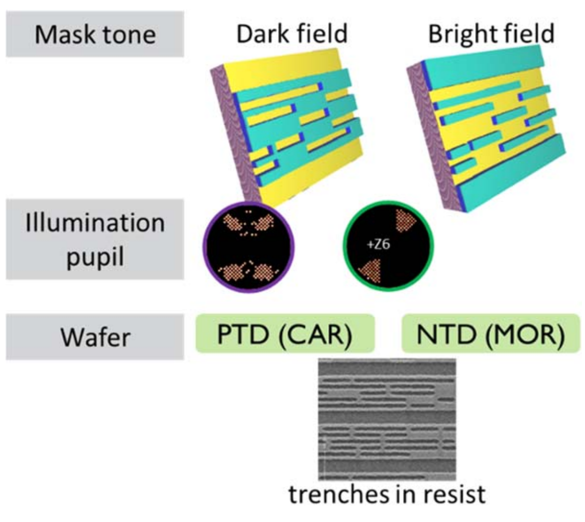

Fig. 10. Illustration of the co-optimization of mask tone, illumination pupil and wafer resist tone to print trenches in resist for a logic metal clip.

Combining such optimized illumination pupil with bright field mask tone and negative tone development (NTD), metal-oxide resist (MOR) on wafer has been studied in Ref. 19. For logic metal designs the overall layout density for dark field or bright field mask tone is comparable. They conclude that bright field imaging in combination with a fading corrected illumination pupil has much lower dose sensitivity for all LS pitches, prints even smaller tip-to-tip and has higher optical contrast at small CD at iso LS pitch.

In earlier work it has been introduced that a multiple monopole exposure scheme can alleviate M3D effects by removing image shifts from a single exposure with a multipole illumination pupil.[20] Figure 11 Left illustrates the principle for a LS grating: originally exposed by a dipole illumination pupil the aerial image would suffer from fading due to the image shifts from each pole of the dipole. In the multiple monopole exposure scheme the LS grating is exposed first with the right pole of the original dipole at half the exposure dose, then in the second exposure also at half the exposure dose the left pole is using together with a wafer stage shift to compensate for the image shift. The resulting aerial image of the LS grating is constructed by symmetric imagery and thus shows an improved contrast compared to the single dipole exposure.

Significant imaging improvements have been experimentally demonstrated at NA0.33 by using a multiple monopole exposure scheme, including increased exposure latitude (due to recovered aerial image contrast), reduced best focus shifts through pitch, smaller line width roughness, smaller tip-to-tip patterning and reduced micro-bridging defects in the stochastic cliffs for narrow trenches.[21] Figure 11 right exemplifies the latter by plotting the detected microbridge defect levels versus the trench CD of a pitch 50 nm LS grating in case of a dipole exposure and a split pole exposure scheme. At the same wafer trench CD, the split pole exposure scheme reduces the micro-bridging defects by 6X. The other way around, this split pole exposure scheme prints smaller wafer trench CDs at a given defect density.

Together with the search for novel absorber masks, the above cited techniques offer alternative ways to mitigate M3D effects in EUV lithography.

By simulations we also explore the imaging feasibility at NA beyond 0.55, which is called Hyper NA EUVL, to ensure scaling into the future of the technology roadmap. The main candidate for the NA value, which we will discuss here, is 0.75 with the same anamorphic magnification and similar central obscuration as NA0.55. We also use the current Mo/Si multilayer mirror of the EUV mask, since it was found adequate to support NA0.75 performance.

As a starting point of the imaging feasibility, we evaluated how the image contrast deals with the enlarged angles at mask side and the polarization state of the incoming EUV light.[22] In case of pitch 10 nm LS a screening through the EUV *n*&*k* space for potential mask absorbers pointed out that the novel mask absorber (low-*n*, high-*k*) under development for NA0.55 are suitable for Hyper NA (see Fig. 12 Left).[22] Until NA0.55 the incoming EUV light is unpolarized, but with the advent of Hyper NA we need to consider the

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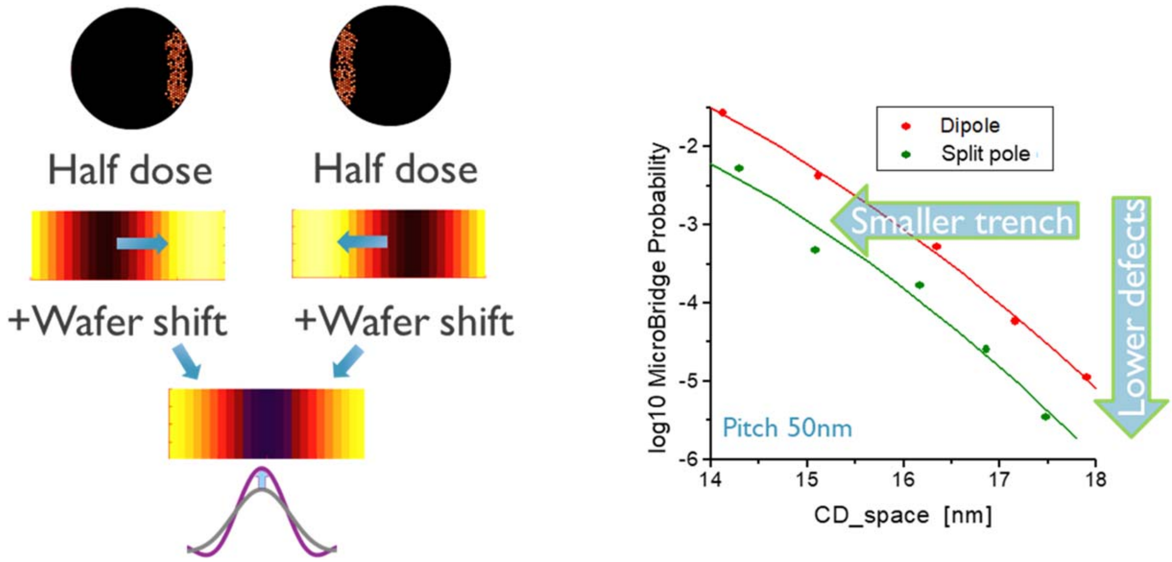
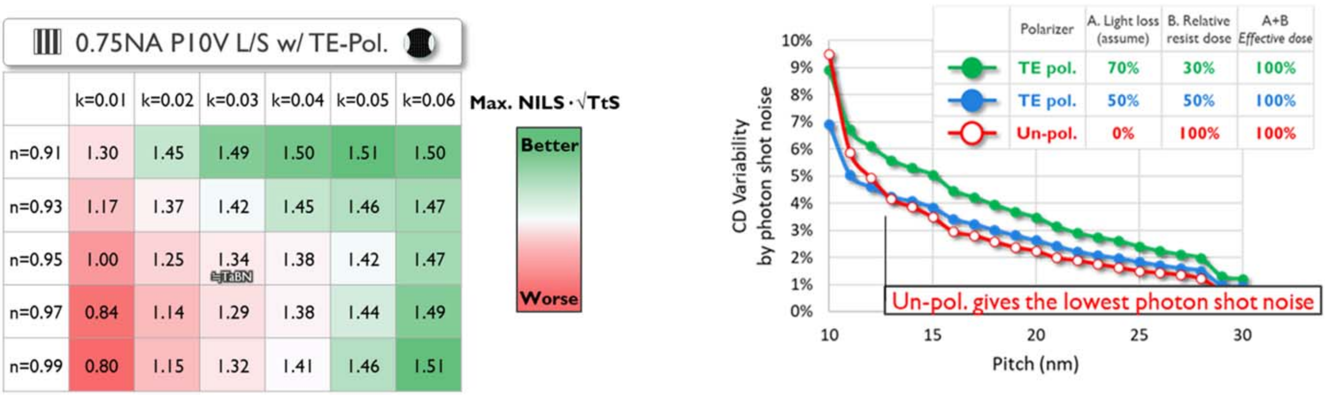


Fig. 11. Left: principle of split pole exposure and the resulting increased aerial image contrast. Right: Stochastic cliff data for pitch 50 nm LS.[21]



	k=0.01	k=0.02	k=0.03	k=0.04	k=0.05	k=0.06
n=0.91	1.30	1.45	1.49	1.50	1.51	1.50
n=0.93	1.17	1.37	1.42	1.45	1.46	1.47
n=0.95	1.00	1.25	1.34	1.38	1.42	1.47
n=0.97	0.84	1.14	1.29	1.38	1.44	1.49
n=0.99	0.80	1.15	1.32	1.41	1.46	1.51

Polarizer	A. Light loss (assume)	B. Relative resist dose	A+B Effective dose
TE pol.	70%	30%	100%
TE pol.	50%	50%	100%
Un-pol.	0%	100%	100%

Fig. 12. Left: Heatmap table of mask absorber EUV *n*&*k* space for maximum NILS.sqrt(threshold-to-size) of pitch 10 nm LS at NA0.75 using TE polarized illumination.[22] Right: CD variability by photon shot noise as a function of pitch with and without polarization at a constant effective dose at NA0.75.[22]

potential polarization impact, where the TM-polarized light will degrade the final image contrast even more due to the larger angles at mask side. In contrast to DUV lithography, the refractive index of the resist is close to 1, which does not reduce the angles between the beams inside the resist. However, polarizing the incoming light by double reflection implies light loss by 50%–70%. For the same effective dose or same throughput, only 50%–30% will reach the wafer in case of TE polarization compared to 100% dose at wafer in case of unpolarized illumination. In case of TE polarization, the consequent increased photon shot noise, will counteract the NILS gain. In Fig. 12 Right, based on a simplified stochastic aerial image model, the unpolarized illumination gives the lowest photon shot noise down to pitch 13–11 nm LS.[22] So, even if polarization control could provide significant NILS gain for LS, it should be balanced with the throughput loss and increased CD variability.[23]

6. Conclusions

In this paper we presented an overview of the recent status of mask innovations on the eve of High NA EUV lithography, which are categorized into four areas.

- Novel absorber masks: low-*n* masks offer dose reduction and contrast gain but need M3D mitigation. We looked ahead on the single exposure technology roadmap with rigorous simulation capability and foresee a further shift in mask absorber options (towards high EUV extinction) to fully exploit the High NA and even Hyper NA EUVL prospect.
- Enabling stitching towards High NA EUVL: stitching feasibility is demonstrated experimentally at NA0.33. OPC is a key control mechanism at the stitching zone and should be supported by the required mask quality at the mask edge.
- Mask variability causes background intensity in the diffraction spectrum. The illumination pupil shape and NA determine which part of the diffraction background is transferred to wafer.
- Innovative imaging solutions: M3D effects at NA0.55 can be mitigated by smart choice of illumination pupil in combination with mask tone and type. The exploration of the Hyper NA EUVL space at NA0.75 shows evolutionary imaging and mask trends.

Through these forecasts we can prepare the industry well in advance to enable innovations in the field of masks, scanner, materials, and metrologies.

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