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Improvement of self-heating effect in Ge vertically stacked GAA nanowire pMOSFET by utilizing Al_2O_3 for high-performance logic device and electrical/thermal co-design

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For improving self-heating effect (SHE) in Ge vertically stacked gate-all-around (GAA) nanowire (NW) p-type metal-oxide-semiconductor field-effect transistor (pMOSFET), aluminum oxide (Al_2O_3, alumina) is utilized for gate dielectric layer. From the high thermal conductivity of Al_2O_3, SHE is significantly improved. In order to validate the proposed device structure, technology computer-aided design simulation is performed through Synopsys Sentaurus three-dimensional tool. As a result, when Al_2O_3 is incorporated in Ge vertically stacked GAA NW pMOSFET, SHE can be remarkably improved from 534 to 419 K. In addition, the method of simultaneously accomplishing improvement of SHE and low gate leakage current (I_{gate}) have been specifically investigated and proposed with numerous simulation data. © 2021 The Japan Society of Applied Physics

1. Introduction

Recently, with the advent of the fifth-generation (5G) era and the big data era, the amount of data to be processed has exponentially increased and the demand for high-performance (HP) devices has also increased every year.[1–4)] In accordance with these technological trends, lots of candidates for next-generation semiconductor devices have been broadly researched to replace conventional silicon (Si) based semiconductor devices, by utilizing various new materials such as germanium (Ge), indium phosphide (InP), gallium arsenide (GaAs), and indium arsenide (InAs).[5–8)]

Among these candidates for channel material, Ge material has attracted significant attention as a practicable candidate to replace conventional Si-based p-type metal-oxide-semiconductor field-effect transistor (pMOSFET) due to its excellent intrinsic hole mobility. Specifically, Ge has outstanding intrinsic hole mobility about 1900 cm^2 $(V \times s)^{-1}$ compared to the others [Si: 450, InP: 200, GaAs: 400, InAs: 500 cm^2 $(V \times s)^{-1}$].[9)] Therefore, it is widely accepted that Ge material can be a viable solution for the future semiconductor industry due to the possibility of achieving high on-current (I_{on}) from high intrinsic hole mobility of Ge.[10–12)]

In addition, since the key to the next-generation HP logic device is how to achieve high I_{on}, the vertically stacked channel structure has been expected as the most promising next-generation HP logic device structure.[13–15)] For these reasons, the International Roadmap for Devices and System (IRDS) Society has predicted a Ge vertically stacked gate-all-around (GAA) nanowire (NW) pMOSFET as an optional logic device structure in 2024–2029 and mainstream structure for the logic device after 2030.[16)] Therefore, it has been widely accepted that Ge vertically stacked GAA NW pMOSFET will be the decisive logic device in about 10 years, and considerable research has been conducted.[17–19)]

Unfortunately, there is a very important factor that will hinder the commercialization of Ge vertically stacked GAA NW pMOSFET, namely "self-heating effect (SHE)".[20,21)] Specifically, considerable current flows from the high intrinsic mobility of Ge and its vertically stacked channel structure, and much more heat is consequently generated.[22)] What's worse, since the channel of the conventional Ge vertically stacked GAA NW pMOSFET is completely wrapped with hafnium oxide (HfO_2) that has lower conductivity of 0.35 W $(K \times m)^{-1}$] at sub-10 nm thickness,[23)] it is hard to dissipate the heat generated by the current.[24–26)] For these reasons, it is well-known fact that GAA structure is inferior to FinFET structure in terms of heat dissipation, namely SHE.[27,28)]

Given that the effective hole mobility decreases as the lattice temperature of the channel increases due to SHE,[29)] conventional Ge vertically stacked GAA NW pMOSFET is difficult to fully utilize both advantages of the high intrinsic hole mobility from Ge and the high I_{on} from its vertically stacked channel structure. In addition, this SHE also causes lots of reliability issues such as metallization lifetimes of the circuit,[30)] hot-carrier induced degradation,[31)] negative-bias temperature instability,[32)] and decrease of threshold voltage (V_{TH}) as well. Therefore, it is essential to improve the SHE issues for accomplishing successful next-generation HP devices.

To address these issues, omega-shaped-gate NW field-effect transistor and FinFET have been proposed as alternative structure,[33)] however, this structure basically deteriorate gate controllability. Moreover, they are not a suitable structure for future HP logic devices which requires a higher I_{on}. Therefore, another approach is needed.

In this framework, the aim of this paper is to improve SHE in Ge vertically stacked GAA NW pMOSFET by utilizing high thermal conductivity of aluminum oxide (Al_2O_3, alumina). Conventionally, even though Al_2O_3 also belongs to high-κ material, it has not received much attention due to low permittivity compared to HfO_2.[34] However, in the case of next-generation semiconductor devices, it is necessary to investigate a new method of utilizing higher thermal conductivity of Al_2O_3 [sub-10 nm thin film: 0.55 W $K^{-1} \times m^{-1}$][23] instead of HfO_2 [sub-10 nm thin film: 0.35 W $K^{-1} \times m^{-1}$],[23] since SHE issue has recently emerged with scaling effect (more heat generation per unit area from the increased transistor density).[35] Therefore, this research has tried to improve the SHE by incorporating Al_2O_3 as gate dielectric material.

This paper is organized as follows. Firstly, the basic electrical characteristics such as transfer curve and I_{on} are analyzed after calibration. Secondly, the improvement of SHE from the proposed structure has been demonstrated by the location of the heat sink and heat dissipation path. Then, the electrical characteristics enhancement from SHE improvement is discussed regarding effective hole mobility improvement and I_{on} enhancement. Finally, the method of simultaneously accomplishing SHE improvement and low gate leakage current (I_{gate}) have been specifically investigated and proposed with numerous simulation data.

2. Device structure and simulation methodology

The conventional device structure with HfO_2 and the proposed device structure utilizing Al_2O_3 used in this paper are simulated using Synopsys Sentaurus three-dimensional (3D) technology computer-aided design (TCAD) simulation.[36] For the detailed specification of structures, the values in the 5 nm node presented in IRDS is utilized.[16]

2.1. Device structure of Ge vertically stacked GAA NW pMOSFET

Figure 1 shows the schematic view of Ge vertically stacked GAA NW pMOSFETs. For a fair comparison, the same equivalent oxide thickness (EOT) is adopted in both the conventional Ge vertically stacked GAA NW pMOSFET (with HfO_2) [Fig. 1(b)] and the proposed Ge vertically stacked GAA NW pMOSFET (with Al_2O_3) [Fig. 1(c)]. The EOT of each device is calculated as Eq. (1), and "i" in Eq. (1) indicates the number of gate dielectric layers

$$\mathrm{EOT} = \sum_{n=1}^{i}\left(\text{Physical thickness} \times \frac{3.9\,\varepsilon_0}{\text{permittivity of each material}}\right). \quad (1)$$

EOT of 1.5 nm is initially adopted (and later, various EOT thicknesses of 1, 1.25, 2, 2.5, 3 nm are also applied for more details). Specifically, the conventional Ge vertically stacked GAA NW pMOSFET has 5.6 nm thick HfO_2 and 0.5 nm thick SiO_2 interfacial layers for EOT of 1.5 nm, whereas the proposed Ge vertically stacked GAA NW pMOSFET has 2.5 nm thick Al_2O_3 and 0.5 nm thick SiO_2 interfacial layers. Both structures have a gate length (L_{gate}) of 16 nm, channel thickness (T_{ch}) of 5 nm, and channel width (T_W) of 7 nm. The doping concentration in source/channel/drain regions are set as $1 \times 10^{21}/1 \times 10^{15}/1 \times 10^{21}$ cm^{-3}, respectively. The thermal conductivity of 7.5/0.45/0.55/0.35/28 W $K^{-1} \times m^{-1}$ are applied for Si (sub-10 nm channel)[22]/SiO_2 (interfacial layer)[37]/Al_2O_3 (sub-10 nm)[23]/HfO_2 (sub-10 nm)[23]/TiN (titanium nitride),[38] respectively. For details, all parameters are summarized in Table I.

For the precise analysis of the electrical and thermal characteristics, thermodynamics, high field saturation, Shockley–Read–Hall recombination, and Fermi models are used by Synopsys Sentaurus 3D TCAD simulation. Regarding tunneling mechanisms, trap-assisted-tunneling, direct tunneling, and Fowler Nordheim tunneling are considered to precisely investigate I_{gate} and off current (I_{off}).

2.2. Workflow of this study and calibration process

Figure 2(a) illustrates the overall workflow of this study. The calibration of GAA pMOSFET is performed with the fabricated device of the previous research[39] and then Ge vertically stacked GAA NW pMOSFET structure is applied. Finally, validation of the proposed Ge vertically stacked GAA NW pMOSFET is conducted in terms of SHEs and I_{gate}.

During calibration, quantum correlations are conducted with quantum mechanics adjustment for I_{DS}–V_{GS} calibration under Synopsys Sentaurus 3D TCAD simulation.[36] In specific, we adopt the mobility model (phumob/Enormal (Lombardi)/thin layer) to consider Coulomb scattering and interfacial surface roughness scattering. First, I_{DS}–V_{GS} calibration is proceeded by carefully applying the quantum model and velocity saturation model. Then, the work function is carefully adjusted for accurate I_{DS}–V_{GS} calibration. Thereafter, thermal boundary condition (300 K), thermal conductivity, heat conduction paths are adjusted to reflect the thermal characteristics of the GAA pMOSFET. Figure 2(b) shows our simulation results are well fit with the real measured data of the fabricated GAA pMOSFET.[39]

3. Results and discussion

3.1. Comparative analysis on electrical characteristics

Figure 3(a) shows the transfer characteristics of the conventional Ge vertically stacked GAA NW pMOSFET (incorporating HfO_2) and the proposed Ge vertically stacked GAA pMOSFET (incorporating Al_2O_3). The overall transfer characteristics are almost similar due to the same EOT. For accurately comparing the basic I_{on} of these structures, drain voltage (V_{DS}) and gate voltage (V_{GS}) is fixed at −0.7, −0.8 V, respectively. Remarkably, the actual value of I_{on} is greater with the proposed Ge vertically stacked GAA NW pMOSFET compared to the conventional Ge vertically stacked GAA NW pMOSFET. This is because the conventional Ge vertically stacked GAA NW pMOSFET suffers more SHEs compared to the proposed Ge vertically stacked GAA NW pMOSFET and more mobility degradation concomitantly occurs.

3.2. Improvement of SHE by the proposed structure and its scaling behavior

In order to investigate the improvement of SHE, the maximum temperature of the device is analyzed with the conventional Ge vertically stacked GAA NW pMOSFET and the proposed Ge vertically stacked GAA NW pMOSFET as demonstrated in Fig. 4. The maximum temperature is determined by the maximum lattice temperature among all device structure. The maximum temperature is calculated under $V_{DS} = -0.7$ V and $V_{GS} = -0.8$ V and it has been demonstrated that the maximum temperature is considerably

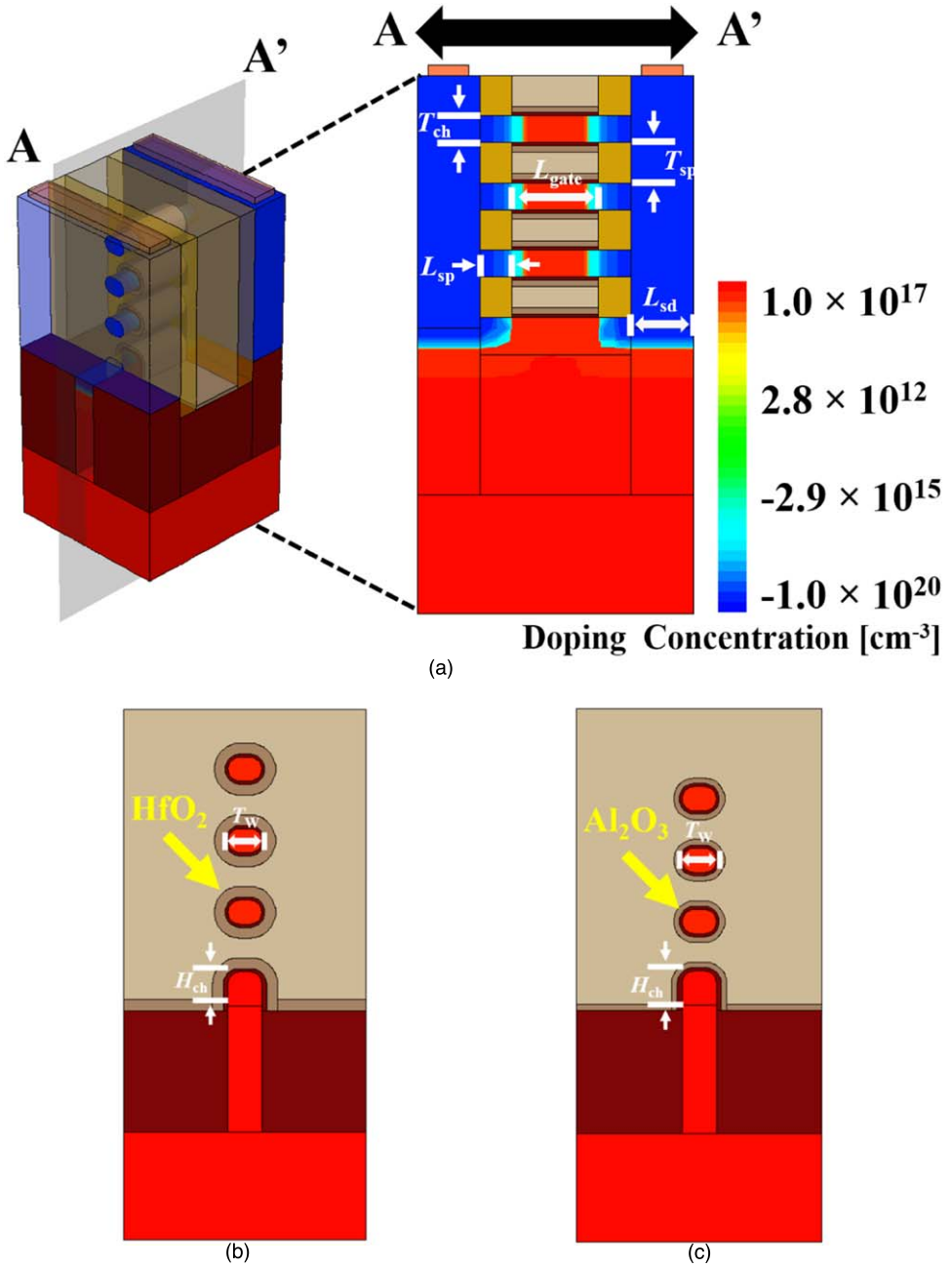


Fig. 1. (Color online) (a) Overall structure of the Ge vertically stacked GAA NW pMOSFET with a cross-sectional view, (b) cross-sectional view of the conventional Ge vertically stacked GAA NW pMOSFET (with HfO_2), and (c) cross-sectional view of the proposed Ge vertically stacked GAA NW pMOSFET (with Al_2O_3).

Table I. Dimension of the Ge vertically stacked GAA nanowire pMOSFET.

Symbol	Model parameter	Value	Unit
L_{gate}	Gate length	12/14/16/18	nm
L_{sd}	Source/drain length	6	
L_{sp}	Spacer length	6	
T_{ch}	Channel thickness	5	
T_W	Channel width	7	
T_{SiO_2}	Silicon dioxide thickness	0.5	
H_{ch}	Parasitic channel height	8	

improved from 534 to 419 K by using the proposed Ge vertically stacked GAA NW pMOSFET, as illustrated in Fig. 4(a). This is because the Al_2O_3 acts as an effective heat sink, namely an effective heat dissipation path from channel to metal as shown in Fig. 4(b).

For more details, the SHE improvement has been widely investigated with different L_{gate}. As illustrated in Fig. 5(a), especially in the case of the conventional Ge vertically stacked GAA NW pMOSFET, the maximum temperature increases as L_{gate} decreases. This is because the short channel effect including V_{TH} roll-off occurs as the device is scaled down [Fig. 8], and higher I_{on} flows with more heat generation [Fig. 7]. Therefore, this SHE improvement becomes more important as the device is scaled down, and our proposed strategy is much more important in future scaled devices.

In addition, this improvement also becomes noticeable as the EOT of device decreases. As shown in Fig. 5(b), the conventional Ge vertically stacked GAA pMOSFET (with HfO_2) that has lower EOT generates more heat compared to the others. This is because the reduced EOT makes more current flow and generates more heat. Therefore, our

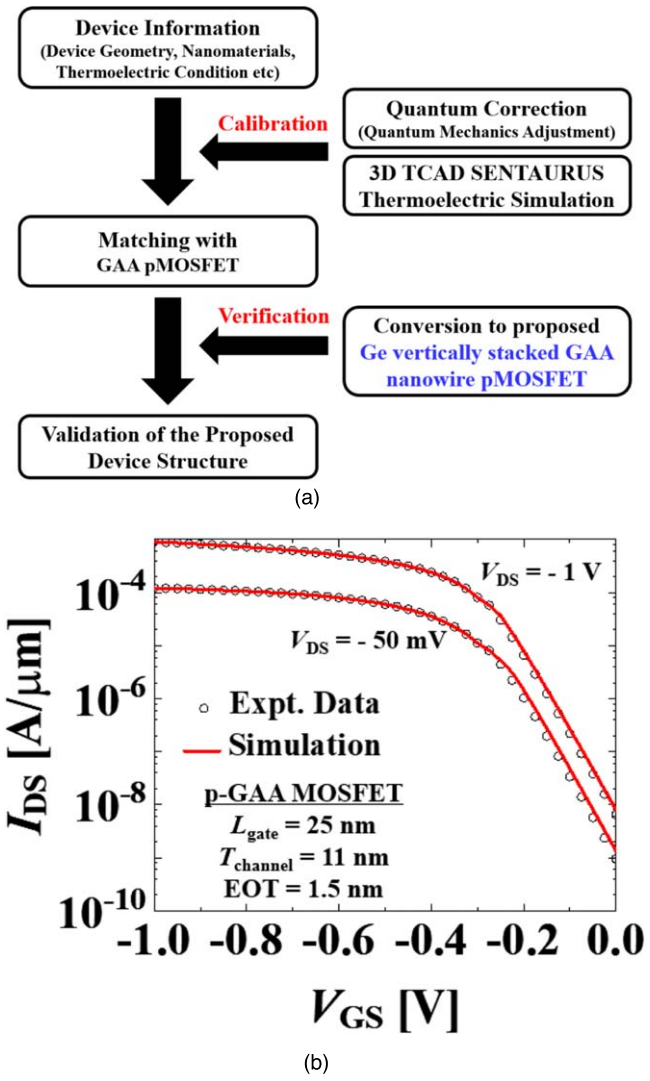


Fig. 2. (Color online) (a) Overall workflow for validation of the proposed Ge vertically stacked GAA NW pMOSFET structure, and (b) I_{DS}–V_{GS} calibration results with the GAA pMOSFET structure [40].

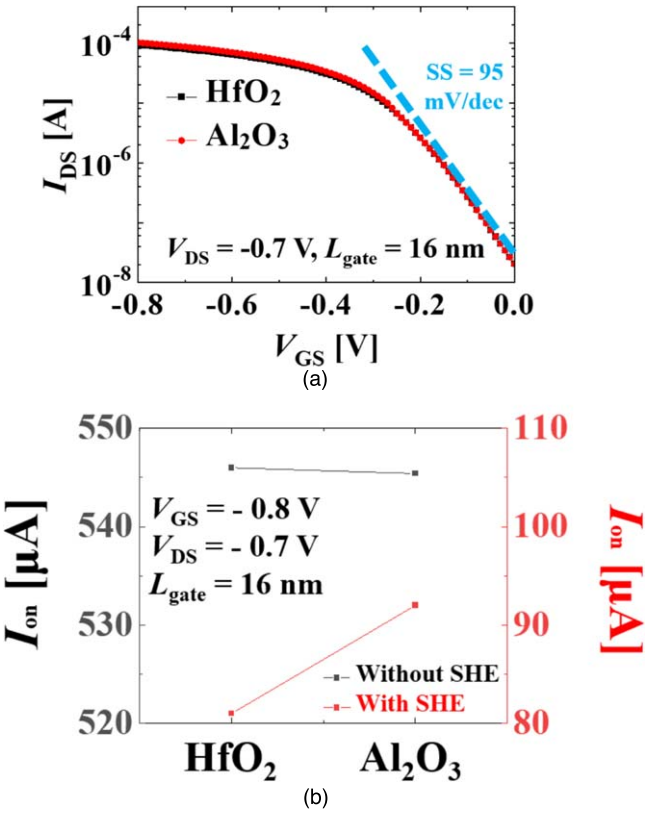


Fig. 3. (Color online) (a) Transfer characteristics of the conventional Ge vertically stacked GAA NW pMOSFET and the proposed Ge vertically stacked GAA NW pMOSFET, and (b) I_{on} comparison with and without SHE. It is remarkable that the proposed structure has higher I_{on} under same EOT condition due to improvement of SHE.

proposed technique is very strategic for future scaled devices with reduced EOT.

3.3. Enhancement of electrical characteristics by SHE improvement

The improvement of SHE mentioned above consequently leads to an improvement of electrical properties. In other words, SHE improvement eventually leads to improvement of effective hole mobility and I_{on} in Ge vertically stacked GAA pMOSFET. As demonstrated in Fig. 6, the effective hole mobility can be significantly improved through the proposed Ge vertically stacked GAA pMOSFET due to SHE improvement. Specifically, the effective hole mobility decreases as L_{gate} decreases [Fig. 6], because more SHE leads to more degradation of effective hole mobility.[30)]

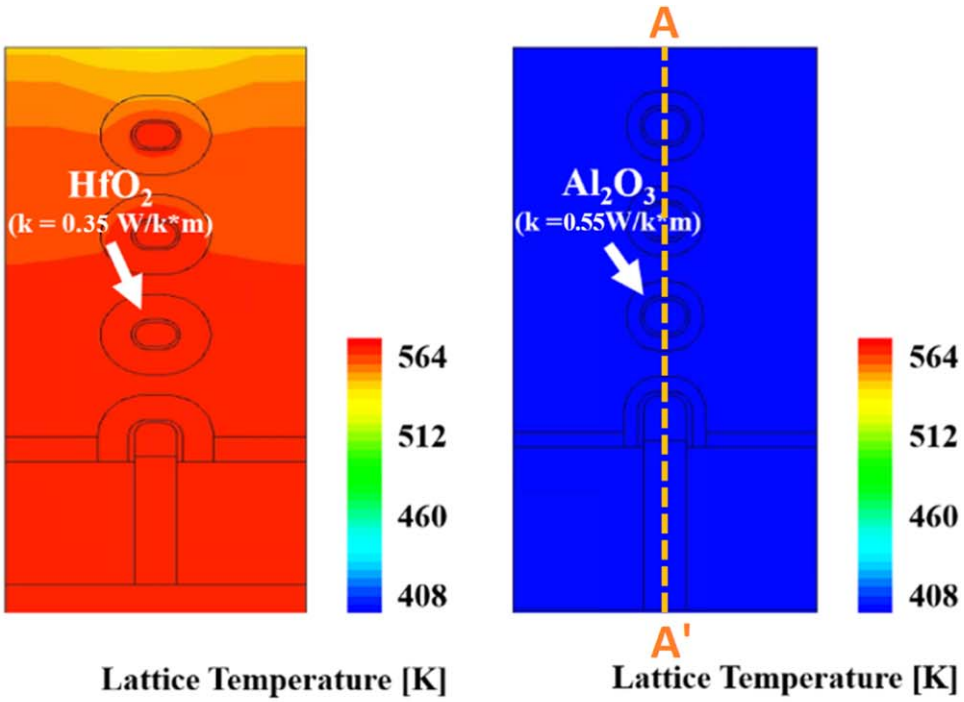
Figure 7 illustrates how much I_{on} improves due to the enhancement of effective hole mobility from the proposed structure. It is remarkable that it is possible to achieve higher I_{on} even with the same EOT value by adopting our proposed structure. Therefore, the proposed Ge vertically stacked GAA NW pMOSFET can act as a strategic device structure for the next-generation HP device.

In addition, our improvement becomes remarkable as the device scaled down. As demonstrated in Fig. 7, Ion becomes greater as the device scaled down due to the threshold voltage roll-off issue [Fig. 8], and hence more heat is generated consequently. Therefore, our proposed improvement technique becomes more important as the device scaled down.

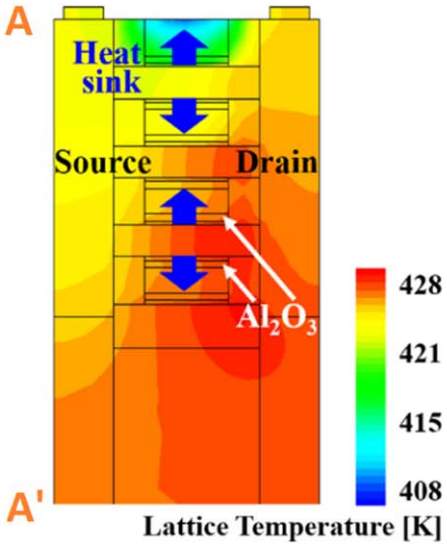
3.4. Viable Al_2O_3 thickness maintaining low gate leakage current

So far, it has been demonstrated that the proposed device structure utilizing Al_2O_3 can alleviate SHE and improve I_{on}. However, there must be some important questions that readers may be wondering about. It is the limitation of low permittivity, which is a disadvantage of Al_2O_3 compared to HfO_2. Specifically, Al_2O_3 has a lower permittivity than HfO_2, and thus a much thinner oxide film is needed to be made for the same EOT. This can cause a I_{gate} issue. Fortunately, the higher bandgap of Al_2O_3 (7.0 eV) (see bandgap of HfO_2: 5.6 eV)[40)] can act as a buffer to alleviate this issue. In this section, the I_{gate} issue will be discussed with a detailed explanation.

First, it is investigated how much I_{gate} flows in both structure under the condition of the same physical thickness. As shown in Table II, it is demonstrated that the proposed Ge vertically stacked GAA NW pMOSFET has lower I_{gate} compared to the conventional Ge vertically stacked GAA NW pMOSFET under same interfacial layer thickness (T_{SiO_2}) and high-κ layer thickness ($T_{high\text{-}k}$). In specific, the I_{gate} is reduced by about 40%–50% [Table II] and this can be explained by energy band diagram. As illustrated in Fig. 11, HfO_2 has bandgap of 5.6 eV whereas Al_2O_3 has bandgap of 7.0 eV. Therefore, the proposed Ge vertically stacked GAA



(a)



(b)

Fig. 4. (Color online) (a) Cross-sectional view at the center of the channel describing distribution of lattice temperature in the conventional Ge vertically stacked GAA NW pMOSFET and the proposed Ge vertically stacked GAA NW pMOSFET, and (b) another cross-sectional view at the center of the channel illustrating the location of the heat sink in the proposed Ge vertically stacked GAA NW pMOSFET. (The duration of 1 s is applied with V_{GS}.)

pMOSFET has lower conduction band offset (E_{CBO}) and lower valence band offset (E_{VBO}) at the same time. Thus, the proposed Ge vertically stacked GAA pMOSFET has lower direct tunneling, which result in less I_{gate}.

Second, it is analyzed how much I_{gate} flows in both structure under the same EOT condition. The results are summarized in Fig. 9 (HfO_2) and Fig. 10 (Al_2O_3). From the excellent permittivity of HfO_2, the HfO_2 can have approximately twice physical thickness compared to Al_2O_3 when both are made under the same EOT condition. Therefore, it is found that the conventional Ge vertically stacked GAA pMOSFET (with HfO_2) has lower I_{gate} than the proposed Ge vertically stacked GAA pMOSFET (with Al_2O_3). Then, for successfully utilizing Al_2O_3 as gate dielectric material, it is essential to investigate the method for achieving both SHE improvement and I_{gate} suppression at the same time while utilizing Al_2O_3. The viable solution can be found in the result of Fig. 10. Namely, three factors (1) permittivity of fabricated Al_2O_3, (2) EOT value, and (3) T_{SiO_2} must be considered simultaneously.

As many previous researches have demonstrated, in the case of Al_2O_3, its dielectric constant depends on how the fabrication process is performed and it is usually between 9 and 12.[41,42] Even though some previous researches show it is possible to fabricate Al_2O_3 with a dielectric constant between 15 and 20 by depositing Al_2O_3 with adding Silver (Ag) atoms,[43] our research does not contain this case because it is unclear whether or not a thin film about 3 nm could be made with good oxide quality by this method.

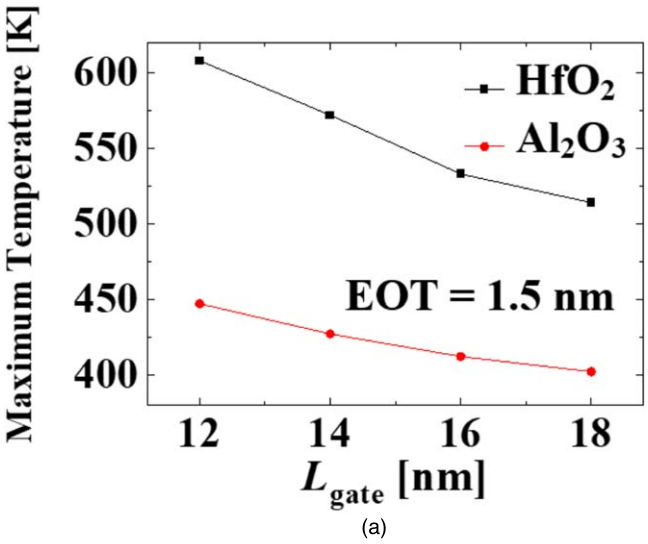


Fig. 5. (Color online) (a) Maximum temperature in two structures with different L_{gate}, and (b) maximum temperature in two structures with different EOT.

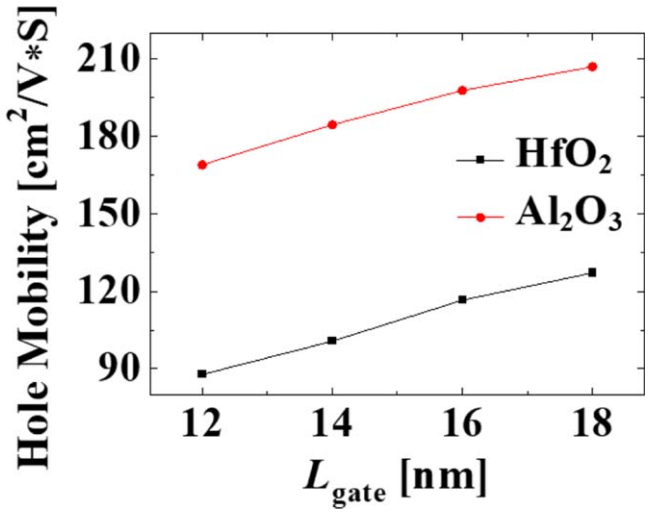


Fig. 6. (Color online) Improvement in effective hole mobility by using the proposed Ge vertically stacked GAA NW pMOSFET with various L_{gate}.

Figure 10 provides numerous simulation data with I_{gate}. It is possible to achieve meaningful interpretation by adopting 3 ways as follows. First, the higher the permittivity of Al_2O_3, the lower I_{gate} can be achieved at the same EOT and T_{SiO_2},

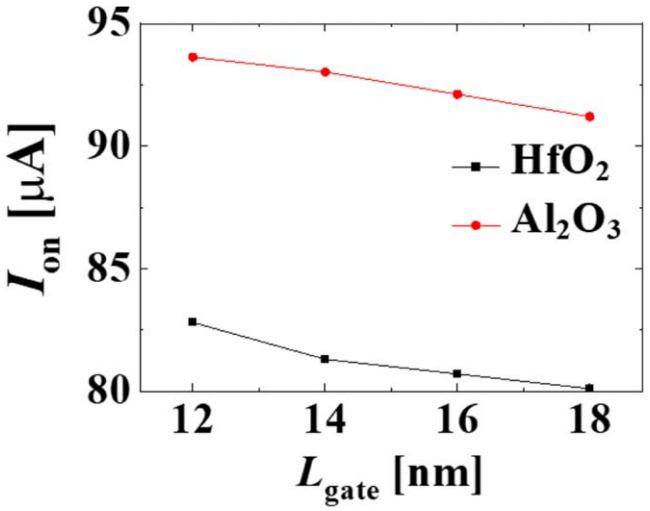


Fig. 7. (Color online) Improvement of I_{on} by adopting the proposed Ge vertically stacked GAA NW pMOSFET with various L_{gate}.

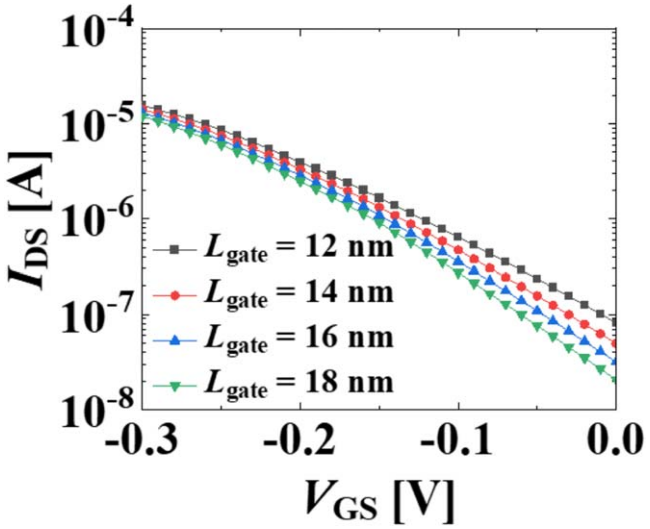


Fig. 8. (Color online) V_{TH} roll-off issue due to short L_{gate}.

Table II. Gate leakage current with respects to different gate dielectric material. (T_{SiO_2}, $T_{high\text{-}k}$, T_{GD} stand for interfacial layer thickness, high-κ dielectric thickness, and total gate dielectric thickness, respectively)

T_{SiO_2} [nm]	$T_{high\text{-}k}$ [nm]	T_{GD} [nm]	I_{gate} [fA] (HfO_2)	I_{gate} [fA] (Al_2O_3)
0.4 nm	3.4	3.8	0.4	0.2
0.5 nm	2.8	3.3	22.8	11.3
0.6 nm	2.2	2.8	196.3	130.1

because the same EOT value can be made with thicker physical oxide layers. Second, in the same EOT condition and Al_2O_3 permittivity condition, the lower I_{gate} can be achieved by lower T_{SiO_2}. Specifically, when the device is fabricated with lower T_{SiO_2}, the thicker high-κ layer can be used and the total physical thickness of gate dielectric materials consequently increases. Therefore, the dielectric tunneling can be effectively suppressed and lower I_{gate} can be achieved. Third, even though the lower I_{gate} can be achieved by applying the higher EOT, it can also cause deterioration of subthreshold swing. Therefore, selecting an appropriate EOT value under this trade-off issue will be the key in the next-generation Ge vertically stacked GAA NW pMOSFET.

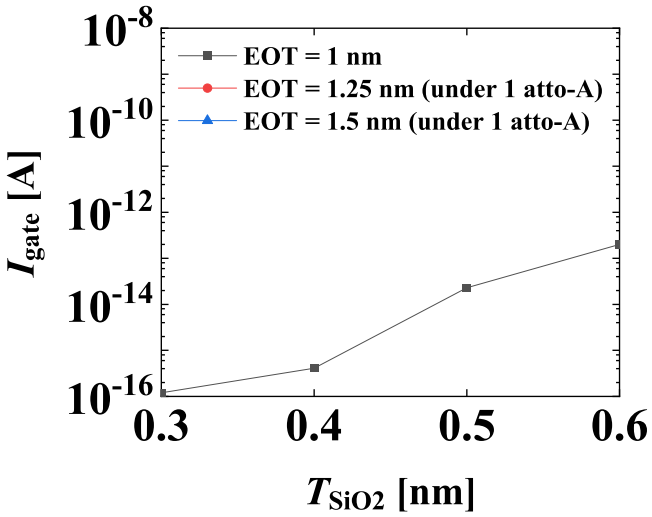


Fig. 9. (Color online) Gate leakage current by adopting HfO_2 as high-κ dielectric material. (T_{SiO_2} stands for interfacial layer thickness)

In addition to the aforementioned "qualitative analysis", a meaningful conclusion that can be drawn through "quantitative analysis" with Fig. 10 are as follows. First, when Al_2O_3 is made with permittivity of $12\varepsilon_0$, sub-1fA I_{gate} can be achieved if the T_{SiO_2} is less than 0.5 nm. At this time, the options become wider. If the manufacturer aims to reduce EOT, I_{gate} can be achieved at the 10^{-14} A scale by reducing EOT to about 1.25 nm. Second, when the permittivity of Al_2O_3 is made $11\varepsilon_0$–$12\varepsilon_0$, it is necessary to fabricate thinner interfacial layer (lower T_{SiO_2}). In this case, by making T_{SiO_2} to 0.3 nm, there is a possibility of lowering I_{gate} to about 1fA. Third, when the permittivity of Al_2O_3 is made $9\varepsilon_0$, EOT must be taken to 1.5 nm and T_{SiO_2} must be maintained at 0.3 nm to barely achieve I_{gate} at the 10^{-14} A scale.

3.5. SHE according to alternating current (AC) signal

Considering the practical operating condition of recent semiconductor logic devices, it might be essential to investigate the SHE according to AC signal. When an AC signal is applied to the gate, the SHE is different from when a direct current (DC) signal is applied. This is because the heat-accumulation/heat-dissipation repeatedly occur under AC condition. In specific, heat-accumulation occurs during ON states and heat-dissipation occurs during OFF states.

For investigating the effect of AC signal on the SHE, a pulse-type input signal was given [Fig. 12]. A voltage of −0.8 V, an increased time of 5% of a period, a decreased time of 5% of a period, and a duty cycle of 50 % are injected to gate contact. Figure 13 shows thermal characteristics according to frequency. In the 100 megahertz (MHz) band [Fig. 13(a)], the heat-accumulation and heat-dissipation are repeatedly generated. However, the overall maximum temperature is increased as more cycles are applied. This is because the 1 cycle of heat-accumulation/heat-dissipation leaves background heat. This tendency can be also found in 1 gigahertz (GHz) band [Fig. 13(b)] and 10 GHz band [Fig. 13(c)].

From 1 GHz, the maximum temperature decreases compared to 100 MHz. This is *G* because there is less time to

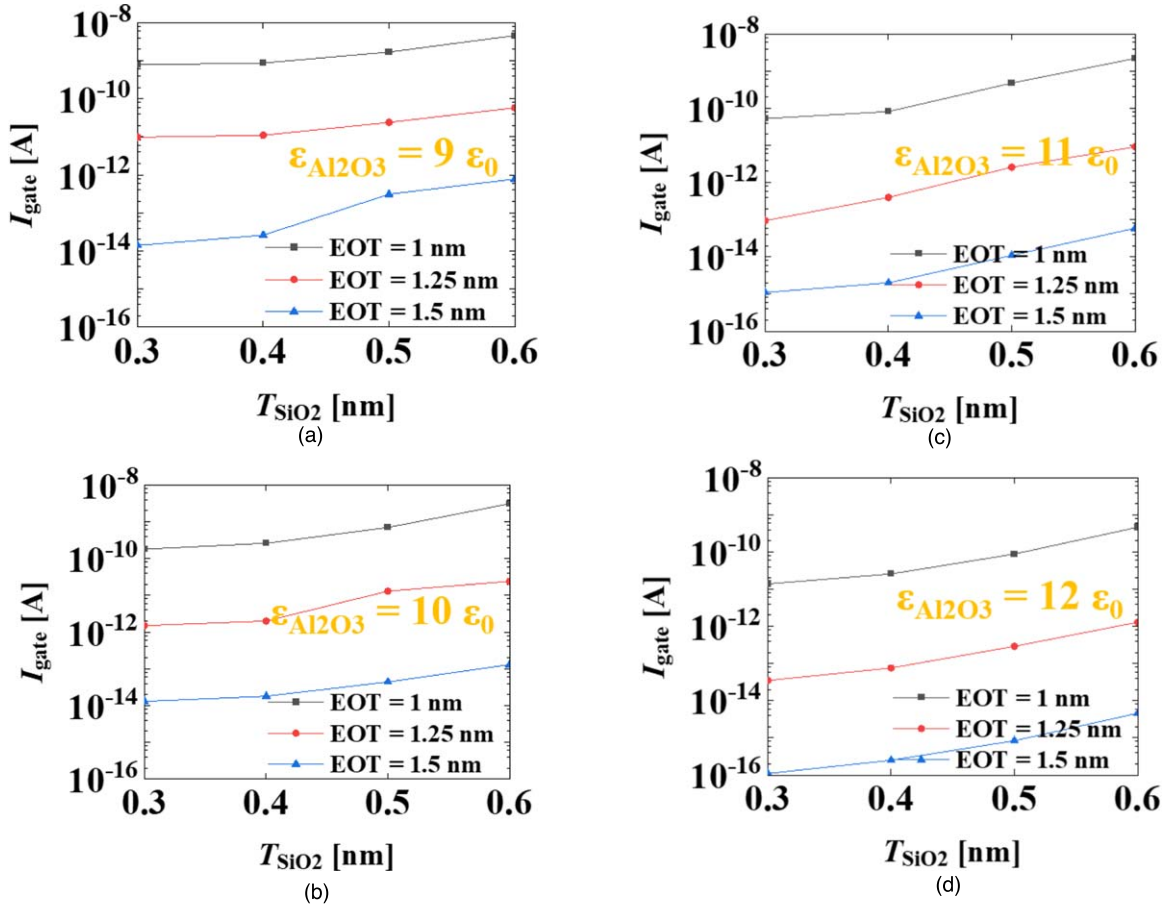


Fig. 10. (Color online) Gate leakage current by adopting Al_2O_3 as high-κ dielectric material with the permittivity of (a) $9\varepsilon_0$, (b) $10\varepsilon_0$, (c) $11\varepsilon_0$, and (d) $12\varepsilon_0$. (T_{SiO_2} stands for interfacial layer thickness)

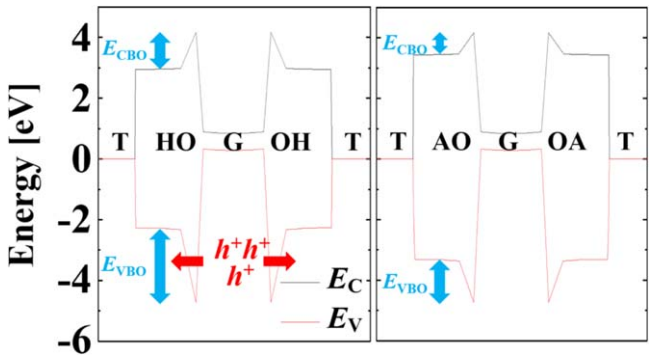


Fig. 11. (Color online) Energy band diagram in the conventional Ge vertically stacked GAA NW pMOSFET and the proposed Ge vertically stacked GAA NW pMOSFET (T, H, O, G, A stand for TiN, HfO_2, SiO_2, Ge, Al_2O_3, respectively).

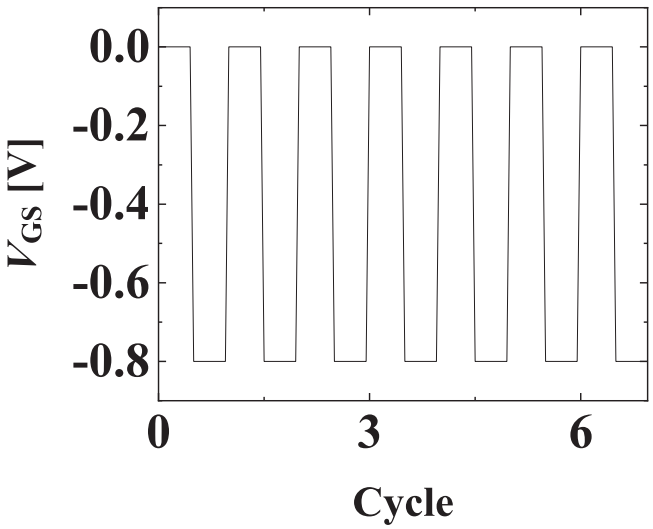


Fig. 12. Pulse signal V_{GS} input for AC analysis.

accumulate heat. However, there is also less time to dissipate the heat in the 1 GHz band compared to a 100 MHz band. Therefore, only 18% of increased temperature (during ON state) is dissipated during OFF state. As a result, heat is increasingly accumulated under 1 GHz as more cycles are applied, compared to 100 MHz.

Under 100 MHz, 1 GHz, 10 GHz, it has been demonstrated that incorporating Al_2O_3 could improve the thermal performance of the semiconductor logic devices. Even though less heat is generated under AC conditions compared to DC conditions, the SHE improvement can be commonly achieved under both AC and DC conditions by utilizing Al_2O_3.

In summary, it would be desirable to fabricate thin Al_2O_3 film as well as possible and increasing its permittivity as much as possible. In addition, it would be much better if a fabrication technology will be further developed and be capable of making an interfacial SiO_2 layer as thin as possible with good film quality. The fabrication method for making Al_2O_3 with high permittivity[44,45] and making a good thin SiO_2 interfacial layer[46,47] have been broadly researched in many previous studies. Therefore, researchers who are reading this paper are recommended to look for these relevant previous researches and fabricate it based on their knowledge if possible.

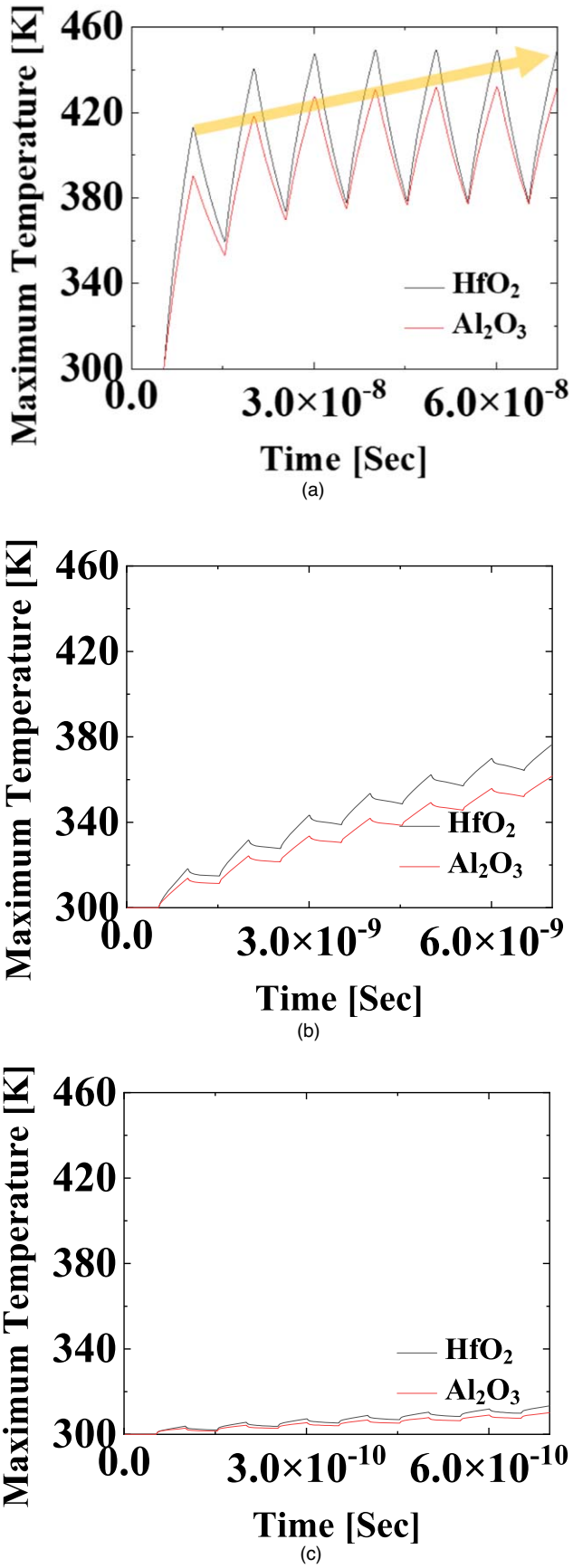


Fig. 13. (Color online) Maximum temperature difference at (a) 100 MHz, (b) 1 GHz, and (c) 10 GHz.

3.6. Proposal for future research

We have proposed the design methodology for improving the thermal performance of HP semiconductor logic devices.

However, even though our research has put a lot of effort to validate our proposed design methodology of electrical/thermal co-design, our research is basically based on simulation results and it may be different from the real fabricated device. For example, the quality of dielectric films (including the amount of fixed charge and carrier traps) may affect the electrical characteristics and reliability issue. As demonstrated in lots of previous research,[44–47] the quality of dielectric films depends heavily on the fabrication method. Therefore, we the authors would like to suggest future research to readers by fabricating our proposed device structure. It may be an interesting and desirable topic to optimize the high-κ dielectric film layers by electrical/thermal co-design with the parameter of thermal conductivity, fixed charge, carrier traps, bandgap, I_{gate}, and thermal performance.

4. Conclusions

We have demonstrated the improvement of self-heating characteristics by our proposed structure with Al_2O_3 in Ge vertically stacked GAA NW pMOSFET. Our proposed structure utilizes the advantage of the high thermal conductivity of Al_2O_3 for improving SHE. As a result, the SHE is significantly improved under both AC and DC conditions since the Al_2O_3 acts as an effective heat sink. Our proposed structure is very strategic for the future HP logic device market with the improved SHE and high on current.

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