Japanese Journal of Applied Physics

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To cite this article: Yoshihiro Koga and Kazunari Kurita 2020 *Jpn. J. Appl. Phys.* **59** 051002

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Japanese Journal of Applied Physics **59**, 051002 (2020) **REGULAR PAPER**

https://doi.org/**10.35848/1347-4065/ab82af**

Fabrication of silicon on insulator wafer with silicon carbide insulator layer by surface-activated bonding at room temperature

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Received November 14, 2019; revised March 10, 2020; accepted March 23, 2020; published online April 21, 2020

We propose a process for the fabrication of a silicon-on-insulator (SOI) wafer with a silicon carbide (SiC) insulator layer by combining plasma-enhanced chemical vapor deposition and surface-activated bonding without thermal stress to obtain sufficient thermal conductivity for self-heating power and high-frequency device applications. The thermal conductivity of the deposited SiC layer is twice that of a silicon dioxide (SiO_2) layer, and the breakdown electric field of this layer is 10–11 MV cm^{-1}, the same as that of a SiO_2 layer. In addition, the bonding interface between the silicon layer and the deposited SiC insulator layer has no voids or punch-out dislocations. Therefore, the SOI wafer with a SiC layer has high thermal conductivity and breakdown electric field; this SOI wafer and its fabrication process will be important for the realization of next-generation self-heating devices such as power and high-frequency devices. © 2020 The Japan Society of Applied Physics

1. Introduction

Abnormal weather due to global warming has been occurring worldwide, resulting in many natural disasters: thus, the reduced use of fossil fuels has become increasingly important. For example, gasoline cars are being replaced with hybrid electric and fully electric cars. These cars include many electric devices.[1,2] Power devices are the most important components for automobiles to operate at a high-voltage and a high electric current. It is necessary to manufacture next-generation automobiles with custom power devices having breakdown voltages of at least several hundred volts. Since such automobiles are powered by battery motors, it is important to decrease the leakage current in the electrical isolation regions between such power devices. Therefore, it is essential to clarify how the electrical isolation regions between such power devices are formed.

On the other hand, the Internet of Things can connect wireless communication applications, such as smartphones, tablets, high-definition multimedia interfaces, automobiles, and robots.[3–5] Since high-frequency devices have been widely used in wireless communication applications, it will be necessary for these applications to send larger amounts of data to data centers in the future. Thus, high-frequency devices must operate at a higher speed in the future. In addition, since wireless communication applications are operated by batteries, future high-frequency devices must have lower power consumption to operate at a higher speed. Therefore, it is also important to know how to form electrical isolation regions between such high-frequency devices.

Figure 1 shows a cross-sectional image of power and high-frequency devices fabricated on a silicon wafer. Devices A, B, and C are surrounded by electrical isolation regions. When the isolation regions are formed by a pn junction, it is necessary to implant boron and phosphorus into the silicon wafer to dope carriers for p-type and n-type formation in the isolation region. After such implantation, annealing is necessary to recrystallize the silicon wafer to repair the damage generated by implantation and electrically activate the implanted boron and phosphorus. However, because the recrystallization of the implanted silicon wafer and the electrical activation of the implanted elements are not perfect, a leakage current is generated between the devices through the pn junction at a high temperature and voltage.[6,7] Thus, such isolation is not useful for conventional power and high-frequency devices, and the most efficient way to decrease the leakage current through an isolation region is to replace a pn junction with silicon dioxide (SiO_2) without the damage caused by implantation.[8–13]

Silicon-on-insulator (SOI) wafers have been used to fabricate power and high-frequency devices.[14,15] Figure 2(a) shows a cross-sectional image of an SOI wafer. This wafer has a buried oxide (BOX) layer made of SiO_2 as the insulator layer in the wafer. Figure 2(b) shows an SOI wafer containing isolation regions made of SiO_2 formed by shallow trench isolation (STI).[9] The devices in this SOI wafer are surrounded by SiO_2, which comprises a BOX layer and an STI region. Because SiO_2 has low thermal conductivity, these devices are self-heating,[16] and thus their electrical characteristics deteriorate owing to their self-heating, adversely affecting their performance. To resolve this issue, the BOX layer is changed from SiO_2 to an alternative material with sufficient thermal conductivity.

Wide-band-gap semiconductor materials generally have a high breakdown electric field.[17] In particular, diamond and silicon carbide (SiC) also exhibit high thermal conductivity.[18] The breakdown electric field of single-crystal diamond is the highest among the semiconductor materials. However, it is difficult to grow diamond on a substrate of another material. Since the difference in the lattice constant between single-crystal diamond and silicon is above 30%,[18] single-crystal diamond is difficult to grow on a silicon substrate. On the other hand, polycrystalline diamond can be easily grown on substrates of other materials by scratching with diamond powder or by carbon-bias-enhanced nucleation to form seeding diamond.[19,20]

In a previous study, we deposited polycrystalline diamond on a silicon substrate as an insulator layer by seeding spin-coated nanometer-size diamond on the surface of the substrate.[21] The polycrystalline diamond layer exhibited

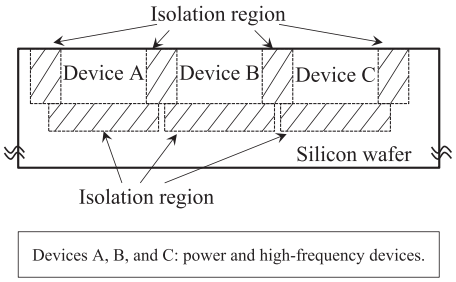

Fig. 1. Cross-sectional image of power and high-frequency devices fabricated on a silicon wafer.

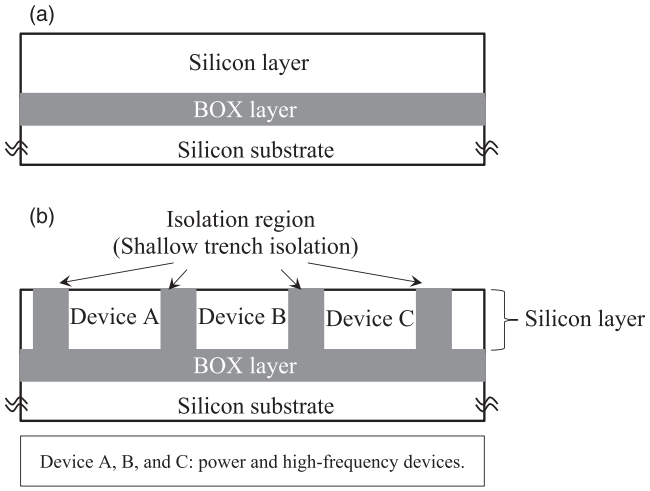

Fig. 2. Cross-sectional image of SOI wafers. (a) SOI wafer and (b) SOI wafer with fabricated power and high-frequency devices.

higher thermal conductivity than the SiO_2 layer. However, its breakdown electric field was lower than that of the SiO_2 layer. When a polycrystalline diamond layer is formed as an insulator layer for customized power devices operating above 1000 V, it may have a thickness of more than 10 μm. We thus assume that an SOI wafer with a polycrystalline diamond insulator layer is not useful for customized power devices operating above 1000 V. In this study, we have been attempting to form a SiC layer as an insulator layer with thermal conductivity similar to that of diamond. A temperature of above 1300 °C is necessary for the growth of a SiC crystal layer.[22–24] If a SiC crystal layer is grown on a silicon substrate above 1300 °C, many slips will be generated in the silicon substrate and the substrate will warp. Thus, we attempted to grow a SiC layer on a silicon substrate at a low temperature using standard chemical vapor deposition equipment.

It generally takes a few hours to fabricate an SOI wafer by bonding a silicon layer to a BOX layer as well as a temperature of more than 800 °C.[25] Because of the long time and high temperature, the doping element used to form the pn junction in the silicon layer on the BOX layer is out-diffused and leakage current is generated at the pn junction in the well region of the fabricated device. In this study, a silicon layer is fixed to a SiC layer by surface-activated bonding (SAB) at room temperature in an ultrahigh vacuum for a short time.[26,27] Because the silicon layer is bonded to the SiC layer without the need for a high temperature for a long time, the doping element in the silicon layer is not out-diffused. In addition, no metallic impurities contaminate the SOI wafer.

2. Experimental methods

Figure 3 shows our method of fabricating an SOI wafer with a SiC layer. Three silicon wafers were fabricated: a base wafer, a bonding wafer, and another wafer. The SiC layer was deposited on the base wafer by plasma-enhanced chemical vapor deposition (PE-CVD) with flows of CH_4 and CH_3SiH_3 at 300 °C.[28] After depositing the SiC layer on the base wafer, its top surface was polished by chemical mechanical polishing (CMP).

The bonding wafer was then fixed to the base wafer with the polished SiC layer by SAB at room temperature in an ultrahigh vacuum for a short time. Figure 4 illustrates this SAB process. It is generally necessary for the temperature to be above 1300 °C to grow a single-crystal SiC layer.[22–24] Because the temperature in our study was less than 1300 °C, the deposited SiC layer is not a single-crystal and has many stable dangling bonds, making it difficult to attach to a silicon layer and thus connect two substrates. Therefore, an ultra thin silicon layer was deposited as an adhesive layer on the SiC

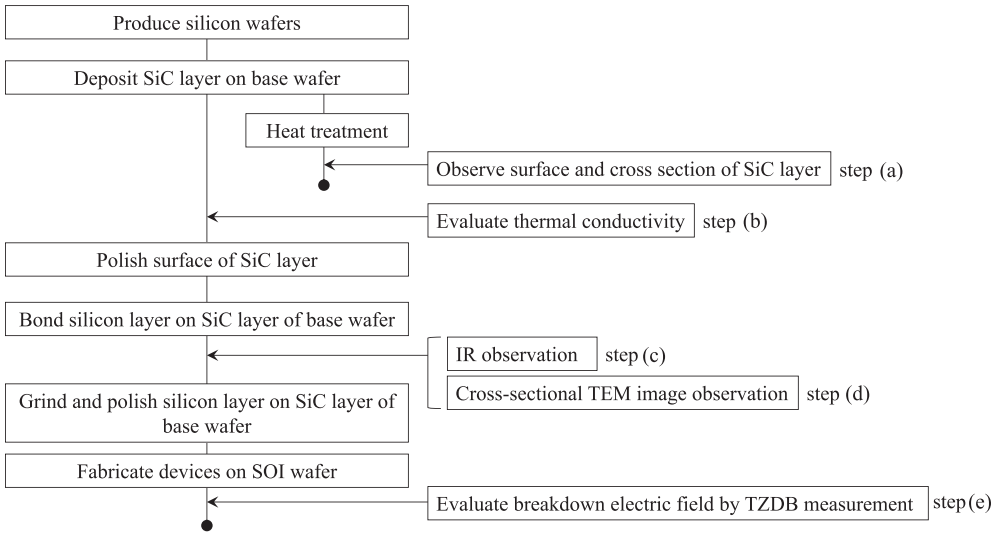

Fig. 3. Experimental flow. Step (a): observation of SiC layer, step (b): evaluation of thermal conductivity, step (c): IR observation, step (d) cross-sectional TEM image observation, and step (e): evaluation of breakdown electric field by TZDB measurement.

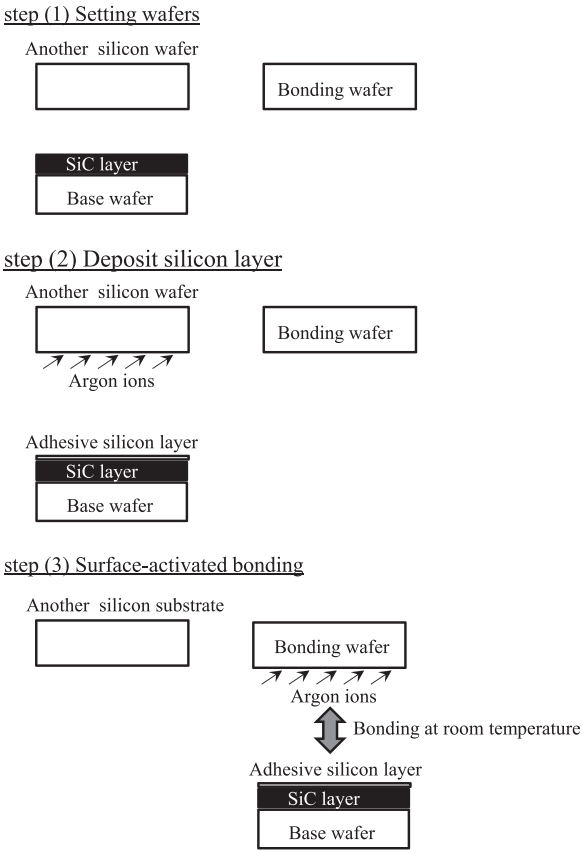

Fig. 4. Flow of fixing bonding layer on SiC layer by SAB. Step (1): setting of three wafers, step (2): deposition of ultrathin adhesive silicon layer on the SiC layer, and step (3): SAB of wafer on the SiC layer.

layer to bond the bonding wafer to the base wafer with the SiC layer. The ultrathin silicon layer deposition was carried out by irradiating another silicon wafer with argon ions and sputtering the silicon from the other silicon wafer before bonding the bonding wafer to the base wafer with the SiC layer [step (2)]. Then, the bonding wafer was activated by irradiating argon ions and bonded to the SiC layer through this ultra thin silicon layer [step (3)].[29,30] After bonding the two wafers (the bonding wafer and the base wafer with the SiC layer), the bonding wafer was ground and polished from the back side, which is opposite the wafer-bonding region, to the thickness of the active layer of the device. In addition, a reference SOI wafer was fabricated using SiO_2 as an insulator layer instead of SiC by PE-CVD.

2.1. Sample preparation

(100) Czochralski (CZ) 2 inch silicon wafers were used in this study. The base wafer and bonding wafer making up the silicon layer were polished to a thickness of 500 μm. These wafers were made of boron-doped CZ silicon single-crystal. Their resistivity was 5 Ω cm and their oxygen concentration was 1.2×10^{18} atoms cm^{-3}. A SiC insulator layer was deposited on one of the 2 inch base wafers at 300 °C by PE-CVD at flow rates of 130 sccm for CH_4 and 25 sccm for CH_3SiH_3, as shown in Fig. 3. The thickness of this layer was varied from 140 nm to 6 μm depending on the evaluation; the thicknesses used to evaluate the thermal stability, the thermal conductivity, and the breakdown electric field of the insulator layer were 6 μm, 4 μm, and 140 nm, respectively. The surface of this insulator layer was polished by CMP. Then, an ultra thin silicon layer was deposited on the insulator layer of this base wafer, and the base wafer was fixed to the bonding wafer by SAB in an ultrahigh vacuum of less than 1×10^{-5} Pa at room temperature (Mitsubishi Heavy Industries Machine Tool Co., Ltd. MWB08-AX). The three silicon wafers (the bonding wafer, the base wafer with the SiC layer, and another wafer for the deposition of the ultra thin silicon layer) were irradiated with argon ions at an energy of 1–2 keV for 5 min. After bonding the bonding wafer and the base wafer with the insulator layer, the back side of the bonding wafer was ground and polished to a thickness of 20 μm. A reference sample was fabricated by the PE-CVD of SiO_2 as the insulator layer at 500 °C and fixed by SAB at room temperature.[31]

2.2. Experimental procedure

As shown in Fig. 3, the SiC layer was deposited on the base wafer as the insulator layer. The surface of the SiC layer was then observed to evaluate its thermal stability after heat treatment [step (a)]. The thermal conductivity of the SiC layer on the base wafer was continuously evaluated [step (b)]. Next, voids and defects were searched for after bonding the silicon layer to the SiC layer [steps (c) and (d)]. Finally, after the bonding wafer was ground and polished as the active layer of devices, actual devices were fabricated on the silicon layer for time-zero dielectric breakdown (TZDB) measurement,[32] and the breakdown electric field of the SiC layer was evaluated using these fabricated devices [steps (e)].

2.2.1. Observation of surface of SiC layer on base wafer and cross section of studied SOI wafer. An OPTIPHOT-88 microscope (Nikon) was used for optical microscopy (OM) and an H9000UHR-I microscope (Hitachi) was used for transmission electron microscopy (TEM). OM was performed to characterize the coverage of a SiC layer of 6 μm thickness after depositing it on the base wafer and after heat treatment. This heat treatment was carried out at 1100 °C for 4 h in nitrogen, where the high temperature and prolonged treatment were to simulate the heat process during power device fabrication,[33,34] and the sample stage was loaded and unloaded at 900 °C in nitrogen in a furnace. Cross-sectional TEM and high-resolution TEM (HR-TEM) images were used to characterize structural defects, such as wafer-bonding-induced defects, during the fabrication of the bonding wafers.

2.2.2. Evaluation of thermal conductivity of SiC layer on base wafer. We evaluated the thermal conductivity of the studied sample and a reference sample formed with only an insulator layer of 4 μm thickness without bonding a silicon layer. The studied sample consisted of a SiC layer on a base wafer, and the reference sample consisted of a SiO_2 layer on a base wafer. The thermal conductivity of the insulator layer on the base wafer was evaluated by transiently measuring the resistivity at the surface of the sample after applying heat to the surface of the insulator layer on the base wafer. The thermal conductivity was evaluated using a TCi Thermal Property Analyzer (C-Therm Technologies).[35,36] This analyzer is composed of a sensor, control electronics, and computer software. The sensor has a spiral central heater/sensor element surrounded by a guard ring. The guard ring generates heat in addition to the spiral heater, thus approximating the one-dimensional heat flow from the sensor into the material under test in contact with the sensor. The voltage drop on the spiral heater was measured before and during each transient measurement. The voltage data were then

translated into values of thermal conductivity for the tested material.

2.2.3. Evaluation of voids remaining after bonding silicon layer to SiC layer on base wafer. The remaining voids were evaluated by infrared (IR) transmission observation after bonding a silicon layer to the SiC layer deposited by SAB at room temperature in an ultrahigh vacuum. An IRise (Moritex) system was used for the IR observation. In this system, because the wavelength of the IR radiation is higher than 1000 nm, the IR radiation is transmitted through a silicon wafer and reflected by the remaining voids. Thus, the remaining voids in a wafer can be detected by this IR irradiation.

2.2.4. Evaluation of breakdown electric field of SiC layer in SOI wafer. Two SOI wafers (test and reference) were also fabricated to form a 140 nm thick layer to investigate the intrinsic breakdown electric field. The studied sample had a SiC layer deposited on an SOI wafer as an insulator layer. On the other hand, the reference sample had a SiO_2 layer deposited as an insulator layer. The breakdown electric field for the layers of these samples was then evaluated by TZDB measurement after patterning a test element group (TEG) in the silicon layer on these layers to connect a metal on the silicon layer. This TZDB measurement is a voltage-step-stress method. While a voltage of 0 V was supplied to the silicon substrate under the deposited layer, an additional input voltage of 0.1 V was supplied to the silicon layer on the deposited layer. A Keithley 237 High-Voltage Source-Measure Unit (Keithley) was used as the measurement system and an STN-W010-D0.5-L32 system (Tiatech) was used as the probing equipment. The probe was made of tungsten and had a diameter of 10 μm.

3. Results and discussion

3.1. Evaluation of thermal stability of SiC layer on base wafer

We observed the surface of the SiC layer of 6 μm thickness on the base wafer after heat treatment at 1100 °C for 4 h in nitrogen. Figure 5(a) shows a photograph of a quarter of a wafer before heat treatment (after depositing the SiC layer on the base wafer). The SiC layer was deposited on the wafer from the center to 3 mm from the edge; the remaining area was where the sample holder of the deposition equipment fixed the silicon wafer, so no SiC layer was deposited in this area. Figure 5(b) shows a photograph of the wafer after heat treatment. The entire wafer was gray, similar to the base wafer before depositing the SiC layer. Therefore, we found that the deposited SiC layer on the base wafer was removed and concluded that this SiC layer had poor thermal stability.

We then fabricated a sample with a SiC layer having thermal stability. A thin silicon nitride (SiN) layer was formed on a SiC layer as a capping layer by PE-CVD at flow rates of 25 sccm for CH_3SiH_3 and 120 sccm for N_2. The thickness of the SiN layer was 20 nm. Figure 6(b) shows a cross-sectional OM image of this sample capped with the SiN layer after heat treatment at 1100 °C for 4 h. This SiC layer remained after heat treatment. Therefore, this SiC layer and capping SiN layer had thermal stability.

3.2. Evaluation of thermal conductivity of SiC layer on base wafer

We fabricated a base wafer with a SiC layer of 4 μm thickness and a capping SiN layer of 20 nm thickness, and measured the thermal conductivity of this SiC layer with the capping SiN layer using the TCi thermal conductivity analyzer to transiently measure the resistivity at the surface of sample after heating. We evaluated three samples: a silicon substrate as a reference sample, a SiO_2 layer with a thickness of 4 μm deposited on a silicon substrate as another reference sample, and the SiC layer and capping SiN layer on a silicon substrate as the studied sample. The thickness of the base wafer or the silicon substrate was 500 μm.

Figure 7 shows the thermal conductivity of the two reference samples and one studied sample, which were 120 W m^{-1} K^{-1} for the reference sample with the SiO_2 layer, 237 W m^{-1} K^{-1} for the studied sample with the SiC layer, and 291 W m^{-1} K^{-1} for the silicon substrate (another reference sample) without the deposited layer. According to these data, the SiO_2 layer has 40% of the thermal conductivity of the silicon substrate. Since SiO_2 hardly has very low heat conductivity,[37–40] this result is reasonable. Also, the studied sample with the SiC layer has twice the conductivity of the reference sample with the SiO_2 layer and about 80% of the thermal conductivity of the silicon substrate. Higurashi and co-workers reported that the conductivity of a SiC layer was higher than that of a silicon layer, and the thermal resistivity of a SiC layer was lower than that of a silicon layer.[41] Since a SiC layer easily conducts heat,[17] our result is also reasonable.

In a previous study, the diamond layer had thermal conductivity of 348 W m^{-1} K^{-1} and could also easily conduct heat.[21] The thermal conductivity of the studied SiC layer was not higher than that of the previous diamond

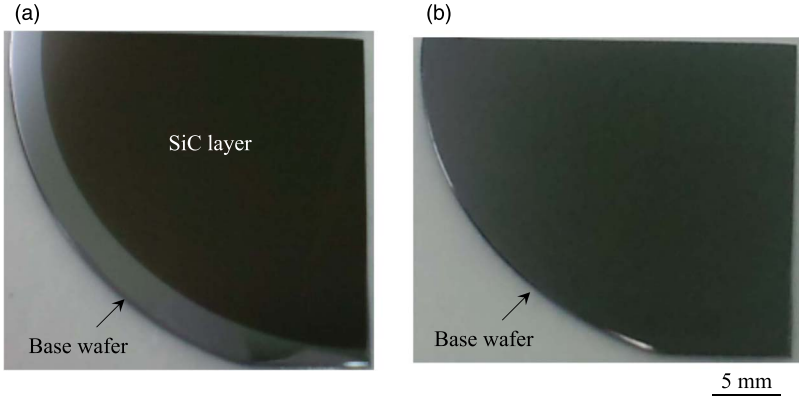

Fig. 5. Images of the surface of the SiC layer on a base wafer. (a) Before heat treatment and (b) after heat treatment.

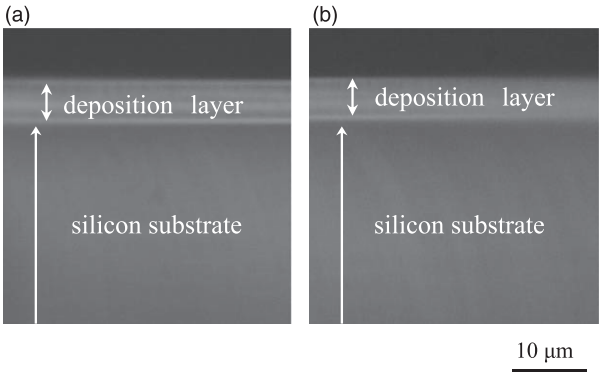

Fig. 6. Cross-sectional OM images. (a) Before heat treatment and (b) after heat treatment.

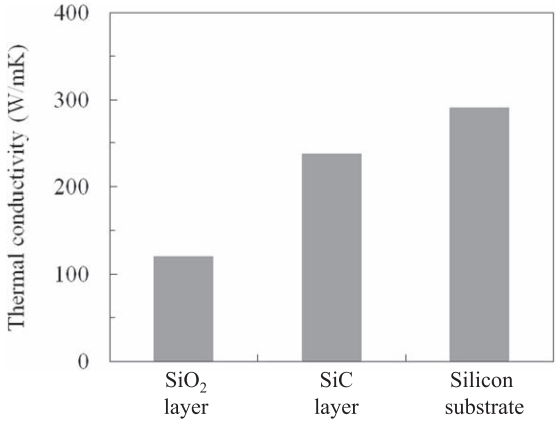

Fig. 7. Thermal conductivity of the three samples.

layer, but was higher than that of the SiO_2 layer. Therefore, we concluded that the studied SiC layer had sufficient thermal conductivity.

3.3. Evaluation and observation of voids formed when fixing silicon wafer to deposited layer of base wafer by SAB

Figure 8 shows an IR transmission image of the above-mentioned sample after SAB bonding of a silicon wafer to the polished SiC layer of 140 nm thickness with a capping SiN layer of 20 nm at room temperature and a pressure of 1×10^{-5} Pa. There were no voids with gaps larger than 200 nm in the wafer except in three regions (shown by arrows in Fig. 8); this observation method can only detect gaps larger than 200 nm. We assumed that these regions were generated by impurities on the SiC layer introduced during the polishing of the surface of the SiC layer before fixing the silicon layer to the SiC layer. The silicon layer was thus successfully fixed to the SiC layer with the capping SiN layer by SAB.

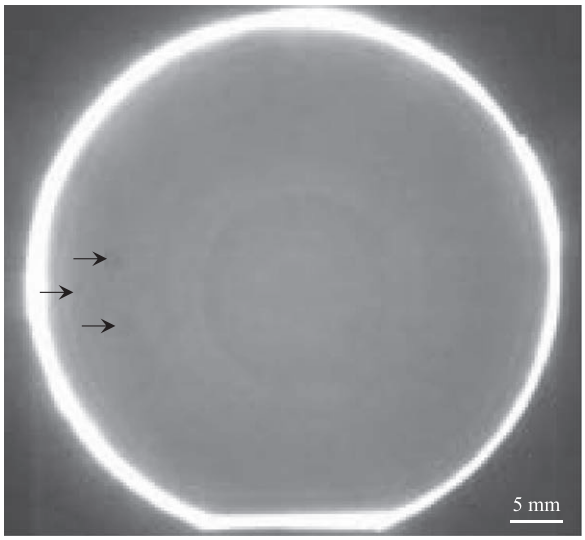

Fig. 8. IR transmission image of 2 inch wafer after bonding a silicon wafer on the SiC layer of a base wafer.

We also observed the bonded interface on a cross-sectional TEM image of the chip obtained after dicing the bonded wafer at its center [Fig. 9(a)]. The bonding surface was flat and there were no voids with gaps larger than 20 nm or defects at the bonding interface between the silicon and insulator (SiC with capping SiN) layers over a wide area.

Figure 9(b) shows a cross-sectional HR-TEM image of the same sample. There were no cavities or punch-out dislocations larger than 1 nm at the bonding interface. An amorphous layer of 10 nm thickness was observed at the bonding interface. This amorphous layer was formed by two layers of 5 nm thickness, namely, in the silicon wafer (layer) and on the SiN insulator layer. According to the SAB process illustrated in Fig. 4, argon ion sputter silicon at the surface of the silicon wafer (layer) and sputtered silicon were adsorbed on the surface of the SiN layer on the SiC layer. Suga and co-workers reported that a 4H-SiC wafer could be fixed to another 4H-SiC wafer by SAB using a silicon adhesive layer of 10 nm thickness on the SiC wafer.[42] Mu and co-workers reported that a 4H-SiC wafer could be fixed to a silicon wafer by SAB using a silicon adhesive layer of 3 nm thickness on the silicon wafer.[43] In these reports, the 4H-SiC-crystal wafer was fixed to a semiconductor substrate without voids except in the contaminated region, and the 4H-SiC-crystal wafer was fixed to the substrate using the amorphous adhesive layer containing the silicon element. Kondou and co-workers reported that a silicon wafer could be fixed to a SiN layer on a silicon wafer by SAB using an iron-containing adhesive layer of nm-orders thickness.[44] In addition, according to previous studies, SAB can fix not only crystalline materials but also noncrystalline materials.[21,31,45] Our results are thus reasonable.[24,29,30] Therefore, we concluded that a silicon wafer (layer) could be fixed to a SiC layer with a capping SiN layer of a base wafer without voids or punch-out dislocations larger than 1 nm by depositing the amorphous adhesive layer containing silicon before bonding.

3.4. Evaluation of breakdown electric field of SiC layer into SOI wafer

Figure 10 shows the breakdown electric field for the studied sample (insulator layer: SiC) and reference sample (insulator layer: SiO_2) obtained by TZDB measurement. When the leakage current through the BOX layer from the silicon layer to the silicon substrate was larger than 1×10^{-4} A cm^{-2}, the intrinsic breakdown electric field was defined to be in the C mode.

The breakdown electric field of the reference sample was 10.2 MV cm^{-1}, as illustrated by the dotted line α in Fig. 10. Since that of SiO_2 is generally 10–15 MV cm^{-1},[32] this result was reasonable. The breakdown electric field of the studied sample was 10.8 MV cm^{-1}, as shown by the solid line β in Fig. 10. This value was the same as that of SiO_2 and ten times higher than that of a polycrystalline diamond layer with high

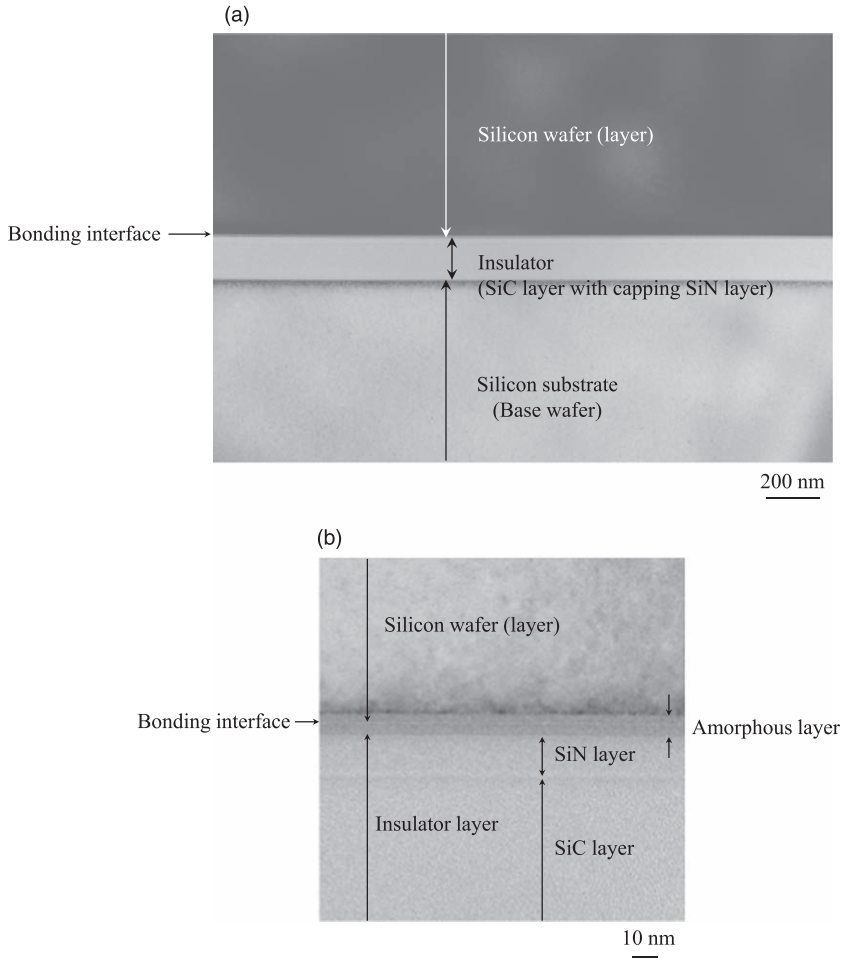

Fig. 9. Cross-sectional TEM images after bonding a silicon layer on the SiC layer of a base wafer. (a) TEM and (b) HR-TEM images.

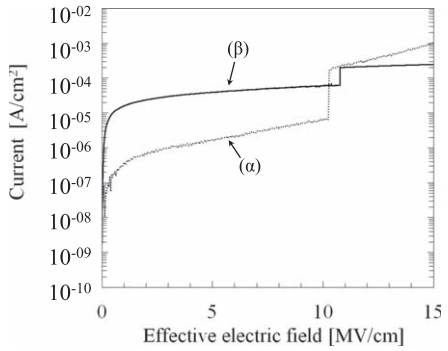

Fig. 10. TZDB measurement results for insulator layer. (α) Reference (SiO_2 layer) and (β) studied (SiC layer) samples.

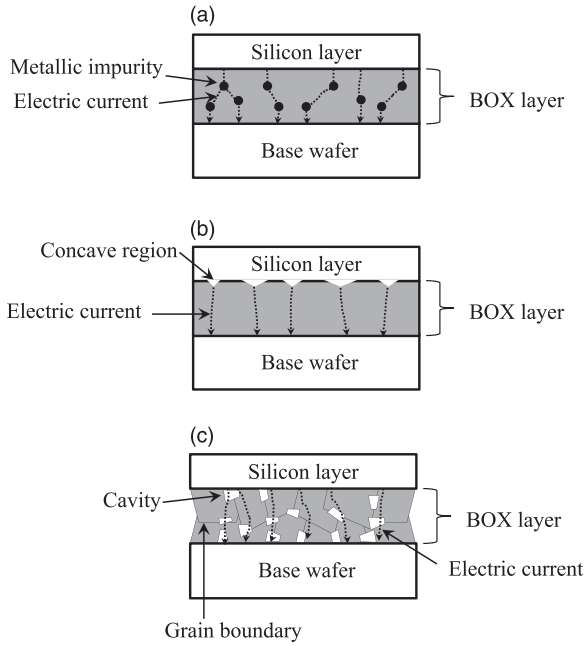

Fig. 11. Leakage current modes for isolator except intrinsic leakage current. (a) Metallic impurities contaminating an isolator layer, (b) roughening of an isolator surface, and (c) cavites and grain boundaries in an isolator layer.

thermal conductivity.[21] Therefore, we concluded that the studied SiC layer had the characteristic of an insulator with sufficient thermal conductivity for an SOI wafer.

3.5. Mechanisms of flow electric current in insulator layer

With the exception of the intrinsic leakage current of the isolator layer, leakage currents into the isolator layer are mainly generated in three modes,[46–51] as shown in Fig. 11. In the first mode [Fig. 11(a)], when metallic impurities are introduced into an isolator layer, since they act as low-resistivity spots in the isolator layer, an electric current flows in the contaminated region.[48,49] In the second mode [Fig. 11(b)], when the surface of the isolator layer is roughened, since a stronger electric field is generated in the concave regions in the roughened isolator layer, an electric current flows into the hollow regions.[50] In the third mode [Fig. 11(c)], when the cavities and grain boundaries exist in an isolator layer, since a local electric charge is generated at

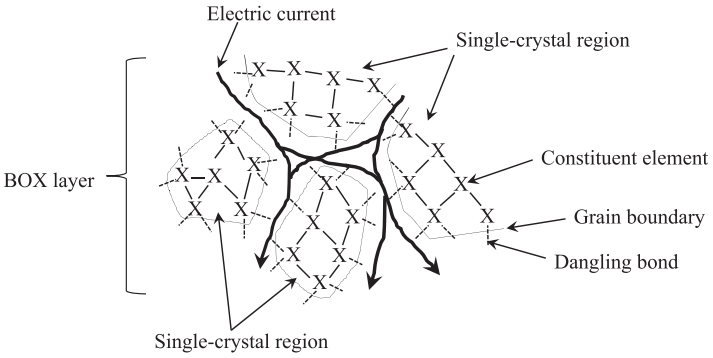

Fig. 12. Leakage current paths in the polycrystalline insulator layer.

the cavities and grain boundaries, an electric current flows near them.[51)]

In general, a SiC layer is formed as a single-crystal above 1300 °C.[22–24)] Because the SiC layer was deposited at 300 °C in this study, the deposited SiC layer was not a single-crystal layer but a polycrystalline or amorphous layer. Because there were no grain boundaries in the SiC layer, as shown in Fig. 9(b), we concluded that an amorphous SiC layer rather than a polycrystalline SiC layer was formed in the insulator layer.

When the insulator layer is polycrystalline, the leakage current in the insulator layer is lower than that in a single-crystal layer. Figure 12 shows a schematic of the leakage current paths in the polycrystalline layer. Dangling bonds are formed at grain boundaries between single crystals. Since a dangling bond has unpaired electrons and is negatively charged, electric current is generated at the dangling bonds. Thus, in terms of the insulation characteristic, a polycrystalline insulator with dangling bonds is leakier than a single-crystal insulator without dangling bonds.

We previously examined the breakdown electric field of an SOI wafer with a polycrystalline diamond layer as a wide-band-gap semiconductor material.[17)] This breakdown electric field was 1 MV cm^{-1}, which is much lower than that of a single-crystal diamond layer.[21)] The breakdown electric field of a single-crystal SiC layer is generally 2–3 MV cm^{-1}.[17)] If the studied SiC layer was polycrystalline, the breakdown electric field would have been lower than 2 MV cm^{-1}, which however, was not the case. As mentioned above, the SiC layer does not have any grain boundaries, as shown in Fig. 9(b). Therefore, we concluded that the studied SiC layer was not polycrystalline but amorphous.

On the other hand, the leakage currents of the two samples (reference and studied) were above 1×10^{-7} A cm^{-2} at 0–10 MV cm^{-1}, as illustrated in Fig. 10. We assumed that metallic impurities were introduced into the insulator layer from the deposition equipment when depositing the layer on the base wafer. The leakage current of the studied sample (insulator layer: SiC) was greater than that of the reference sample (insulator layer: SiO_2), as shown in Fig. 10. Because the PE-CVD equipment was different for the SiC and SiO_2 layers, the concentration of metallic impurities in these layers might differ and the SiC layer might have a higher concentration of metallic impurities than the SiO_2 layer. This issue can be resolved by coating the metallic components of the equipment with silica. In addition, because the temperature of the deposited SiC layer (300 °C) is lower than that of the deposited SiO_2 layer (500 °C), a SiC layer might not be as closely deposited as the SiO_2 layer. We will attempt to optimize the deposition conditions of the SiC layer above 300 °C in our future work.

4. Conclusions

We proposed a fabrication process for an SOI wafer with a SiC layer as a BOX layer with high thermal conductivity for self-heating high-voltage power and high-frequency devices. The SiC layer was formed by PE-CVD at 300 °C for a short time, and a silicon layer was fixed to the deposited SiC layer by SAB at room temperature in an ultrahigh vacuum without thermal stress. The thermal conductivity of this deposited SiC layer was twice that of a SiO_2 layer, and the breakdown electric field of this layer was 10–11 MV cm^{-1}, the same as that of a SiO_2 layer. In addition, the bonding interface had no voids or punch-out dislocations after bonding a silicon layer to the deposited SiC layer as an insulator layer. Therefore, this SOI wafer has high thermal conductivity, and we conclude that it will be useful for the fabrication of next-generation self-heating power and high-frequency devices.

Acknowledgments

This work was conducted at Kitakyushu Foundation for the Advancement of Industry, Science and Technology, Semiconductor Center, supported by "Nanotechnology Platform Program" of the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan, Grant No. JPMXP09F19FA0024. We thank Mitsubishi Heavy Industries Machine Tool Co., Ltd. for the support in the bonding process, and Mr. Shuzo Takeuchi of Fuzzy Logic Systems Institute for help in TEG fabrication. We also thank Dr. Hisashi Furuya and Mr. Naoki Ikeda of SUMCO for management support and helpful discussion.

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