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# Investigation of interface state density near conduction band edge of 4H-SiC MOSFET based on inversion capacitance and drain-current characteristics

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We propose a simple method to evaluate interface state density ($D_{it}$) near the conduction band edge of 4H-SiC MOSFETs, which is difficult to observe by conventional methods although it degrades device characteristics. We focus on a capacitance–voltage method with inversion capacitance, applying high voltage to a set reference point where almost all traps are occupied and sweeping downward gradually. Our method is applicable for mass production because of the convenient sequence. We also demonstrate that the device characteristics calculated based on the extracted $D_{it}$ are in good agreement with the measured characteristics. © 2020 The Japan Society of Applied Physics

## 1. Introduction

Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) have been recognized as next-generation power devices[1–4] and circuit elements that can be used in harsh environments, i.e. high temperatures[5–8] and high radiative conditions.[9–12] To design a circuit with SiC devices, a device model is needed. However, it is difficult to substitute the conventional model because the interface trap density, $D_{it}$, of SiC MOSFETs is too large.

Conventionally, the high–low method,[13,14] conductance method,[15,16] Gray–Brown method[17–19] and capacitance–surface-potential method[20,21] have been used to measure $D_{it}$ with accumulation capacitance. The measurable energy range is 0.2–0.6 eV, whereas shallower traps that were not obtained by the above-mentioned methods would dominate the on-state characteristics of SiC MOSFETs.

The recent progress with Hall measurement has made it possible to evaluate such shallow traps. Saku et al. pointed out that the density of free electrons, $n_{free}$, is not equal to the total density of inversion layer electrons, $n_{total}$, if a substantial amount of the electrons in the inversion layer are trapped. Therefore, the effective mobility, $\mu_{eff}$, is also not equal to the actual electron mobility, $\mu_n$.[22] Hatakeyama et al. measured the dependency of the ratio of $n_{free}$ and $n_{total}$ on the post-oxidation annealing time in nitric oxide at 1250 °C.[23] These methods make it possible to estimate the fundamental properties of the $SiO_2$/SiC interface.[24–26]

However, Hall measurement is not suitable for wafer-level testing in mass production. To provide device models for design circuits, the development of a simpler measurement technique is required.

We focused on the difference between shallow and deep traps. Generally, shallow traps originate from the physical properties of SiC, e.g., atomic staking configuration[27] or carbon-related defects,[28] and their density is typically greater than that of deep traps. In terms of the device characteristics, deep and shallow traps influence subthreshold and on-state characteristics, respectively. The former can cause the hysteresis effect due to its long time constants and prevents us from obtaining the correct measurement results. Therefore, we set the initial gate bias large enough to invert the channel sufficiently and to occupy all traps. Then the gate voltage is swept gradually so as not to cause fluctuation of the trapped charge from deep level traps in the capacitance–voltage ($C$–$V$) and $I_d$–$V_g$ measurement. By suppressing the hysteresis effects, we estimated the $D_{it}$ with inversion capacitance of a 4H-SiC n-channel MOSFET in p-well, though an MOS capacitor on n-substrate was used conventionally. Consequently, we obtained shallower $D_{it}$.

We showed the relationship of $D_{it}$ with the $C$–$V$ curve and $I_d$–$V_g$ curve in "Ref. 29") By using this method, shallow traps would be easily measurable once we had obtained the correct $C$–$V$ curve. In this report, we will give the detail of our model and demonstrate a simple and proper measurement method for shallow interface traps and their impact on device characteristics.

We evaluated the validity of our measurement method by the quasi-static C–V (QSCV) method. Then we estimated $D_{it}$ with the results of QSCV. Finally, we measured and calculated $I_d$–$V_g$ characteristics using the Pao–Sah double integral (PSDI).

## 2. Fabrication and experimental method

A lateral n-channel SiC MOSFET was fabricated by the following process. P-well regions were formed by ion implantation, $N_a = 4 \times 10^{17}\,cm^{-3}$, on an n-type 4H-SiC (0001) substrate. Then, p-type and n-type contact regions were formed. The acceptor and donor ions were Al and N, respectively. They received 50 nm thick gate oxide deposited by chemical vapor deposition. Post-oxidation annealing was conducted in a nitric-oxide-containing atmosphere. The phosphorus-doped n-type gate poly-Si was deposited and patterned. Electric contact between the substrate and the metal electrode was made. Channel length and width were 100 $\mu$m and 200 $\mu$m, respectively.

We measured the $C$–$V$ curve by the QSCV method with Keysight B1500A semiconductor device analyzer. Hold and integration time were 1 s and 40 ms, respectively. We also measured the $I_d$–$V_g$ characteristics with 4156C semiconductor parameter analyzer, $V_d = 50$ mV. As to the gate voltage, two ways were tested, from +20 V to −20 V and from −20 V to +20 V. For $V_g = +20$ V, the MOSFET is in the on-state so that the conduction band edge of the SiC approaches the Fermi level. Therefore, the evaluated energy range was low, between about 0.05 eV and 0.2 eV.

 

The theoretical $C$–$V$ curve was calculated by[30)]

$$C_s(\psi_s, N_a, T) = \frac{dQ_s(\psi_s, N_a, T)}{d\psi_s} \quad (1)$$

$$C_g(\psi_s, N_a, T) = \frac{C_{ox} C_s(\psi_s, N_a, T)}{C_{ox} + C_s(\psi_s)} \quad (2)$$

$$V_g = \psi_s + \varphi_{MS} - \frac{Q_s(\psi_s, N_a, T) + Q_{ox}}{C_{ox}} \quad (3)$$

where $C_s$ is the SiC capacitance per area, $\psi_s$ is the surface potential, $N_a$ is the acceptor density, $T$ is the temperature, $C_g$ is the gate capacitance of MOSFET per area, $C_{ox}$ is the gate oxide capacitance per area, $V_g$ is the gate voltage, $\varphi_{MS}$ is the work function difference between poly-Si and SiC and $Q_{ox}$ is the equivalent oxide charge. We fitted the measurement results of the QSCV characteristic, $C_{QS}$, with fitting parameters, $N_a$, $Q_{ox}$ and $C_{ox}$. We also calculated the flat band voltage with them in advance for the $D_{it}$ estimation.

Then, we calculated $D_{it}$ with[31)]

$$D_{it} = \frac{C_{QS}(\psi_s) - C_s(\psi_s)}{q^2} \quad (4)$$

where $q$ is elementally charged. $\psi_s$ was for $C_{QS}$ estimated with

$$\psi_s(V_g) = \int \left(1 - \frac{C_{QS}(V_g)}{C_{ox}}\right) dV_g + A \quad (5)$$

where $A$ is an integral constant which was determined so that $\psi_s = 0$ V at flat band voltage.

For the following calculation of $I_{ds}$, we supposed that $D_{it}$ was described as[32)]

$$D_{it} = D_{it}^{mid} + D_{it}^{edge} \exp\left(\frac{E - E_c^{T_0}}{\sigma}\right). \quad (6)$$

Then we fitted $D_{it}$ with $D_{it}^{mid}$, $D_{it}^{edge}$ and $\sigma$.

Next, we calculated the $I_d$–$V_d$ characteristic with PSDI:

$$I_{ds} = \pm q\mu \frac{W_g}{L_g} \int_0^{V_{ds}} \left( \int_\delta^{\psi_s} \frac{\left(\frac{n_i^2(T)}{N_a}\right) e^{\frac{q(\psi - V)}{k_B T}}}{E(\psi, V_d, T)} d\psi \right) dV \quad (7)$$

where $\mu$ is the channel motility, $W_g$ is the gate width, $L_g$ is the gate length and $E$ ($\psi$, $V_d$, $T$) is the electric field in the gate oxide. Gate voltage was

$$V_g = \psi_s + \varphi_{MS} - \frac{Q_s(\psi_s) + Q_{ox}}{C_{ox}} - \frac{qN_{it}(\psi_s, T)}{C_{ox}} \quad (8)$$

$$N_{it} = \int_{E_i}^{E_c} D_{it}(E) f(E, T) dE \quad (9)$$

where $E_i$ is the intrinsic Fermi level, $E_c$ is the conduction band energy, $f(E, T)$ is the Fermi–Dirac distribution, $T$ is the temperature and $N_{it}$ is the total number of interface traps.

In our model, once we obtain $D_{it}$ distribution in proper measurement, we can incorporate $D_{it}$ effect for $I_d$–$V_g$ calculation with Eqs. (8) and (9). For the calculation of $I_{ds}$, we used $N_a$ and $Q_{ox}$ from the QSCV result as constant values. Then we fitted the measured $I_{ds}$ by $\mu$ in the on-state region. In this study, we adjusted $D_{it}^{mid}$ and $D_{it}^{edge}$ by a constant factor.

Finally, we estimated the trapped charge by interface trap sites by the gate-voltage shift, $\Delta V_g$, on $I_d$–$V_g$ characteristics.

$$\Delta V_g = \frac{qN_{it}}{C_{ox}}. \quad (10)$$

## 3. Results

Figure 1 plots the QSCV measurement results with down-sweep. All $C$–$V$ characteristics matched each other. On the other hand, Fig. 2 shows those results with up-sweep. For reference, it also plots the result with down-sweep from 20 V to −10 V as shown by the broken line. These depended on the initial negative gate voltage. Particularly for $V_g < -3.0$ V, $C$–$V$ characteristics shifted negatively, while they were consistent with each other for $V_g > -3.0$ V.

To clarify what type of charge caused the hysteresis in the QSCV measurement, we calculated the energy band diagram at the SiC/$SiO_2$ interface. Figure 3 shows the calculated energy diagram. As shown by the blue broken line, $E_i = E_F$ at the $SiO_2$/SiC interface ($x = 0$) for $V_g = -2.5$ V. Figure 3 also plots $E_i$ for $V_g = -5.0$ V, as shown by the red line and supposed distribution of donor-like and acceptor-like states. Donor-like states upper $E_F$ were positively charged. These charges caused a negative shift of $C$–$V$ characteristics because they have a long time constant. It is worth pointing out that we could eliminate the hysteresis by applying high voltage and by sweeping downward gradually.

Figure 4 plots the measurement result of QSCV with down-sweep and the calculation result. Both results were in good agreement with each other. This is the second reason why the down-sweep measurement is the correct way for SiC MOSFETs.

In the region labeled (a), the measurement results were exclusively fitted by $C_{ox}$. In region (b), we fitted the slope by $N_a$ and $Q_{ox}$. Then we obtained integral constant $A$ in Eq. (5) so that $\psi_s = 0$ V at flat band voltage. If the gate voltage swept upward in this region, hysteresis prevented us from fitting and obtaining those parameters.

Extracted parameters were $C_{ox} = 6.80 \times 10^{-8}$ F cm$^{-2}$ (gate oxide thickness, $t_{ox} = 49.5$ nm), $N_a = 4.00 \times 10^{17}$ cm$^3$ and $Q_{ox}/q = 3.10 \times 10^{12}$ cm$^2$.

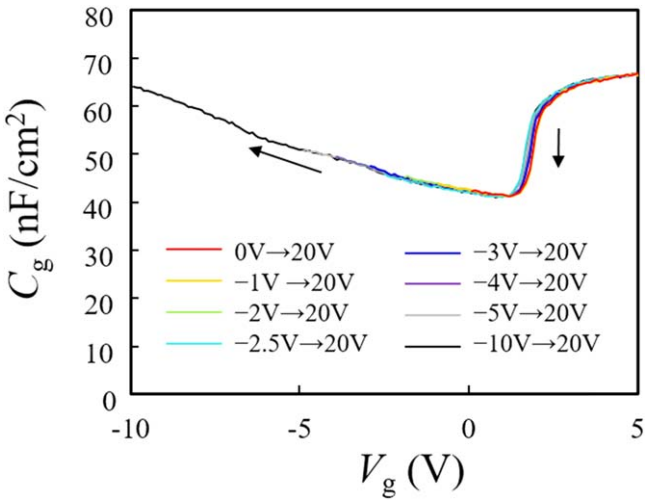


**Fig. 1.** (Color online) QSCV results by down gate sweep. All $C$–$V$ characteristics matched each other.

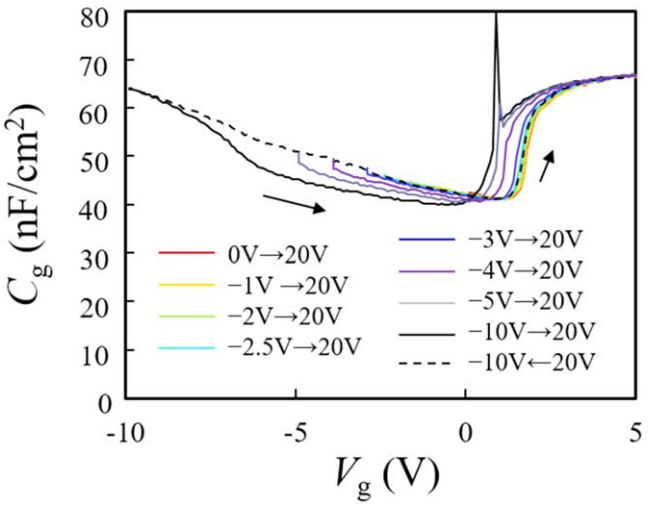


**Fig. 2.** (Color online) QSCV results by up gate sweep. It also plots the result with down-sweep from 20 V to −10 V (broken line).

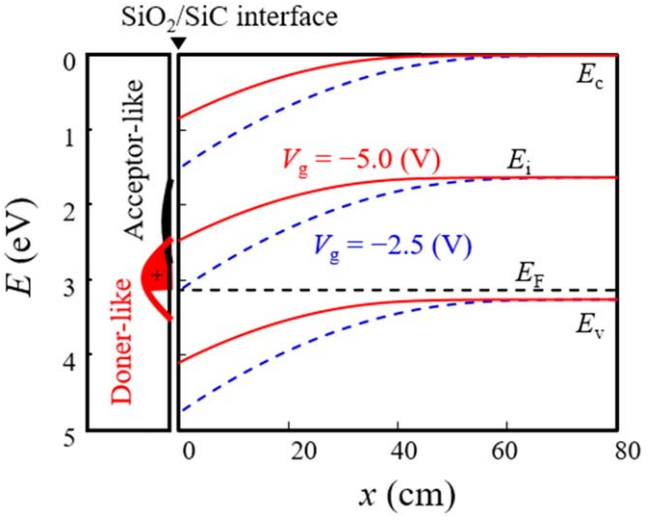


**Fig. 3.** (Color online) Calculated energy diagram and supposed distribution of mid-gap traps for $V_g = -5.0$ V. Donor-like state upper $E$F was positively charged.

In the region labeled (c), the measured $C$–$V$ curve was broadened in the positive direction because the negative trapped charges due to the interface trap states shifted the

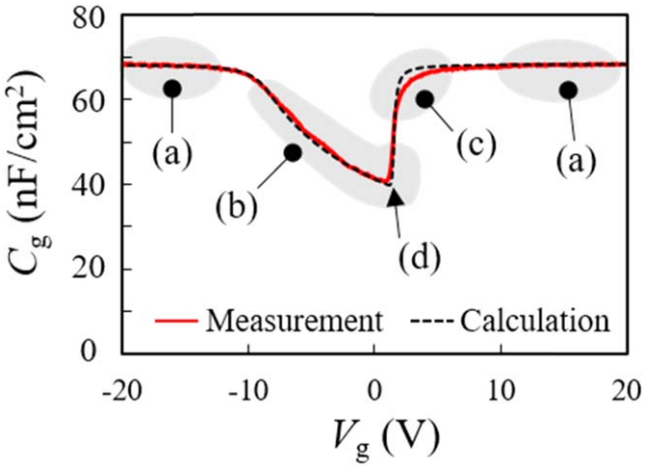


**Fig. 4.** (Color online) $C$–$V$ characteristics of n-channel MOSFET.

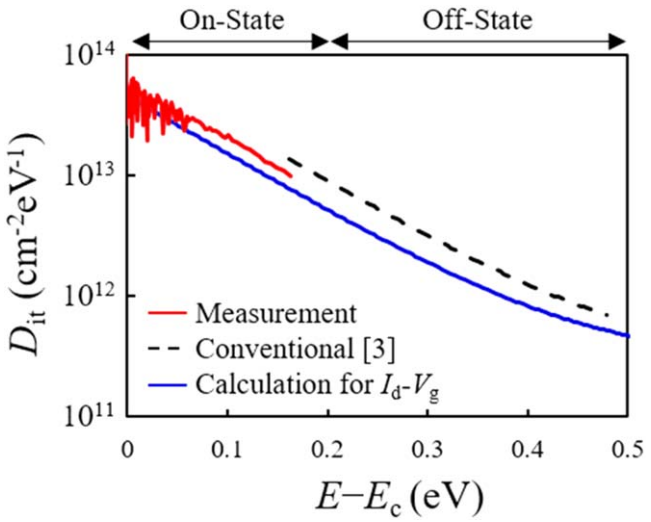


**Fig. 5.** (Color online) $D$it distribution calculated by the $C$–$V$ method with inversion capacitance of an n-channel MOSFET.

gate voltage. We calculated $D_{it}$ by these differences between measurement and calculation results with Eqs. (4) and (5).

Figure 5 shows the estimated $D_{it}$ distribution. We measured shallower interface trap density than the conventional method. It was in the order of $10^{13}$. These huge amounts of $D_{it}$ affect device characteristics.

We calculated $I_d$–$V_g$ characteristics with $D_{it}$ based on QSCV results and Ref. 3 using Eq. (6). Figure 5 also plots $D_{it}$ distribution for $I_d$–$V_g$ calculation as shown by the blue line. The fitting parameters were the following: $\mu = 22\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, $\sigma = 0.07$ eV, $D_{it}^{mid} = 3.0 \times 10^{11}\,\mathrm{cm^{-2}\,eV^{-1}}$ and $D_{it}^{edge} = 4.5 \times 10^{13}\,\mathrm{cm^{-2}\,eV^{-1}}$.

Figure 6 shows the calculation and measurement results of the $I_d$–$V_g$ characteristic (black circle and red solid line, respectively). Both characteristics were consistent with each other from the subthreshold region to the on-state region. This indicates the validity of the estimated $D_{it}$ because deep and shallow level traps affect the former and latter, respectively.

Then we estimated that total trapped charge at the SiC/SiO$_2$ interface for $V_g = 20$ V with Eq. (9) and the gate voltage shift with Eq. (10). The results were $N_{it} = 4.9 \times 10^{12}\,\mathrm{cm^{-2}}$ and $\Delta V_g = 11.5$ V, respectively. This

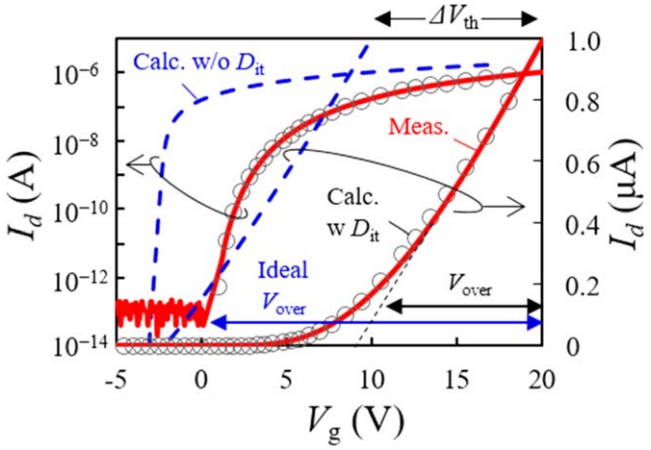


**Fig. 6.** (Color online) Measurement and calculation result of $I_d$–$V_g$.

indicates that such a huge gate voltage shift occurred in strong inversion.

To estimate the amount of $D_{it}$ effect, we also calculated the $I_d$–$V_g$ characteristic without interface traps, as shown by the blue broken line. The difference in subthreshold voltage, $V_{th}$, between the red and blue line was about 12 V. This is almost the same value of estimation by QSCV, $\Delta V_g = 11.5$ V.

The consistency of these two results indicates the validity of our method. In addition, our method gave an insight into the overdrive voltage, $V_{over}$, which is defined from subthreshold to gate-source voltage ($V_{over} = V_{gs} - V_{th}$). According to our calculation, ideal $V_{over}$ was about 20 V. On the other hand, measured $V_{over}$ decreased to about 10 V. It is, indeed, almost half of the ideal value. Consequently, huge $D_{it}$ at $SiC/SiO_2$ caused the degradation of device characteristics.

## 4. Conclusions

We estimate interface trap density by QSCV measurement with an n-channel SiC MOSFET. Sweeping $V_g$ downward from high voltage avoided hysteresis effects due to the mid-gap state and gave us the distribution of the shallow traps at 0.2 eV energy depth from the conduction band edge, which was of the order of $10^{13}$. We demonstrated that this huge amount of interface traps caused the gate overdrive voltage degradation in $I_d$–$V_g$ characteristics. Because the proposed method is so simple that it can be used for wafer-level testing in mass production, it will open up new opportunities to improve device performance and circuit operation.


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