Comparison of SOI FinFETs and Bulk FinFETs

Invited Paper

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The scaling-down of MOSFETs is strongly required to achieve high integration density and performance. However, in the sub-50 nm regime, the scaling of conventional planar MOSFETs has been facing problems such as threshold voltage (V_{th}) lowering, subthreshold swing (SS) degradation, drain-induced barrier lowering (DIBL), fluctuation of device characteristics with random channel dopant, leakage increase due to dielectric tunneling, and band-to-band tunneling at the junction.

To solve these problems, several device structures have been proposed: thin-body silicon-on-insulator (SOI) MOSFETs [1], double-gate MOSFETs [2], triple-gate MOSFETs [3], and FinFETs [4],[5]. Among these structures, FinFET is considering a promising candidate for ultimate CMOS device structure because the device has robustness against short channel effect (SCE), higher current drivability, nearly ideal subthreshold swing (SS), and mobility enhancement [6]. FinFETs are classified into two types: SOI and bulk FinFETs. Fig. 1 shows 2-D cross-sectional views of SOI FinFET and bulk FinFET, respectively. H_g, W_{fin}, and T_{ox} represent the gate height, fin width, and gate oxide thickness, respectively. Bulk FinFETs have shown several advantages over SOI FinFETs while keeping nearly the same scaling-down characteristics as those of SOI FinFETs. The several advantages of bulk FinFETs are low cost, low defect density, no floating-body effect, high heat transfer rate to the substrate, and nearly the same process flow as conventional bulk CMOS technology. Compared to bulk FinFETs, SOI FinFETs could suppress any possible leakage between source and drain through the fin body below the channel fin, and has low source/drain to substrate capacitance so that speed characteristics could be better. Recently, body-tied FinFETs (bulk FinFETs) built on bulk silicon (Si) wafer have been demonstrated experimentally and studied [7],[8]. The bulk FinFETs could be applied to dynamic random access memory (DRAM), static random access memory (SRAM), and flash memory devices [9]-[11]. FinFET application to high-speed logic is found in [12].

Several figures are prepared to compare both FinFETs with the same geometry and doping. Fig. 2 shows the V_{th} and DIBL of n-type FinFETs versus the W_{fin}. The SS characteristics are shown in Fig. 3. The bulk FinFETs (solid circles) have nearly the same V_{th} and DIBL characteristics as those of SOI FinFETs (open circles), which guarantees good scalability of the bulk MOSFETs. Fig. 4 shows device temperature versus gate bias at a given V_{DS} of 0.9 V. The bulk FinFET with W_{fin} of 20 nm shows much lower device temperature than the 30 nm SOI FinFET.

We will show further data on both FinFEETs by introducing device simulation and fabrication, V_{th} modeling, reliability, and compact I-V models. In this work, both SOI and bulk FinFETs are investigated in terms of scalability, fundamental characteristics, and application area. FinFETs have side channel, which has a sort of double-gate nature, and top channel. Analysis on these channels will be given and I-V model also will be introduced. We will briefly address key factors in device fabrication, the dilemma and prospect of FinFETs.

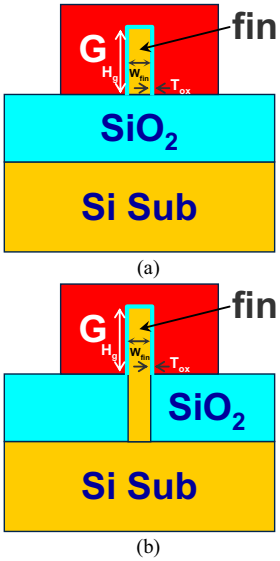

Fig. 1. 2-D cross-sectional view. (a) SOI FinFET. (b) Bulk FinFET.

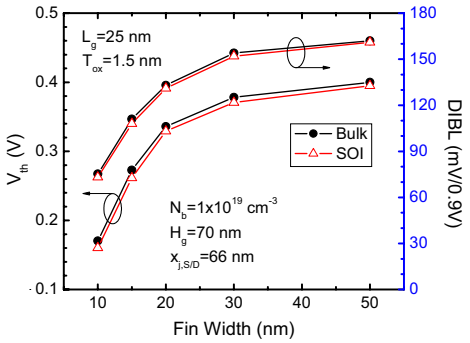

Fig. 2. V_{th} and DIBL charactersitics of bulk and SOI FinFET versus W_{fin}. The n$^+$ poly Si gate was applied.

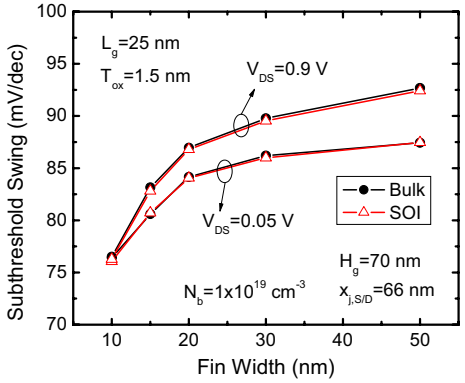

Fig. 3. SS characteristics versus W_{fin} for bulk and SOI FinFET as a function of V_{DS}.

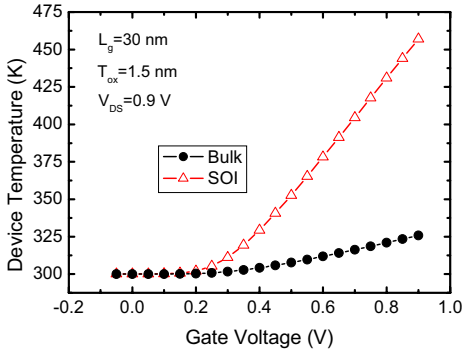

Fig. 4. Temperature characteristics of bulk and SOI n-type FinFET versus V_{GS}. The results were obtained through 3-D device lattice temperature simulation.

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