Review of Some Critical Aspects of Ge and GeOI Substrates

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This paper is a review of the different types of Germanium (Ge) and Ge On Insulator (GeOI) substrates, their critical aspects and their main applications.

Substrates for Ge bulk channel devices

Two types of pure Ge substrates are studied nowadays: Bulk wafers and thick Ge epitaxial layers on Silicon (Ge/Si).

Ge Bulk Substrates (GBS). Today, the best crystalline quality Ge wafers in the market are GBS with an Etch Pit Density (EPD) said to be 0 counts/cm² [1]. Those wafers are commercially available, with different doping types, levels and orientation. However, both economical reasons (Ge is a rare material: around 5E-4 % of the earth's crust [2]) and technical reasons (Ge is 2.5 denser than Si and suffers from mechanical weakness; the handling of Ge wafers can thus be an issue) may be a limitation to the use of these substrates for the micro-electronics mass market.

Ge/Si substrates (GSS). The other type of Ge substrates is epitaxial (GSS). They are obtained through an epitaxy of Ge on Si. Due to the 4.2% lattice parameter mismatch between Ge and Si, the critical thickness for plastic relaxation is reached after a few nm of Ge, limit at which dislocations appear. The two techniques used to obtain such substrates with reduced TDD (Treading Dislocations Density) call upon either thick SiGe buffers or low temperature / high temperature growth strategies. The first one uses a $Si_{1-x}Ge_x$ graded buffer (with x varying from 0% up to 100% at roughly 10% per µm) on top of which a pure Ge layer is grown, leading to more than 10µm thick stacks [3]. The second technique requires the stacking of a high growth temperature Ge layer on top of a low growth temperature Ge layer, itself on Si (001), with some subsequent thermal cycling [4], leading to a less than 3µm thick epitaxial layer. The TDD obtained with these two techniques is between 1^E6 and 1^E7 per cm². The GSS, due to their Si like mechanical behavior and their reduced cost (compared to GBS and graded buffer substrates), are attractive. However, the impact of their high TDD values has yet to be evaluated on device performances and may lead to a poor manufacturing yield. Thus, their uses will probably be limited to R&D.

Germanium On Insulator Substrates

GeOI substrates benefit from both bulk Ge properties (transport properties, lattice parameter) and "On Insulator" advantages (for microelectronic applications: better electrostatic control i.e. less short channel effect, reduced junction capacitances and lower substrate coupling in RF). Another main advantage of GeOI substrates is the limited quantity of Ge used to obtain such a substrate but also its mechanical behavior, which is close to the one of a Si wafer. In this section, we will describe the four main types of GeOI substrates.

GeOI by layer transfer. The most commonly used technique is the Smart Cut ™ which was developed first on Si [5] and then applied to numerous materials such as Ge [6]. 200mm GeOI substrates with Ge layers thinner than 100nm were obtained starting with either GBS or GSS. p-MOSFETs devices were formed on these substrates, leading to functional devices. The measured performances (μ_h=120cm²/V/s on GeOI with GSS donor) [7] are promising and will be improved when both the substrates and the devices become mature. An advantage of this technique is the recycling of the donor wafer which can be used several times.

GeOI by Condensation. Since 2003, the use of the Ge condensation technique, in order to make GeOI substrates, has been studied by several teams in the world [8] [9]. p-MOSFETs realized on such substrates exhibit a 1600cm²/V/s hole mobility [10]. This performance is due to both the use of Ge and of strain induced by the Ge condensation technique. This technique is appropriate to obtain thin and localized Ge films particularly adapted to microelectronic applications. The main limitation of the Ge condensation approach are its thermal budget (more than 3 h. at 1050°C) and process induced damage such as dislocations generated when exceeding the critical thickness for plastic relaxation during Ge enrichment.

GeOI by liquid Phase Epitaxy (LPE). The LPE of Ge was presented by Liu [11] in 2004. Since the fusion temperature of Ge (937°C) is substantially smaller than for Si (1415°C), LPE is adapted to obtain GeOI. In [11], p-MOSFETs exhibit 120cm²/V/s hole mobility for 22nm thick Ge layer with TDD ~1E4 /cm². The main interests of this technique come from its reduced thermal budget (950°C, a few sec.) and its potential ability to transfer the crystalline orientation of the seed region to the Ge layer (realization of 6° axis twisted GeOI templates for GaAs grow). Limitations of LPE are the integration density (the seed region is a lost space) and the control of the thermal flow during crystallization (heat must be evacuated by the seed region even for long active areas).

GeOI by Bond and etch back technique (B-GeOI). This technique consists in the bonding of a Ge donor wafer (GBS or GSS) on top of a Si wafer via oxide layers. Then the Ge wafer is etched and polished to the desired thickness. Today, due to CMP non uniformity, the Ge layers cannot be thinner than 2µm. Such substrates are thus adapted to applications requiring thick Ge layers. However, during the etch back step, the donor wafer is lost, which is a drawback of B-GeOI.

Ge and GeOI main applications

The study of High K on Si CMOS devices has given a leverage to Ge based devices as a current booster for MOSFETs [12]. This material is also suitable for GaAs epitaxy (solar cells or HBT applications) or for CMOS / opto-electronics co-integration. Moreover, Ge and GeOI substrates are promising material for a monolithical integration of CMOS and Ge IR photodiodes.

Conclusion

In this paper, we reviewed the different types of Ge and GeOI substrates and showed their advantages and limitations, which is an important consideration to be taken into account to determine which substrates are suitable for which application.

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