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Perspective—Opportunities and Future Directions for Ga_2O_3

Opportunities and Future Directions for Ga_2O_3

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The β-polytype of Ga_2O_3 has a bandgap of ∼4.8 eV, can be grown in bulk form from melt sources, has a high breakdown field of ∼8 $MV.cm^{-1}$ and is promising for power electronics and solar blind UV detectors, as well as extreme environment electronics (high temperature, high radiation, and high voltage (low power) switching. High quality bulk Ga_2O_3 is now commercially available from several sources and n-type epi structures are also coming onto the market. There are also significant efforts worldwide to grow more complex epi structures, including β-$(Al_xGa_{1x})_2O_3/Ga_2O_3$ and β-$(In_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures, and thus this materials system is poised to make rapid advances in devices. To fully exploit these advantages, advances in bulk and epitaxial crystal growth, device design and processing are needed. This article provides some perspectives on these needs.

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Properties of Ga_2O_3 that make it attractive for power electronics and solar blind UV photodetectors.—Most applications for semiconductor electronic devices are classified as high-speed or high-power. A rough guide to this application space is given in Figure 1 as a two-dimensional slice in power-frequency. The power axis is a function of current and voltage handling capability as well as reliability (ruggedness and thermal considerations), performance (linearity, efficiency), size, cost and legacy.[1] The applications for Ga_2O_3 include power electronics, solar blind UV detectors and gas sensors.

Schottky diodes, used in switches or rectifiers, have high switching speed but tend to have high leakage in the reverse-biased off-state. Increasing the thickness or decreasing the doping in the drift region increases the breakdown voltage but also increases the on-resistance,

$$R_{on-sp(ideal)} = \frac{W_D}{q\mu_n N_D} = \frac{4(V_B)^2}{\varepsilon_s E_c^3 \mu_n},$$

where V_B is the breakdown voltage and E_c is the critical field for avalanche breakdown in a particular semiconductor. The denominator in this equation, which is also the Baliga figure of merit, is exceptionally high in Ga_2O_3.

Several figures of merit (FOM) are listed in Table I. The large bandgap of Ga_2O_3 allows high temperature operation and the large critical field allows high voltage operation (relative to maximum breakdown). Additionally, Ga_2O_3 has a high saturation electron velocity ($v_{sat} = 2 \times 10^7$ cm/s), which is partially accountable for the high current density, I_{max} ($I_{max} \approx qn_s v_{sat}$ where $q = 1.6 \times 10^{-19}$ C, n_s = sheet charge density, v_s = electron saturation. velocity), and potentially high operating frequency as $f_t \approx v_{sat}/L_{eff}$.

The high-power/high-voltage market is primarily served by Si and SiC devices. Ga_2O_3 is the leading candidate to address the ultra-high power market (>1 kW). The open question is how quickly will the Ga_2O_3 substrate cost decrease and size increase, thus enabling Ga_2O_3 devices to compete with SiC Schottky and Si-LDMOS in the medium to high power market.

The main market segments for high-power, high-frequency transistors are defense and military applications (radar, jamming, countermeasures, guided weapons), wireless infrastructure (3G, 3G+, WiMAX/LTE base stations and backhaul), and broadcast and communication satellites (SatCom). The relatively low thermal conductivity, λ, of Ga_2O_3 creates self-heating effects that must be mitigated in order to utilize Ga_2O_3 in high-frequency devices.

Current Status

What is needed to advance insertion of Ga_2O_3 in applications? *Bulk and epi growth (crystal quality, doping, heterostructures).*—Bulk, insulating or conducting β-Ga_2O_3 crystals can be grown by edge-defined film-fed (EFG) growth using Ir crucibles, by Czochralski or by float zone and are commercially available.[2–4] Each has advantages and limitations, but to date, each has proven capable of producing high quality crystals. EFG substrates with excellent transparency and uniformity are commercially available in up to 2" sizes,[2] with demonstrations at 4" and 6" plates in development, as shown in Figure 2.[2] The 10 × 15 mm^2 substrates are available in three orientations, namely (⁻201), (010) and (001) while the larger circular substrates are available only in the (⁻201) orientation. The wafers contain no twin boundaries.[2]

There has also been progress in development of epi growth by a number of techniques, including MOCVD, HVPE and MBE with

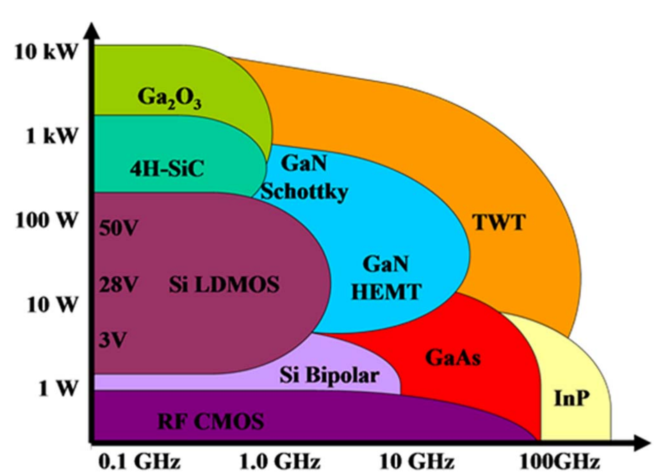

Figure 1. Power - frequency diagram of the application space for several semiconductor materials. At extremely high power and/or frequency, vacuum electronics, e.g., traveling wave tubes, are still implemented; however, Ga_2O_3 will overtake much of this application space.

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Table I. Normalized unipolar power-device figures of merit. The Johnson and Baliga figures of merit are exceptionally high for Ga_2O_3.

	Si	GaAs	4H-SiC	GaN	Ga_2O_3	Notes
Bandgap E_g [eV]	1.12	1.42	3.25	3.4	4.85	
Dielectric constant, ε	11.8	12.9	9.7	9	10	
Breakdown field, E_c [MV/cm]	0.3	0.4	2.5	3.3	8	
Electron mobility, μ [$cm^2/V \cdot s$]	1500	8500	1000	1250	300	
Maximum velocity, Vs [10^7 cm/s]	1	1	2	3	2	1.8 ⟨0 0 1⟩ and ⟨0 1 0⟩, 2.0 ⟨0 1 0⟩
Thermal conductivity, λ, [W/cm · K]	1.5	0.5	4.9	2.3	0.23	0.13 W/cm · K ⟨1 0 0⟩, 0.23 W/cm · K ⟨0 1 0⟩
Figure of merits / relative to Si						
Johnson = $E_c^2 \cdot V_s^2/4\pi^2$	1	1.8	277.8	1089.0	**2844.4**	power-frequency capability
Baliga = $\varepsilon \cdot \mu \cdot E_c^3$	1	14.7	317.1	846.0	**3214.1**	specific on-resistance in (vertical) drift region
Combined = $\lambda \cdot \varepsilon \cdot \mu \cdot V_s \cdot E_c^2$	1	3.7	248.6	353.8	37.0	combined power/frequency/voltage
Baliga high frequency = $\mu \cdot E_c^2$	1	10.1	46.3	100.8	142.2	measure of switching losses
Keyes = $\lambda \cdot [(c \cdot V_s)/(4\pi \cdot \varepsilon)]^{1/2}$	1	0.3	3.6	1.8	0.2	thermal capability for power density / speed

controlled n-type doping over the range 10^{15}–10^{19} cm^{-3} using Sn or Si shallow donors.[1,5–8] HVPE is probably the most developed at this point, but requires subsequent polishing to provide an acceptable morphology. The dislocation density of current bulk wafers is of order 10^3 cm^{-2}, a key result for making large area power rectifiers and the n-type doping is stable against annealing.[2] Progress in bulk and n-type epi films has been impressive, with future need for development of coherent β-$(Al_xGa_{1x})_2O_3$/Ga_2O_3 and β-$(In_xGa_{1-x})_2O_3$ heterostructures.[9] The solubility limit of Al_2O_3 in β-Ga_2O_3 is ∼65% in the range 850–1950 °C and for MBE growth temperatures (600–800 °C), the solubility limit of Al_2O_3 in β-Ga_2O_3 is drastically reduced due to the formation of a $AlGaO_3$ intermediate compound.[9] This necessitates use of high oxygen fluxes during MBE to achieve high growth rate. Similar limitations will be encountered in MOCVD and HVPE growth and exploration of optimized growth conditions and the role of strain and extended defects is an important area of future research.

For p-type doping, there have been no reports on achieving conductive material with acceptors,[10] due to their predicted large ionization energies, presence of common n-type impurities and native defects and the resulting n-type background conductivity that must be overcome. This will require a systematic measurement of the ionization energies of candidate acceptors (by optical methods initially) and a better understanding of the compensation by native point defects and their complexes plays an important role in influencing the efficiency of doping in Ga_2O_3 and related alloys. These compensating centers may be native defects or complexes from either sublattice or simply impurities. At high enough levels, the doping itself might induce self-compensation. This is a common phenomenon in other compound semiconductors where the formation energy of acceptor-like vacancies in n-type material decreases as the Fermi level rises closer to the conduction band edge. The understanding of native defects in Ga_2O_3 is far from complete and has been largely driven by first principal calculations using different approaches.[11] The formation energy of these defects is generally dependent on the Fermi level.

Processing (ohmic and Schottky contacts, implant doping and isolation, controlled low damage dry etching and wet etching, gate dielectrics, surface passivation).—Many very promising Ga_2O_3-based power rectifiers, MESFETs, MOSFETs and even finFETs have been reported,[1,10–20] along with various types of solar blind photodetectors.[21,22] Another limitation is the lack of high quality patterning, doping and contacting processes that exist for the more mature semiconductors.[23] High quality ohmic contacts are a prerequisite for any device and should provide low contact resistance at moderate anneal temperatures. Additional contact resistance leads to slower device switching speeds as well as reliability issues due to local contact heating during current flow during device operation. Etching is needed for intra-device isolation or for exposing layers for subsequent contacting. Ion implantation can be used for channel/contact region doping and device isolation where planarity requirements preclude the use of mesa etching. The other major issue is the limited and anisotropic thermal conductivity of Ga_2O_3 (0.27 $W.cm^{-1}$ K^{-1} for [010] and 0.11 $W.cm^{-1}$ K^{-1} for [100]),[10] which might be addressed using heatsinks like diamond or microfluidic approaches or transfer to a metal substrate, all currently being developed for GaN electronics. However, the lower thermal conductivity of Ga_2O_3 relative to other wide bandgap materials means these techniques must be even more

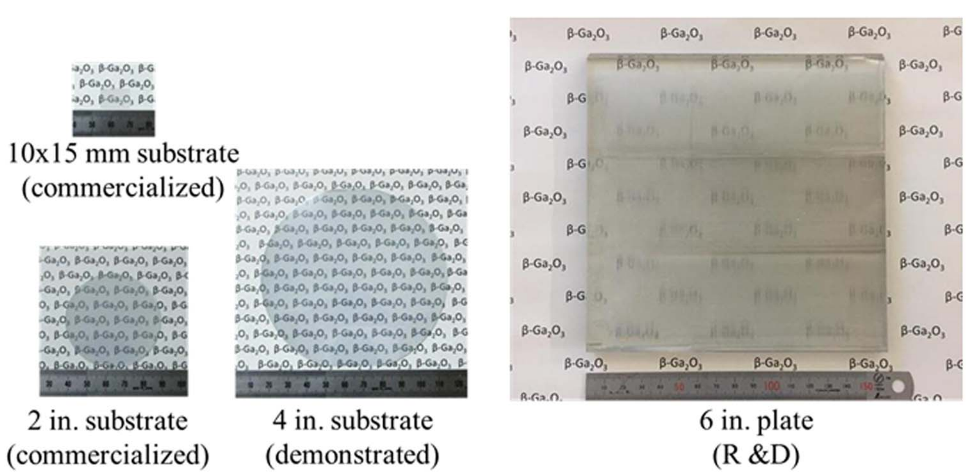

Figure 2. Status of edge-fed-grown bulk Ga_2O_3 wafer size. Currently, 2″ diameter crystals are commercially available, while 4″ diameter substrates and 6 × 6 ″ plates have been demonstrated or in development, respectively.

effective. For this reason, Ga_2O_3 is projected for high voltage, lower current applications than GaN.

Contacts on n-Ga_2O_3.—The usual approaches involve surface etching or cleaning to reduce barrier height or increase of carrier concentration of the surface through preferential loss of oxygen.[10,12,23–25] To date, contact schemes involving IZO or dry etching in BCl_3/Ar to enhance the surface n-type conductivity, followed by Ti/Au annealed at 500°C have been common. Specific contact resistances of ~4.6–8 $\times 10^{-6}\ \Omega \cdot cm^{-2}$ were reported for Ti/Au contacts on n-Ga_2O_3 epitaxial layers in which Si was implanted and annealed at 925°C, followed by dry etching, metal deposition and annealing at 470°C.[23,24] Many published I-V characteristics are only quasi-linear at low current and shows the need for improved contact approaches. Cr has a low work function of 4.5 eV and is currently one of the best choices for ohmic contacts on n-Ga_2O_3.

For an n-type semiconductor, to achieve an ohmic contact means that the work function of the metal must be close to or smaller than the electron affinity of the semiconductor (affinity of β-Ga_2O_3 is ~4.00 ± 0.05 eV),[25] and thus potential choices if the surface is unpinned include Hf (work function 3.9 eV), Sc and La (both 3.5 eV) and Gd (2.9 eV). Bilayers of these with Au should reduce the contact sheet resistance. The transport mechanisms in the contacts can be determined by temperature-dependent TLM measurements. A traditional ohmic contact follows a thermionic field effect (TFE) or field-effect (FE) depending on the semiconductor effective doping and/or temperature. No significant dependence of the contact resistance on measurement temperature would indicate the dominant transport mechanism is field emission.

Dry etching.—Wet etchants have been reported for Ga_2O_3, including HNO_3/HCl, H_2SO_4, H_3PO_4 and HF-based solutions,[26–28] but little is known about its dry etching characteristics and the associated mechanisms and effects on the properties of the material. Plasma chemistries of Cl_2/BCl_3 for reactive ion etching and BCl_3, BCl_3/SF_6, and CF_4/O_2 for inductively coupled plasma conditions showed generally low etch rates.[29,30] Plasma-induced damage in Ga_2O_3 is found to increase the conductivity of the near surface and lead to improved n-type ohmic contact resistivities, as was the case in the early days of GaN technology. Other options include methane/hydrogen (CH_4/H_2) and mixed Cl_2/H_2 or $BCl_3/Cl_3/H_2$ chemistries. It needs to be established whether they are ion-driven or have a significant chemical etch component. In etching processes occurring by ion-enhanced sputtering in a collision-cascade process, the etch rate will be proportional to $E^{0.5}$-$E_{TH}{}^{0.5}$, where E is the ion energy and E_{TH} is the threshold energy.

Implantation doping/isolation.—Implant isolation is a method of using ion implantation of either electrically inactive or deep level impurities to produce electrically insulating regions that can be used for inter-device isolation. It has a major advantage over mesa isolation of maintaining a planar surface. It has not yet been investigated in Ga_2O_3.

Similarly, little is known about the electrical properties of implanted dopants in Ga_2O_3, especially for p-type doping. For n-type doping, Si, Ge and Sn are donors if incorporated on the Ga site.[21,23] Conversely, the column V elements should be acceptors if incorporated on the O site. Of course, their energy level in the gap determines whether they are shallow or deep and therefore whether they are significantly ionized at room temperature even if they are soluble on the appropriate lattice site. The systematics of damage recovery and substitutionality of the implanted dopant still need much work in Ga_2O_3.[31]

Gate dielectrics and surface passivation.—There are three main criteria that a gate dielectric for Ga_2O_3 must possess. First, it must be thermodynamically stable with the semiconductor and not react during processing. Secondly, it should have a high quality interface with low defect and trap density to ensure high carrier mobility. Finally, it must have sufficient band offsets (typically >1 eV for both conduction and valence band offset) to act as barriers to both electrons and holes. The device performance depends strongly on the type of band alignment, and on the band offsets. The wide bandgap of Ga_2O_3 limits the available choices of gate dielectrics to those with bandgaps >6 eV (eg. SiO_2, Al_2O_3, $HfSiO_4$, Y_2O_3, La_2O_3, $LaAlO_3$) and it will also be necessary to establish the type of band alignments: type I, type II staggered, type III broken gap. If the offsets are not large enough, the dielectric may still be used as a surface passivation layer to protect the surface of Ga_2O_3 from the instabilities induced by exposure to atmosphere. Measurements of band offsets are in their early stages.[32] To date, Al_2O_3, SiO_2 and HfO_2 have been used in metal-oxide-semiconductor (MOS) structures on Ga_2O_3. The process and etch conditions for patterning the dielectrics also need to be established

Role of H in Ga_2O_3.—There is interest in the properties of hydrogen in Ga_2O_3, because of the predictions from density functional theory and total energy calculations that it should be a shallow donor.[33] The generally observed n-type conductivity, therefore, may at least in fact be explained by the presence of residual hydrogen from the growth ambient, rather than to native defects such as Ga interstitials or O vacancies. In some related oxides, oxygen vacancies may even be deep donors. There is some experimental support for the fact that hydrogen may be a shallow donor in Ga_2O_3 from experiments on its muonium counterpart and from electron paramagnetic resonance of single-crystal samples.[34]

Modelling.—In terms of projected devices utilizing Ga_2O_3, the high fields and potentially high temperatures in some of the intended applications are beyond the capabilities of current device models. Device design simulators should include high fields and high temperatures as early as possible so that they can provide accurate guidance. The monoclinic crystal structure has different symmetry than the GaN hexagonal or GaAs zincblende lattices most commonly simulated. The Ga_2O_3 has lattice constants of a = 12.23 Å, b = 3.04 Å, c = 5.80 Å and two types of two kinds of coordination for Ga^{3+} ions in the structure, namely distorted tetrahedral and octahedral, meaning the oxide ions are in a distorted cubic closest packing arrangement, and the gallium (III) ions in the two types of sites have Ga-O bond distances of 1.83 and 2.00 Å, respectively.

Future Needs and Prospects

Work where research will produce the greatest benefits.—

(i) Heterostructure (β-$(Al_xGa_{1x})_2O_3/Ga_2O_3$ and β-$(In_xGa_{1-x})_2O_3$) growth on single crystal Ga_2O_3 substrates, including nucleation for homoepitaxy, characterization of substrate surface, change in growth morphology with orientation and better understanding of carrier transport across heterojunctions, improved understanding of epitaxy (is non-equilibrium growth needed for high acceptor incorporation?)
(ii) Better understanding of dopants and defects, lattice location of dopants and understanding the role of native defects such as oxygen vacancies and their role in residual conductivity relative to extrinsic impurities such as hydrogen and silicon.
(iii) Continued development of high quality bulk crystals of large diameter.
(iv) Role of hydrogen in passivating/compensating acceptors or in enhancing incorporation of acceptors.
(v) Sensitivity of Ga_2O_3 surfaces to adsorbed oxygen and water vapor needs to be established.
(vi) Radiation damage effects in Ga_2O_3 and related heterostructures.
(vii) Band offsets of candidate dielectrics for MOS devices, as well as process /patterning and contacting conditions
(viii) Thermal management approaches for power devices.

Conclusions

More attention needs to be paid to optimizing the buffer layers and crystal quality of Ga_2O_3 and related heterostructures and this should emphasize use of MBE and MOCVD growth methods which allow for better stoichiometry control and higher purity and also allow for taking advantage of the high quality bulk substrates now available. Device performance will be improved with development of better contacts, patterning and doping processes.

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