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A New Instability in MOS Transistor Caused by Hot Electron and Hole Injection from Drain Avalanche Plasma into Gate Oxide

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Results of an experimental study are reported of a new instability found in p- and n-channel MOS transistors. This phenomenon is that when a higher voltage in an excess of a brakdown voltage is applied to the drain electrode the breakdown voltage drifts to a higher value and the drain current also increases. The origin of this instability is investigated by extensive measurements and analyses of the electrical characteristics of the transistors. It is concluded that 1) the semiconductor surface near the drain becomes p-like in the p-channel transistors and n-like in the n-channel transistors and thus the active channel length is shortened, 2) this is caused by charging of the gate oxide due to injection of electrons or holes generated during the drain avalanche breakdown, and 3) electron and hole injection is much affected by electric field across the oxide over the drain junction.

§ 1. Introduction

This paper is concerned with instability of drain currents and avalanche breakdown voltages in MOS transistors. This instability is entirely different from the well-known instability of the gate threshold voltage that is caused by the migration of ions in the silicon dioxide in the direction perpendicular to the semiconductor surface and, in particular, accelerated by so-called bias-temperature treatments with positive bias to the gate electrode. We have found that when we keep applying a higher voltage to the drain electrode in an excess of the breakdown voltage, the breakdown voltage drifts gradually to a higher value. After the drift of the breakdown voltage the drain current at low drain voltages is observed to have also increased.

Gurtler[1] has already reported on the drift of the breakdown voltage in planar passivated p-n junctions that the drift is observed only in p^+-n junctions and that it originates mainly in the migration of the positive charge in the silicon dioxide over the junction in the direction parallel to the semiconductor surface. In our experiments, however, the drift of the breakdown voltage and also the increase in the drain current are observed in both p- and n-channel transistors which have p^+-n and n^+-p junctions, respectively, although the amount is usually less in the n-channel case than in the p-channel case.

In this paper we describe results of extensive measurements and analyses concerning this type of instability appearing in both p- and n-channel transistors. Measurement items include drain saturation current, inversion voltage, C-V characteristics, source-drain conductance in the nonsaturation region and breakdown voltage.

Our overall conclusion derived from analyses of the data is that this type of instability comes from charging of the gate oxide by the electron or hole injection into the gate oxide during the avalanche breakdown.

§ 2. Sample Preparations

Experimental MOS transistors were fabricated on 5 Ω cm n-type and 1, 10 and 100 Ω cm p-type silicon wafers of a (100) orientation. The first oxide film was grown at 1145°C in steam to a thickness of 1 μm. The source

and drain islands were diffused with boron or phosphorus. For the diffusion source of boron BBr_3 was used in most of the samples but BN was also used in some samples in order to check whether possible introduction of Br into the gate oxide near the source and the drain regions has any effects. In the *n*-channel transistors the diffussion source is always $POCl_3$. The gate oxide was grown in the same ambient as that in the first oxide growth and was doped with phosphorus. The film thickness is about $0.2\,\mu$m. The gate electrode is aluminum.

Prior to the experiments we confirmed from results of so-called bias-temperature treatments that ions in the gate oxide do not migrate in the direction normal to the surface under gate voltages and temperatures used in the present experiments.

§ 3. Experimental Results and Analyses

In the present study, we apply two tests (tests A and B) to the transistors at room temperature leading to the drift of the breakdown voltage and the change in the drain current: In test A a high test voltage, V_a, enough for the breakdown is applied to the drain electrode, connecting the source and gate electrodes to the substrate. In test B it is applied both to the source and to the drain with respect to the gate and the substrate. In these tests, we keep applying a test voltage until a breakdown voltage drifts to the test voltage. When the original breakdown voltage is -40 V and the test voltage is -50 V, for example, it takes about ten seconds to drift the breakdown voltage to -50 V.

After test A or B we always observe not only the increase in the drain current but also the increase in the drain conductance in the saturation region (the slope of the drain current). This fact can be well understood if one assumes that the channel becomes shorter after test A or B.

In order to investigate this problem and to elucidate its origin, measurements were made of the drain saturation current, inversion voltage, *C-V* characteristics, source-drain conductance and breakdown voltage before and after test A or B. The results of the measurements and analyses will be described in order in the following subsections.

3.1. *Drain saturation current*

The increase in the drain current after test A was found to occur more remarkably in narrower-channel transistors. For example, the drain saturation current, $I_{D,SAT}$, is increased by around 30 % after applying -70 V to the drain in the *p*-channel transistors with a channel length of $4\,\mu$m. In the case of a channel length of $200\,\mu$m the increase amounts to less than 1 %. We also observed that test B gave rise to a larger increase in $I_{D,SAT}$ than test A. In order to compare the increases in $I_{D,SAT}$ after tests A and B, we measured $I_{D,SAT}$ at a gate voltage of -7 V before and after tests A and B by using twenty *p*-channel transistors with the narrow channel length ($\sim 4\,\mu$m) fabricated on one wafer. When the test voltage is -70 V, the increases in $I_{D,SAT}$ amount to 34 % in test A and 100 % in test B as average. If we ascribe these increases only to narrowing of the channel, the channel length are calculated to be reduced by 25.4 % for test A and by 50 % for test B. The latter value is just twice as large as the former within the experimental accuracy as one expects. In the *n*-channel case we also obtained a similar result but the amount of the change is much smaller than in the *p*-channel case.

3.2. *Inversion voltage*

Effects of tests A and B on the inversion voltage, V_T, were examined. The inversion voltage, V_T, is defined as the voltage intercept of the plot of $I_{D,SAT}^{1/2}$ *versus* the gate voltage, V_G, (see Figs. 1 and 2). In all the samples we have tested, test A yields no detectable change in V_T. Typical results are shown in Figs. 1 and 2. Test B also shows no effect on V_T in most of the samples, but in few ones it leads to a small decrease in the absolute value, as shown in Fig. 2. No increase in $|V_T|$ has been observed.

The inversion voltage, V_T, which we have measured is the minimal gate voltage required to invert the whole semiconductor surface between the source and the drain. The surface states at the silicon-silicon dioxide interface and ions in the oxide do not always distribute uniformly along the region from the source to the drain and thus the inversion voltage may not be constant everywhere. Thus the inversion voltage, V_T, defined above is the highest one somewhere in the channel

region.

It is very likely from the experimental conditions and results that the inversion voltage is changed only in the region where the avalanche breakdown takes place. Even in test B the avalanche breakdown is confined within the narrow regions near the source and the drain and does not take place throughout the channel region, in the present experimental transistors even with the narrowest channel length (4 μm) under the experimental conditions (see also sec. 3.4).

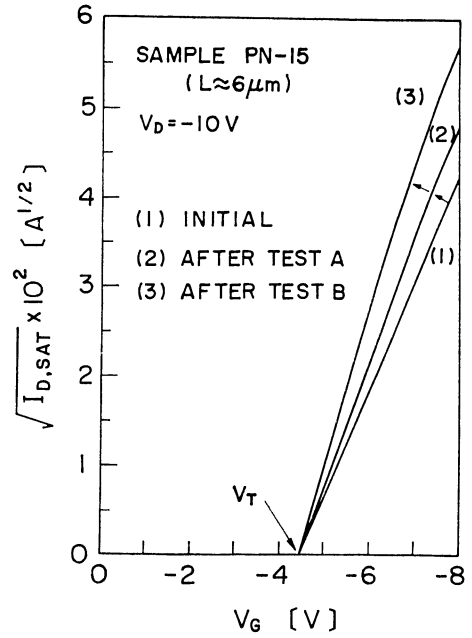


Fig. 1. Plots of square root of drain saturation current, $I_{D,SAT}$, against gate voltage, V_G, before and after test A and B for a p-channel transistor. Test voltage $V_a=-70$ V.

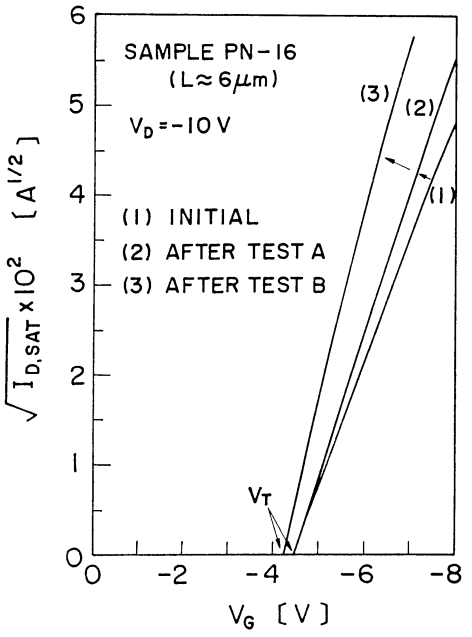


Fig. 2. Plots of square root of drain saturation current, $I_{D,SAT}$, against gate voltage, V_G, before and after test A and B for a p-channel transistor. Test voltage $V_a=-70$ V.

Now we consider two cases: 1) the case when the inversion voltage for the central channel region is higher than or equal to the ones at both the end-sides of the channel, and 2) the case when the inversion voltage for the region near the source or near the drain is higher than the one for the central channel region. In the first case the inversion voltage, V_T, defined above is not changed by tests A and B, even if the inversion voltage for the region near the source or the drain is decreased. This corresponds to the results for most of the samples. In the second case, if the inversion voltage near the source or the drain is decreased by test A or B, its change is detected after test A or B. If the decrease is not detected after test A but detected after test B, it follows that the inversion voltage near the source was highest before the tests and it was decreased by test B. This corresponds to the result for sample PN-16. It is concluded from these considerations that by test B in which the avalanche breakdown takes place in both the source and the drain junctions the inversion voltage near the source and the drain is decreased, and also by test A the inversion voltage near the drain is decreased.

3.3. *C-V characteristics*

In order to look into the probable change in the channel length more explicitly, we measure gate capacitance *versus* voltage, C_G *vs* V_G, characteristics in the p-channel transistors with a narrow channel length of 6 μm. A typical result is shown in Fig. 3. Note that the rapid increase in C_G near zero gate bias comes from the capacitance of the diode provided between the gate and the substrate for protection against electric breakdown of the gate oxide.

It is obvious in Fig. 3 that the minimal capacitance is increased after test B and is larger for larger test voltages, but the volt-

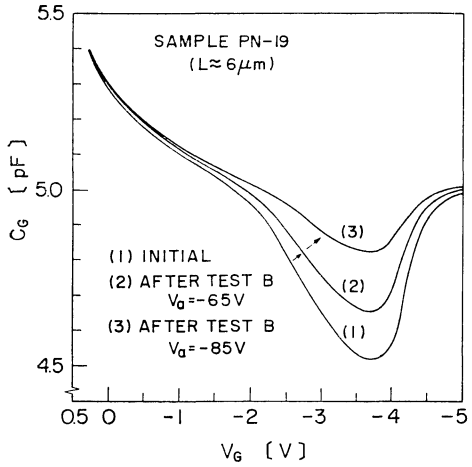


Fig. 3. Plots of gate capacitance, C_G, as a function of biasing gate voltage, V_G, before and after test B for a p-channel transistor. The source and the drain are connected to the substrate.

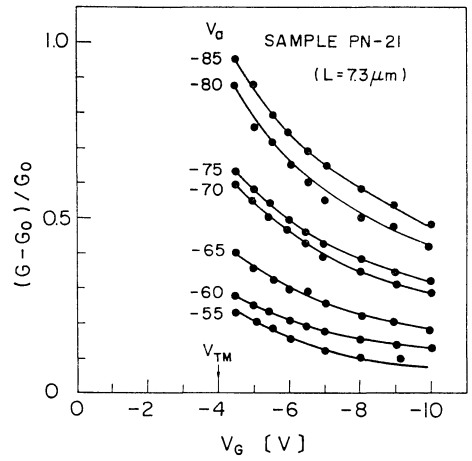


Fig. 4. Change in source-drain conductance as a function of gate voltage, V_G, by test B of various test voltage, V_a, for p-channel transistor PN-21. G_0 is the initial conductance and G is the one after the test. Solid lines are those calculated from eq. (7) using the values of D and V_{TP} plotted in Figs. 7 and 8.

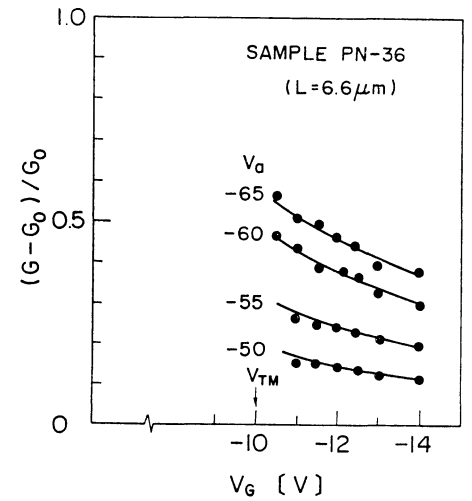


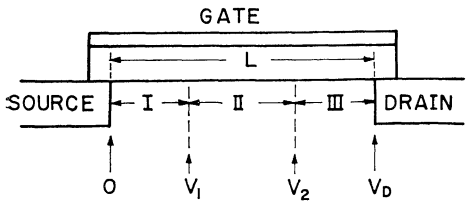
Fig. 5. Change in source-drain conductance as a function of gate voltage, V_G, by test B of various test voltage, V_a, for p-channel transistor PN-36 containing a considerable amount of sodium ions in the gate oxide. Solid lines are those calculated from eq. (7) using the values of D and V_{TP} plotted in Figs. 7 and 8.

age of the minimal capacitance remains unchanged. The minimal-capacitance voltage must be the one corresponding to the central channel region, as in the case of the inversion voltage described in 3.2. The increase in minimal capacitance is most probably due to reduction of the area of the central channel region. This means that the semiconductor surface near the source and the drain would have become p-like after test B.

3.4. *Inversion voltage near the source and the drain*

In order to evaluate the changes in the inversion voltage and the channel length, we have measured the source-drain conductance in the nonsaturation region as a function of the gate voltage.

In Figs. 4 and 5, the results of the measurement of two p-channel transistors are shown. In these figures G_0 is the initial source-drain conductance and G is the one after test B. Sample PN-21 (Fig. 4) is a standard transistor with V_T of -4 V. Sample PN-36 (Fig. 5) is a special one with V_T of -10 V, in which intentional sodium ions were introduced into the gate oxide by dipping the wafer into a 0.1 % NaCl solution before Al evaporation. For analyzing the data, a simple model shown in Fig. 6 will be used for the transistor subjected to test B. Two regions, I and III, with the same length of D near the source and the drain, respectively, are the regions where the inversion voltage has been changed by test B. A central region, II, with an inversion voltage, V_{TM}, is assumed not to be affected by test B. We further assume that the inversion voltage, V_{TP}, is same in both regions I and III and uniform within each the potetials at region. V_1 and V_2 are the potentials at the two boundaries between I



	CHANNEL LENGTH	INVERSION VOLTAGE
I	D	V_{TP}
II	L-2D	V_{TM}
III	D	V_{TP}

Fig. 6. A shematic model of potential and inversion voltage distributions in a MOS transistor after test *B*.

and II and between II and III, respectively.

We calculate the channel conductance using this model. Before test B, drain current, I_D, at a low drain voltage, V_D, is given by

$$I_D=B\frac{1}{L}V_D(V_G-V_{TM}), \qquad (1)$$

where B is a geometrical factor of the transistor. The initial conductance, G_0, is then,

$$G_0=B\frac{1}{L}(V_G-V_{TM}). \qquad (2)$$

After test B, the drain current flowing through the three regions is expressed by

$$I_D=B\frac{1}{D}V_1(V_G-V_{TP}); \text{ in region I,} \qquad (3)$$

$$I_D=B\frac{1}{L-2D}(V_2-V_1)(V_G-V_{TM}); \text{ in region II,} \qquad (4)$$

and

$$I_D=B\frac{1}{D}(V_D-V_2)(V_G-V_{TP}); \text{ in region III.} \qquad (5)$$

From eqs. (3), (4) and (5) the source-drain conductance, G, is obtained as follows:

$$G=B\frac{(V_G-V_{TP})(V_G-V_{TM})}{2D(V_G-V_{TM})+(L-2D)(V_G-V_{TP})}. \qquad (6)$$

From eqs. (2) and (6) we obtain,

$$\frac{G_0}{G-G_0}=\left[\frac{1}{2}\left(\frac{L}{D}\right)\frac{1}{V_{TM}-V_{TP}}\right]V_G - \left[1+\frac{1}{2}\left(\frac{L}{D}\right)\frac{V_{TP}}{V_{TM}-V_{TP}}\right]. \qquad (7)$$

The right-hand side of eq. (7) consists of the two terms linearly dependent on and independent of the gate voltage. Rearranging the results in Figs. 4 and 5 by taking the inverse of the vertical coordinate and comparing them with eq. (7), we determine the values of V_{TP} and D. The results are shown in Figs. 7 and 8. It is remarkable that the values of V_{TP} and D are both almost same for two samples PN-21 and PN-36 in spite of the different values of the initial inversion voltage (V_{TM}). V_{TP} varies from the negative to positive values with increasing test voltage. This indicates that negative charges are induced and reside in the oxide near the the source and the drain after test B. Assuming that the change in the inversion

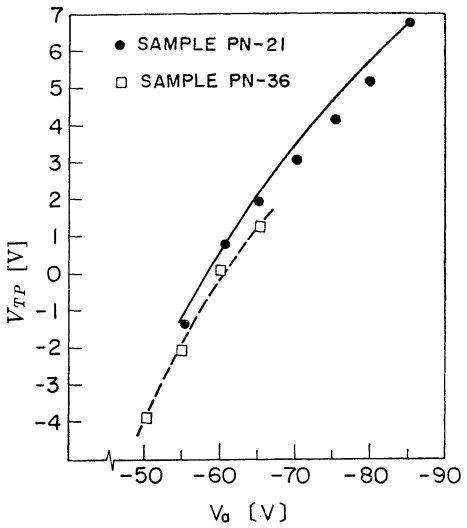


Fig. 7. Plots of inversion voltage, V_{TP}, near source and drain as a function of test voltage, V_a, for p-channel transistors.

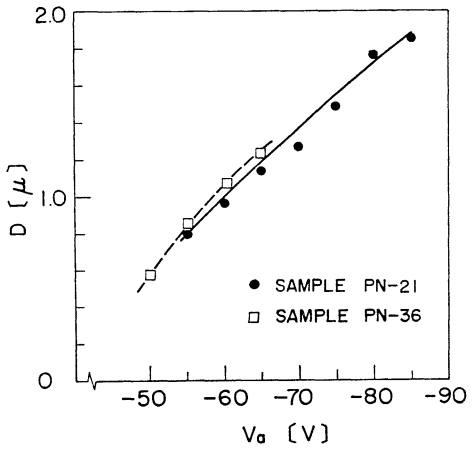


Fig. 8. Plots of changed channel length, D, against test voltage, V_a for p-channel transistors.

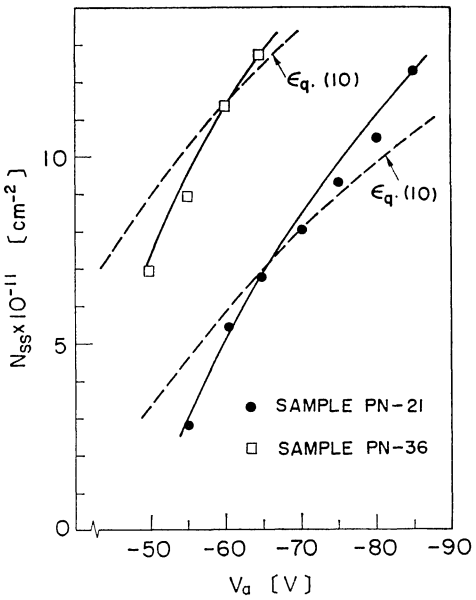


Fig. 9. Plots of introduced negative charge concentration, N_{SS}, as a function of test voltage, V_a. Dotted lines are those calculated from eq. (10) using the values of D shown in Fig. 8.

voltage, V_{TP}, near the source and the drain are all caused by introduction of the negative charge into the oxide, we calculate the amount of the negative charge, $-qN_{ss}$, from $V_{TP}-V_{TM}$. The result is shown in Fig. 9. This figure shows the relation between the charge in the oxide and breakdown voltage, since the test voltage corresponds to the breakdown voltage after the test. On the other hand, if we assume a cylindrical field distribution in the depletion region, we can roughly estimate the drift of the breakdown voltage, ΔV_B, from D and N_{ss} by using the next equation:

$$\Delta V_B \approx \frac{1}{\varepsilon_s} \cdot \frac{\pi}{2} \cdot D \cdot qN_{ss}\,, \qquad (10)$$

where ε_s is the dielectric constant of the semiconductor. The results calculated for samples PN-21 and PN-36 are shown with the dotted lines in Fig. 9, which are in good agreement with the observed ones.

For the negative charge in the oxide we investigate here possible responsibility of impurities with negative charge which may be introduced into the oxide in the fabrication process and may migrate to the oxide near the source and the drain. We consider the following three species: 1) Cl^- coming from $POCl_3$ used in the process of the growth of the phosphosilicate glass on the gate oxide, 2) Br^- coming from BBr_3 used for the diffusion source and 3) OH^- coming from room air. The first and second species can be excluded, since we found the same degrees of the drift of the breakdown voltage and the change in the drain current for the transistors fabricated by using BN for the diffussion source in place of BBr_3 and not doped with phosphorus. In addition we could not detect Cl in the phosphosilicate glass and Br on the silicon surface just after the diffusion process by mass spectrographic analysis within an experimental accuracy of 0.1 ppm. In order to look into the effect of the third one, we heated a p-channel transistor at 300°C for 5 hrs in vacuum, cooled it to room temperature and measured the drift of the breakdown voltage and the change in the drain current, holding the sample in vacuum. The results are entirely similar to those for the untreated transistors. Thus we cannot take for the negative charge in the oxide Cl^-, Br^- or OH^- coming from room air.

3.5. *Breakdown voltage*

It is known that the avalanche breakdown voltage depends largely on the gate voltage.[2] It takes a high or low value according as the gate voltage is in the range of inverting or accumulating the semiconductor surface. This dependence of the breakdown voltage has been considered to come from the following: 1) the change in the minimal drain voltage required to form the depletion region between the drain and the channel region, and 2) the change in the length of the depletion region, which is closely related to the maximum value of the electric field in the depletion region. What we are now interested in is not the value of the breakdown voltage itself but differences in the drift of the breakdown voltage that arise when the depletion region length is changed. We measured the drift of the breakdown voltage in three cases of high positive, zero and high negative gate voltages. In Figs. 10(a) and (b) we show the results for the p-channel transistors. When we measured the breakdown voltage, we applied high voltages to both the source and the drain simultaneously in order to avoid the experimental error coming from large drift currents flowing

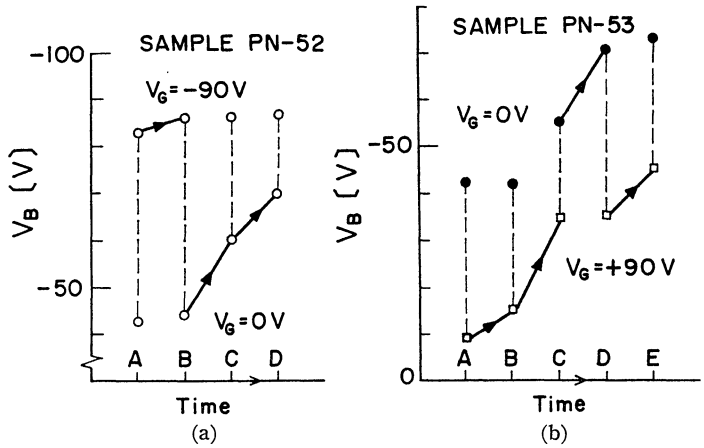


Fig. 10. Drift of breakdown voltage, V_B, for p-channel transistors in the cases of $V_G=-90$, 0 and 90 V. Arrows show the process of the drift of the breakdown voltage.

between the source and the drain. This is because small avalanche currents should be detected to prevent the drift of the breakdown voltage during the measurement. Figure 10(a) shows the drift of the breakdown voltage for the cases of $V_G=0$ and -90 V. For simplicity we shall use hereafter a notation $V_B(V_G)$ for the breakdown voltage as a function of the gate voltage, V_G. Before the drift (step A in Fig. 10(a)) $V_B(0)=-43$ V and $V_B(-90)=-83$ V. It takes longer time to drift $V_B(-90)$ than $V_B(0)$ and the amount of the drift is not so much, as seen in the figure. After $V_B(-90)$ drifts to -86 V (step B), $V_B(0)=-44$ V. $V_B(0)$ is easy to drift appreciably within a short time (say, 1s). Even when $V_B(0)$ drifts to -60 V (step C), $V_B(-90)$ remains at the nearly same value as before.

Figure 10(b) shows the drift of the breakdown voltage for the cases of $V_G=0$ and 90 V. While a small change in $V_B(90)$ appears during step A to B, $V_B(0)$ does not change. When the change in $V_B(90)$ is large (step B to C), however, $V_B(0)$ also drifts to -55 V from -43 V. On the other hand, when $V_B(0)$ drifts to -70 V (step D), $V_B(90)$ remains almost unchanged.

Figures 11(a) and (b) show the cases of n-channel transistors fabricated on a substrate of high resistivity. When the gate voltage is zero or positive, the amount of the drift is no more than 10 V (see Fig. 11(a)). After step C in Fig. 11(a) the break down voltage shows no further change. In the case of a high negative gate voltage (-50 V) the break-

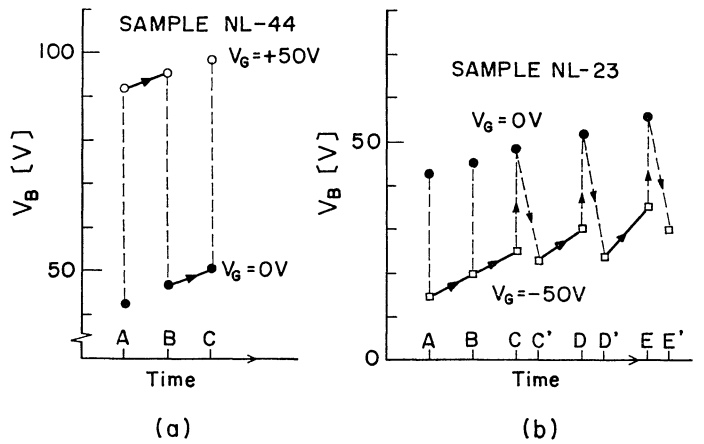


Fig. 11. Drift of breakdown voltage, V_B, for n-channel transistors in the cases of $V_G=-50$, 0 and 50 V. Resistivity of the substrate is 100 Ω cm.

down voltage drifts remarkably and the amount of the drift exceeds 10 V. However, if we induce the breakdown at the zero gate voltage after the drift of $V_B(-50)$, the value of $V_B(-50)$ turns back a little (see step C to C', D to D' and E to E'). Investigation of these results will be given in the next section.

§ 4. Discussions

From the experimental results it is concluded that the increase in the drain current after test A or B originates in the increase in the negative charge (for p-channel cases) and the positive charge (for n-channel cases) in the oxide near the source or the drain. If positive charges, for example, the sodium ions in sample PN-36 are decreased, it shall be ascribed to a part of the increase in the negative charge. The difference in N_{SS} between the two curves for the two different samples subjected to the successive test B in Fig. 9 agrees approximately with the initial difference in N_{SS}, $6.8\times10^{11}\,\mathrm{cm}^{-2}$, corresponding to the initial difference in $V_{TM}(10-4=6\,\mathrm{V})$. This result does not necessarily mean, however, that the sodium ions migrate in the oxide during test B. We can account for the result even if the migration of the sodium ions is not taken into consideration. Let us remind that V_a is the avalanche breakdown voltage of the source or the drain junction having the surface conditions after the test of the same test voltage is applied. The avalanche breakdown voltage is affected by the surface conditions near the source and the drain, that is to say, the net charge in the oxide. It should be pointed out that when two transistors of the same geometical structure are subjected to the test of the same test voltage, the two transistors are considered to have the same amount of net charge in the oxide near the drain and the source. It follows from these considerations that sample PN-36 must have more negative charges enough to compensate the initial positive charges from the sodium ions. Thus one need not ascribe the result shown in Fig. 9 to the migration of the sodium ions during test B.

Now we should investigate the origin of the negative charge in the oxide. Although we have known many species of positive ions in the oxide, there are scarcely any ions with a negative charge in the oxide which come from contaminated circumstances. From our experimental results described in 3.4 we cannot attribute the negative charges to Cl^-, Br^- or OH^- coming from air. Moreover in the case of the n-channel transistors the positive charge must be considered. Thus we shall give up the ionic model. Rather it may be natural to assign the charge in the oxide coming from electrons (for p-channel cases) and holes (for n-channel cases).

Some of electrons or holes generated by impact ionization in the depletion region may attain sufficient energy to sur-mount the potential barrier at the silicon-oxide interface and to enter the oxide, and may reside in the oxide. We shall attempt to estimate the possibility. We take 5×10^5 V/cm for the electric field strength in the depletion region (see Fig. 8). To attain the energy of the potential barrier equal to the energy difference between the conduction band minima of the oxide and the silicon (3.15 eV),[3] the electrons must travel a distance of 630 Å without scattering. The probability, T, of their doing this is roughly*

$$T=\exp\left(-\frac{630}{60}\right)=2.8\times10^{-5}. \qquad (8)$$

We have taken 60 Å for the mean free path between scattering by optical phonons.[4] Supposse that the avalanche current is 0.1 A/m in the transistor of a unit channel width and it flows within a depth, 1 μm, beneath the oxide-silicon interface. Then the number of the electrons which can enter the oxide per second is estimated to be

$$\frac{0.1}{1.6\times10^{-19}}\cdot\frac{60}{10000}\cdot T\approx1\times10^{11}\,\mathrm{m}^{-1}\cdot\mathrm{sec}^{-1}. \qquad (9)$$

If these electrons enter the oxide of the area of 1 μm$\times$1 m, the electron concentration in the oxide per unit area is $10^{13}\,\mathrm{s}^{-1}\cdot\mathrm{cm}^{-2}$. This value is high compared with the experimental result shown in Fig. 9. This would probably come from an overestimation of T. On the other hand when we extrapolate the curve of the spectral distribution of photons from microplasma[7] to 4.2 eV (=3.1+1.1) the fraction of the photons with 4.2 eV is estimated to be around 10^{-7}. If we use this value for T, the electron concentration

* According to Baraff,[5] this method of estimation similar to the one by Shockley[6] results in an overestimation.

entering the oxide amounts to $10^{11}\,cm^{-2}\cdot s^{-1}$. This value is of a reasonable order for the experimental results. In the case of holes, the barrier height is 3.8 eV[8] and the mean free path is ~45 Å.[4] So the probability of holes entering the oxide is smaller than that of electrons. This also generally agrees with the experimental results that in the *n*-channel transistors the the drift of the breakdown voltage and the increase in the drain current are both smaller than those in the *p*-channel cases.

In the course of this study, Nicollian *et al.*[9,10] reported the injection of electrons or holes generated by ionizations in *p*-type silicon into the oxide. Their sample is an MOS diode and a high ac voltage of a period short enough to keep the semiconductor surface from inversion is applied between the gate and the substrate.[9] Thus the high electric field exists in the direction of the surface normal and the generated electrons are readily accelerated to flow into the oxide. So, the effects of the injection may be much larger than those in the transistors. In the case of the transistor structure most of the electrons flow in the direction parallel to the semiconductor surface. However some of them flowing within a distance of the mean free path beneath the oxide will enter the oxide.

Nicollian *et al.* have pointed out that water plays an important role in the charging effect.[9] In their experiment, the charging of the oxide cannot be observed after heating the oxide in vacuum at 600°C for 10 min, and is reduced significantly after heating at 200°C. In the present experiment, the charging effect occurs even after heating the *p*-channel sample at 300°C for 5 hours in vacuum. Note that our gate oxide was grown in steam. The difference in both experimental results may come from the following situation: The oxide near the source and the drain in the *p*-channel transistors will contain an appreciable amount of boron through diffusion from the source and the drain. Since the hydroxyls are known to be unusually stable in the oxide containing Al,[11] the hydroxyls may be also stable in the oxide containing boron.

We can understand the phenomena shown in Figs. 10 and 11 by this model of electron or hole injection. Figure 12 shows schematically a charge and field distribution near the drain in a *p*-channel transistor. The depletion region spreads mainly to the channel, since the drain region is heavily doped. When the avalanche takes place, the electrons generated by ionizations distribute mostly in the channel side of the depletion region and the holes in the drain side of the depletion region.[12] When $V_G=-90$ V, the electrons can hardly enter the oxide since the electric field across the oxide prevents it. Some of holes distributing near the drain can enter the oxide over the drain region. Thus the drift of the breakdown voltage is not large. When $V_G=0$ V, the electrons are accelerated into the oxide by the electric field across the oxide, which results in the large drift of the breakdown voltage. The experimental result that after the drift of $V_B(0)$, $V_B(-90)$ does not change so much (step *B* to *D* in Fig. 10(a)) is explained as follows: When $V_G=0$ V, the depletion region does not extend so deeply into the channel and the electrons will be trapped in the oxide near the drain. On the other hand, when $V_G=-90$ V, the depletion region extends very deeply into the channel and the breakdown voltage, $V_B(-90)$, is little affected by the electrons trapped in the oxide

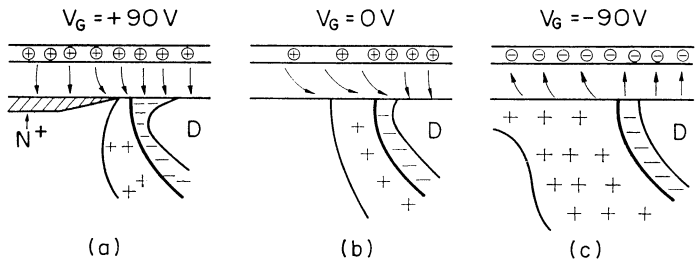


Fig. 12. Cross-sectional representations of expected shapes of depletion region near drain for a *p*-channel transistor.

(a) $V_G=+90$ V, (b) $V_G=0$ V and (c) $V_G=-90$ V.

adjacent to the drain at the zero gate voltage. When V_G=90 V, the drift of the breakdown voltage is very large on account of the accelerating electric field across the oxide (see Fig. 10(b)). At this time the depletion region is very short (see Fig. 12(a)) and the electrons will be trapped in the oxide in close proximity to the drain. Thus these electrons does not raise $V_B(0)$ (step A to B in Fig. 10(b)). When the drift of $V_B(90)$ is large the electrons will distribute in the oxide away from the drain and raise $V_B(0)$ (step B to C). During step C to D in Fig. 10(b), $V_B(0)$ drifts by 15 V while $V_B(90)$ does not change. The electrons newly trapped in the oxide during the drift of $V_B(0)$ will remain far away from the drain. They will not be over the depletion region at V_G=90 V and so $V_B(90)$ does not change during step C to D.

For the n-channel transistors we can understand the results shown in Fig. 11(a) and (b) analogously by replacing electrons with holes. During step C to C' in Fig. 11(b), $V_B(-50)$ decreases a little through the avalanche breakdown given at the zero gate voltage. This will be due to neutralization of the positive charges by electrons during the breakdown at the zero gate voltage.

Finally we describe briefly recovery of the breakdown voltage. The recovery of the breakdown voltage changed by test A or B was investigated by heating the samples at high temperatures and by illuminating the samples with infrared light. The result of the recovery of the breakdown voltage at high temperatures is similar, within a limited range of the heating time, to that observed by Gurtler.[1] However appreciable deviations are observed for longer heating time in all of samples. On illuminating the samples in which the breakdown voltage was changed by test B, the infrared light with a wavelength of 2 μm is shed through the back surface of the substrate, which can arrive at the oxide. No recovery of the breakdown voltage was detected after the illumination. This result agrees with that observed by Nicollian *et al.*[9]

§ 5. Summary and Conclusion

A new instability has been found in p- and n-channel MOS transistors: when a high voltage enough for the breakdown is applied to the drain electrode, the breakdown voltage drifts to a higher value and the drain current increases in low drain voltages. This instability is observed more remarkably in p-channel transistors. We have investigated the origin of the instability and arrived at a conclusion that the instability is caused by injection of electrons and holes generated during the drain avalanche breakdown into the gate oxide near the drain. In p-channel transistors, electron injection occurs predominantly because of accelerating electric field across the gate oxide. The electrons captured in the gate oxide act to raise the breakdown voltage and make more p-like the semiconductor surface near the drain. This leads to reduction of the active channel length. In n-channel cases, the holes play a similar role, but their injection is less than electron injection in p-channel cases because of the higher energy barrier at the oxide-silicon interface and the shorter mean free path for holes than for electrons.

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