An Analytic Current–Voltage Equation for Top-Contact Organic Thin Film Transistors Including the Effects of Variable Series Resistance

Japanese Journal of Applied Physics
Vol. 47, No. 4, 2008, pp. 3174–3178

An Analytic Current–Voltage Equation for Top-Contact Organic Thin Film Transistors Including the Effects of Variable Series Resistance

Keum-Dong JUNG*, Yoo Chul KIM, Byeong-Ju KIM, Byung-Gook PARK, Hyungcheol SHIN, and Jong Duk LEE

Inter-University Semiconductor Research Center (ISRC) and School of Electrical Engineering, Seoul National University, San 56-1, Sillim-dong, Gwanak-gu, Seoul 151-742, Republic of Korea

(Received October 1, 2007; revised November 24, 2007; accepted December 25, 2007; published online April 25, 2008)

An analytic current–voltage (I–V) equation for top-contact organic thin film transistors (OTFTs) is derived by analyzing the channel and the overlap region separately. From the analysis on the overlap region, the series resistance of OTFTs is found to be a function of the gate voltage due to the sheet resistance change of the accumulation layer. Using the derived I–V equation, the characteristics of both the channel and the overlap region are well-explained. The I–V equation is verified with fabricated top-contact OTFTs and metal–insulator–semiconductor (MIS) capacitors, and the predicted I–V characteristics from the equation agree well with the measurements. Also, the ratio of the series resistance to the total resistance of the device is up to 60% which shows significant influence of the series resistance on top-contact OTFT performance.
[DOI: 10.1143/JJAP.47.3174]

KEYWORDS: TFT, OTFT, top-contact, inverted staggered, current–voltage, I–V, modeling, series resistance, pentacene, MIS capacitor, admittance

1. Introduction

Recently, organic semiconductors are used not only to fabricate a single transistor but also to make integrated circuits such as radio-frequency identification (RFID) tags.[1] As a result, it is necessary to establish a physically meaningful device model to extend the applicability of organic thin film transistors (OTFTs). For OTFTs, series resistances near source and drain electrodes have been known to have serious effects on the device characteristics, so that integration of an accurate series resistances model has been one of the key issues in the device modeling.[2] Moreover, if OTFTs are scaled down to realize fast operation, the series resistance model becomes more critical factor on the accuracy of the device model.

Although bottom-contact OTFTs are known to have relatively large series resistance, top-contact OTFTs which are suitable for fast operation also have a serious series resistance problem.[3] There have been a lot of attempts to analyze the series resistance in top-contact OTFTs,[2–6] and some of recent researches show that the series resistance of top-contact OTFT is not a constant value. By using gated transmission line method, Gundlach *et al.*[3] showed that the series resistance is a function of gate voltage. Direct measurements on the series resistance with Kelvin probe microscopy[4] or four-probe system[5,6] also showed that the series resistance changes with the gate voltage. However, there has been no analytic current–voltage (I–V) equation which reflects this observation except for a few empirical models.[7] Therefore, in this paper, by analyzing the gate–source overlap region, an analytic I–V equation including the effects of variable series resistance is derived. Furthermore, the derived equation is verified by applying them to the I–V characteristics of fabricated OTFTs.

2. Derivation of I–V Equation

The cross section of a top-contact OTFT is shown in Fig. 1. The drain current of the device flows from source to drain electrode through the source resistance R_s, the channel resistance R_{ch}, and the drain resistance R_d. Prior to the derivation of I–V equation, following assumptions are made. For linear region operation, the gate is biased to $V_G < V_{TH}$ to accumulate charges in the channel and the drain is biased to a very small value, e.g., $V_D = -0.1$ V. Under this bias condition, the accumulation layer is induced not only in the channel but also at the bottom of the overlap region. The sheet resistance R_{sh} (Ω/sq.) of the accumulation layer can be considered to be uniform because V_D is very small. The current in the channel is assumed to flow only through the accumulation layer, so that the net current in the bulk semiconductor is zero. Due to the effects of R_s and R_d, the intrinsic source and drain voltages, V_S' and V_D', are different from the applied voltages V_S and V_D, respectively. To derive I–V equation under these assumptions, the channel and the overlap region are analyzed separately.

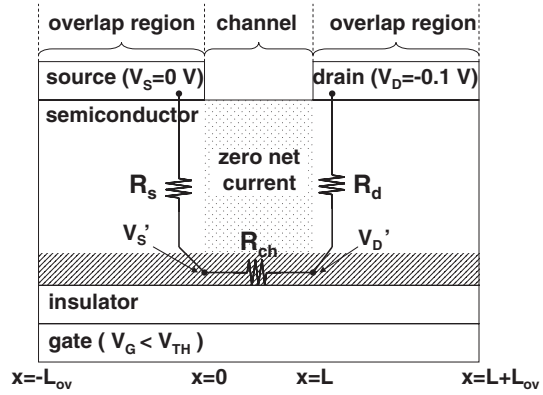

Fig. 1. Cross-section of a top-contact OTFT in the linear region. Accumulation layer is induced uniformly at the bottom of semiconductor due to the negative V_G. V_S' and V_D' represent intrinsic source and drain voltage, respectively. R_s, R_d, and R_{ch} denote source, drain, and channel resistance, respectively.

The channel is considered first as shown in Fig. 2. For the channel, it is assumed that the current flows only through the accumulation layer, so that derivation of an I–V equation is quite similar to that of general metal–oxide–semiconductor field-effect transistor (MOSFET) equations except for considering the effects of the series resistances. Due to the series

*E-mail address: windbit@naver.com

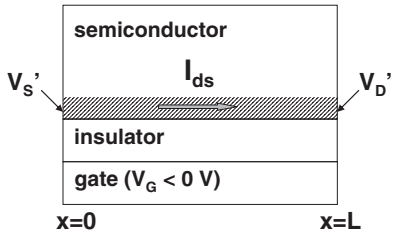

Fig. 2. For the channel, the current is determined by R_{sh} and the intrinsic source and drain voltage, i.e., V_S' and V_D'.

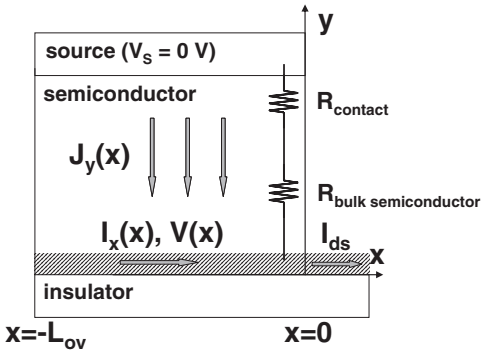

Fig. 3. For the overlap region, $I_x(x)$, $V(x)$, and $J_y(x)$ are determined by R_{sh}, R_y and Kirchhoff's law. For the current continuity, $I_x(x)$ becomes I_{ds} at $x = 0$.

resistances, V_S' and V_D' should be used in the equations instead of V_S and V_D. Therefore, the drain current I_{ds} can be expressed using the sheet resistance R_{sh} as

$$I_{ds} = \frac{W}{L}\frac{V_D' - V_S'}{R_{sh}} \approx \mu_{eff} C_i \frac{W}{L}(V_G - V_{TH})(V_D' - V_S'), \quad (1)$$

where W, L, μ_{eff}, C_i, and V_{TH} represent the device width, device length, effective field-effect mobility, insulator capacitance, and threshold voltage, respectively. Although all the parameters such as mobility and threshold voltage are known, the drain current can not be determined with this equation due to unknown V_D' and V_S'. Therefore, V_D' and V_S' should be obtained prior to calculating I_{ds}.

For eq. (1) and other equations described in this paper, the notation R_{sh} itself is preferred instead of more complex form using mobility and threshold voltage. One reason for using R_{sh} is its simplicity and the other reason is that the relation of R_{sh} with other parameters such as effective mobility and threshold voltage is still under discussion in OTFTs.[7] Therefore, R_{sh} itself is used for further discussion and a detailed analysis on R_{sh} will be bypassed in this paper.

To obtain the potential drop over the series resistance, the overlap region is considered as shown in Fig. 3. For the accumulation layer, $V(x)$ and $I_x(x)$ represents the electric potential and the current which changes with position x, respectively. The sheet resistance of the accumulation layer is the same as R_{sh} in the channel because the accumulation layer is considered to be uniform. From the source electrode to the accumulation layer, it is assumed that the current flows only in y-direction represented by current density $J_y(x)$. R_y denotes the apparent y-direction resistance per unit area ($\Omega\,cm^2$) which includes both contact and bulk semiconductor resistance. In fact, lots of factors in OTFTs are related to R_y such as contact metal, metal/semiconductor interface, semiconductor thickness, intrinsic charge concentration, bulk trap and even morphology.[8–11] As a result, detailed analysis on y-direction resistance can be very complex and unessential for the device modeling. Instead, by using the apparent resistance, the equations become simpler and more intuitive without losing the generality. This apparent resistance R_y is assumed not to depend on V_G because the effects of V_G on R_y can be screened by the charges induced in the accumulation layer by the same V_G.

Using these electrical quantities and Kirchhoff's law, three equations can be derived for the overlap region. First, for $I_x(x)$ and $V(x)$, the potential change in dx is determined by R_{sh} as

$$V(x + dx) = V(x) - I_x(x)R_{sh}\frac{dx}{W}. \quad (2)$$

Next, the potential from the source electrode to the accumulation layer changes from zero to $V(x)$ undergoing potential drops by $J_y(x)$ and R_y as

$$0 - (J_y(x)W\,dx)\frac{R_y}{W\,dx} = V(x). \quad (3)$$

Finally, because $J_y(x)$ contributes to $I_x(x)$ when reaching the accumulation layer, $I_x(x)$ is integral of $J_y(x)$ given as

$$I_x(x) = W\int_{-L_{ov}}^{x} J_y(x)\,dx. \quad (4)$$

If L_{ov} is assumed to be infinite for the ease of solving process, $J_y(x)$, $I_x(x)$, and $V(x)$ are simply obtained as

$$J_y(x) = J_{y0}\exp(x/L_0), \quad (5)$$

$$I_x(x) = WL_0J_{y0}\exp(x/L_0), \quad (6)$$

$$V(x) = -R_yJ_{y0}\exp(x/L_0), \quad (7)$$

$$L_0 = \sqrt{R_y/R_{sh}}, \quad (8)$$

where J_{y0} is an integration constant and L_0 is a characteristic length given by eq. (8). The derived equations show that the current density $J_y(x)$ is not uniform along the overlap region, and most of current flows within L_0 from the edge of the overlap region. The maximum current density is J_{y0} at $x = 0$, which needs another boundary condition to be determined. L_0 is determined only by the ratio of R_y to R_{sh}, and other parameters such as channel length do not affect L_0. Another point that should be noted for L_0 is that L_0 is function of V_G because R_{sh} is dependent on V_G while R_y is not a function of V_G. Considering the relation between R_{sh} and V_G, L_0 increases with larger V_G, i.e., smaller R_{sh}.

It is difficult to measure $J_y(x)$, $I_x(x)$, and $V(x)$ directly from an experiment and there has been no report which tried to measure these quantities in OTFTs. However, using technology computer-aided design (TCAD) simulation, one can indirectly verify the validity of the derived equations. Figure 4 shows one example which compares the simulation results with the equation for $J_y(x)$. As shown in the figure, the simulation results agree well with the derived equation and the values of L_0 also changes with V_G as predicted above. Different simulation parameters such as different insulator thickness or different channel length do not affect the exponential shape of $J_y(x)$ while the values of L_0 and J_{y0} can be changed.

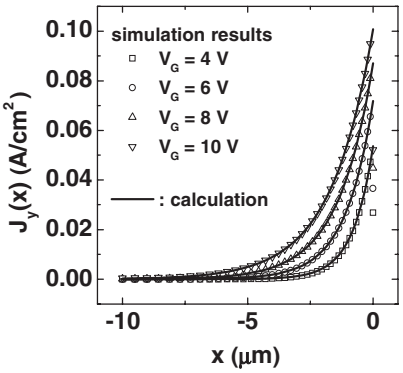

Fig. 4. To verify eq. (5), $J_y(x)$ is obtained from the simulation on an amorphous Si (a-Si) TFT. Good agreement between simulation and calculation confirms that the equation for $J_y(x)$ is properly derived. For the simulation, oxide of 45 nm and a-Si of 250 nm is used for the a-Si TFT. The channel length of the device is 10 μm.

Using the derived equations, a lot of information related to the overlap region can be obtained. Although the equations are derived for the source overlap region, the same equations can be applied to the drain overlap region. First, the total current flowing through the overlap region can be obtained by $I_x(x=0) = WL_0J_{y0}$. Second, the total potential drop along the overlap region becomes $V(x=0) = -R_yJ_{y0}$. Finally, the total series resistance R_{sd} which is twice of R_s is determined by

$$R_{sd} = 2R_s = -2\frac{V(x=0)}{I_x(x=0)} = \frac{2R_y}{WL_0}. \tag{9}$$

The equation shows that R_{sd} is proportional to R_y and inversely proportional to L_0. While R_y is independent on V_G, L_0 is a function of V_G. Therefore, R_{sd} also becomes a function of V_G, which coincide with previous experimental observations.[2–6] With large V_G, the series resistance decreases because L_0 increases. Looking into eq. (9) in more detail, the origin of variable series resistance can be found. L_0 itself is a function of V_G because it is related to R_{sh} in eq. (8). Therefore, the main origin of V_G-dependent series resistance must be R_{sh}, the sheet resistance of the accumulation layer. This observation indicates that R_{sd} in top-contact OTFTs changes with V_G because of the top-contact structure itself, not because of the organic semiconductor. In other words, any thin film transistor which has top-contact or inverted-staggered structure can have V_G-dependent series resistance. On the other hand, most of the unique characteristics of R_{sd} for the OTFTs are related to the characteristics of R_y which is directly related to R_{sd} in eq. (9). Usually, high contact resistance and high bulk resistivity of OTFTs result relatively high R_y, so the effects of the series resistances seem to be larger than those of other TFTs. For some organic semiconductors such as pentacene, the anisotropy of the thin film also affects on R_y. If the mobility of an organic semiconductor is very small, the series resistance becomes very large not only due to large R_y but also due to large R_{sh}, i.e., small L_0.

Using the analysis so far, the I–V equation for top-contact OTFTs can be derived. At the boundary of the channel and the overlap region, the current should be continuous. Therefore, using eqs. (1) and (6), the relation

$$I_{ds} = \frac{W}{L}\frac{V_D' - V_S'}{R_{sh}} = WL_0J_{y0} \tag{10}$$

should be satisfied. Next, V_S' and V_D' can be obtained using eq. (7) as

$$\begin{aligned} V_S' &= V(x=0) = -R_yJ_{y0}, \\ V_D' &= V_D - V(x=0) = V_D + R_yJ_{y0}. \end{aligned} \tag{11}$$

By solving eqs. (10) and (11), the final I–V equation for top-contact OTFTs can be obtained as

$$I_{ds} = W\frac{V_D}{LR_{sh} + 2R_y/L_0}. \tag{12}$$

As generally expected, the equation of I_{ds} in the linear region is proportional to V_D and W. The other parameters to determine I_{ds} are R_{sh}, R_y, and L_0. Because L_0 can be obtained from R_{sh} and R_y using eq. (8), if one can obtain R_{sh} and R_y, I_{ds} can be obtained from eq. (12). As mentioned above, the equation is valid only for very small V_D. For larger V_D to break the symmetry of the device, the equation can not be used due to the different source and drain resistances.

By checking the limiting cases, the validity of the equation can be proved. If R_y becomes zero, I_{ds} converges to the general MOSFET equation, i.e.,

$$I_{ds}|_{R_y\to 0} = W\frac{V_D}{LR_{sh}} \approx \mu_{eff}C_i\frac{W}{L}(V_G - V_{TH})V_D. \tag{13}$$

If the channel length L becomes zero, the whole device characteristics should be determined only by the series resistance. In this case, I_{ds} in eq. (12) becomes

$$I_{ds}|_{L\to 0} = W\frac{V_D}{2R_y/L_0} = \frac{V_D}{2R_y/WL_0} = \frac{V_D}{R_{sd}} \tag{14}$$

which corresponds to eq. (9). Therefore, the equation for I_{ds} in eq. (12) can be considered to have both characteristics of the channel and the overlap region.

3. Device Fabrication and Discussion

To verify the derived I–V equation, OTFTs are fabricated as shown in Fig. 5. An n^+-Si wafer with sheet resistance of 10 Ω/sq. is used as the gate electrode and 35-nm thick thermal SiO_2 is used as the insulator. After pentacene films of different thicknesses from 25 to 100 nm are thermally evaporated through shadow masks, gate and source electrodes are e-gun evaporated with gold through another shadow mask. The dimension W/L of fabricated OTFTs is

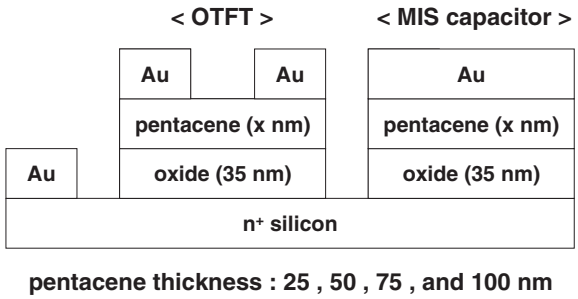

Fig. 5. Structure of the fabricated OTFTs and MIS capacitors. Pentacene thicknesses are varied to obtain different R_y. Gate–source overlap length L_{ov} is fixed to 100 μm.

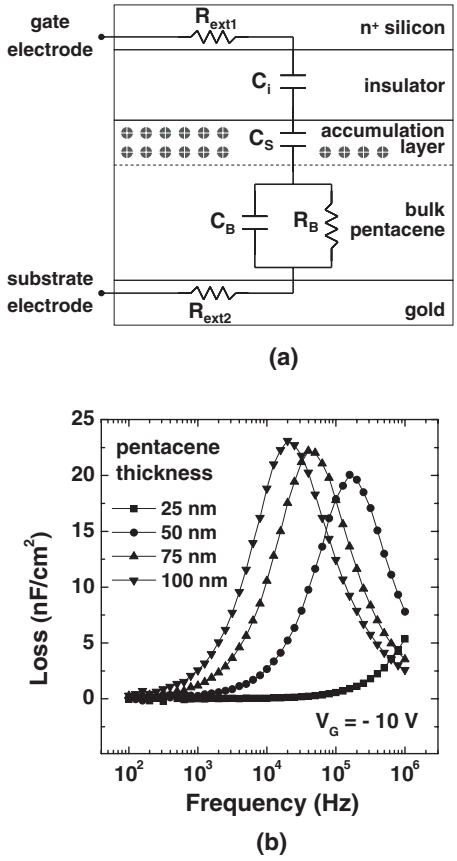

Fig. 6. (a) The model used for the admittance modeling is composed of the insulator capacitance C_i, the semiconductor capacitance C_S, the bulk capacitance C_B, the bulk resistance R_B, and the external series resistance R_{ext}. (b) The peaks of the loss curves shift to the low frequency due to the large bulk resistance of the thick pentacene film.

600/60. *I–V* characteristics of the devices are measured with Agilent 4156C parameter analyzer. Together with OTFTs, metal–insulator–semiconductor (MIS) capacitors are also fabricated as shown in the figure. For the MIS capacitors, admittance measurements are done with HP 4284A LCR meter. The frequency ranges from 100 Hz to 1 MHz, and the gate voltage is fixed to −10 V. All the *I–V* and admittance measurements are done in the air.

To obtain R_y values, the admittance measurement and modeling of the MIS capacitors are used.[8–10] Figure 6(a) shows the equivalent circuit model for the MIS capacitor in the accumulation regime. For the accumulation regime, the admittance is mainly determined by the insulator capacitance C_i, the bulk resistance R_B, and the bulk capacitance C_B. The semiconductor capacitance C_S which has relatively large value in the accumulation regime can be neglected in the admittance modeling because it is connected in series with relatively small C_i. The external series resistance R_{ext} which exists in the n^+-Si gate electrode and the gold electrode also can be negligible in this experiment because it is very small so that the effects can be observed above the frequency of 1 MHz. Under this condition, the admittance of the device is given as

$$Y = \left(\frac{G}{\omega}\right)\omega + j\omega C, \tag{15}$$

$$\frac{G}{\omega} = \frac{\omega C_i^2 R_B}{1 + \omega^2 (C_B + C_i)^2 R_B{}^2}, \tag{16}$$

$$C = \frac{C_i(1 + \omega^2 C_B (C_B + C_i) R_B{}^2)}{1 + \omega^2 (C_B + C_i)^2 R_B{}^2}, \tag{17}$$

where Y, ω, G/ω, and C represents the admittance, the angular frequency, the loss, and the capacitance of the device. The peak frequency f_{peak} of the loss curve is obtained from eq. (16) as

$$f_{peak} = \frac{1}{2\pi(C_i + C_B)R_B}. \tag{18}$$

Therefore, R_B can be obtained from the peak of the loss curve if C_i and C_B can be obtained. Obtaining C_i is not hard because it can be measured directly from the metal–insulator–metal (MIM) capacitor. C_B also can be obtained from the capacitance–voltage (*C–V*) curve of the MIS capacitor because it has the same value with the depletion capacitance of the MIS capacitor.[9] Figure 6(b) shows the measured loss curves with different pentacene thicknesses. For the thicker pentacene film, the peaks of the loss curves shift to the lower frequency. Considering the sum of C_i and C_B becomes smaller for the thicker pentacene thickness, the lower shift of the loss peak is mainly due to the increase of R_B. The values of extracted R_B, which can be considered as R_y in this experiment, are summarized in the Table I. At the pentacene thickness of 25 nm, R_y can not be determined because the loss peak is out of the measuring frequency range. R_y at the pentacene thickness of 100 nm is 3,923 MΩ μm^2, which is relatively large considering the thickness of the semiconductor. The rod-like shape of pentacene can be one of the reasons for this large R_y values. Moreover, R_y changes significantly with the relatively small change of the pentacene thickness, of which the origin is not clear. However, although the characteristics of obtained R_y are not totally understood, R_y still can be used for the *I–V* modeling with eq. (12) because the characteristics of R_y do not affect the derivation of eq. (12).

To obtain R_{sh}, *I–V* characteristics of OTFTs should be used. Because R_y of 25 nm device is relatively small, R_{sh} can be approximately obtained using the *I–V* curve of 25 nm device as shown in Fig. 7(a). Using the obtained R_y and R_{sh}, L_0 can also be calculated with eq. (8) as shown in Fig. 7(b). L_0 changes with the pentacene thickness because R_y is different for each thickness. In addition, the values of L_0 change with V_G as expected from the equation and the value is as large as 20 μm at its maximum.

Finally, I_{ds} for pentacene thickness of 50, 75, and 100 nm are calculated using the obtained R_{sh}, R_y, and L_0 with eq. (12) and compared with the measured values in Fig. 8. The I_{ds} equation predicts the measured *I–V* values with

Table I. The values of extracted R_y from the admittance modeling in Fig. 6.

Pentacene thickness (nm)	R_y (MΩ μm^2)
25	<46
50	426
75	1799
100	3923

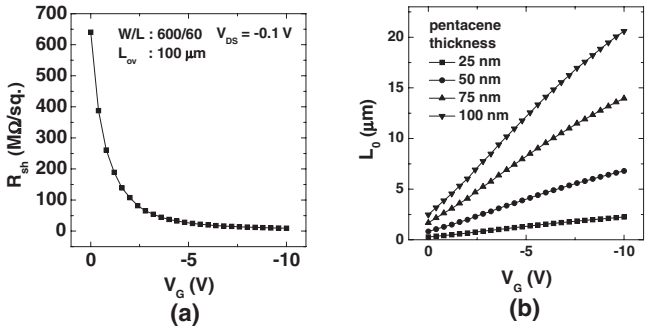

Fig. 7. (a) R_{sh} of the fabricated OTFTs obtained from I–V characteristics of 25 nm device. (b) L_0 of the fabricated devices which are calculated with eq. (8). L_0 is always smaller than the overlap length $L_{ov} = 100\,\mu$m.

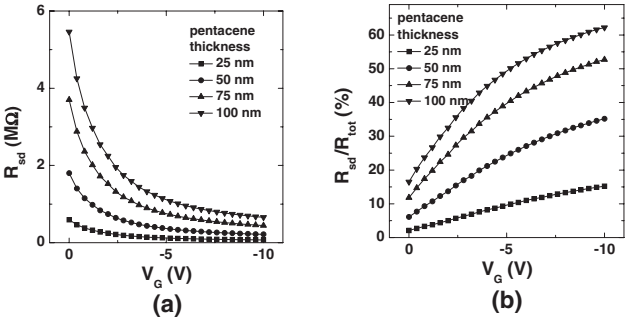

Fig. 9. (a) Obtained R_{sd} using eq. (9) for the fabricated OTFTs. (b) The ratio of R_{sd} to the total resistance is as large as 60% when the pentacene thickness is 100 nm.

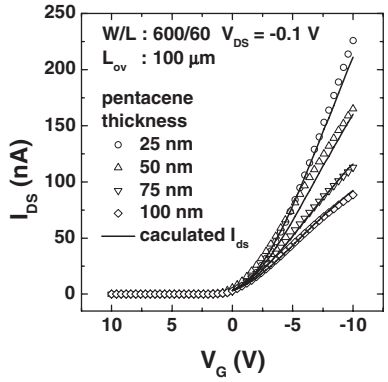

Fig. 8. Measured I–V curve (dotted line) and the calculated I–V curve (solid line) using eq. (12) show good agreement.

relatively small error. In Fig. 9, R_{sd} of the devices using eq. (9) and its ratio to the total resistance are depicted. Although the value of R_{sd} decreases with larger V_G, the ratio of R_{sd} increases with larger V_G. The ratio is as large as 60% at the pentacene thickness of 100 nm, which shows significant influence of R_{sd} on OTFT performance. In addition, it is interesting to notice the shape of I–V curve changes with the ratio. If the ratio is 0%, the I–V curve would be proportional to $(V_G - V_{TH})$ by eq. (13). In contrast, although the ratio is 100%, the drain current can be still modulated by the gate voltage due to the change of the series resistance with V_G. In that case, the drain current would be approximately proportional to $(V_G - V_{TH})^{1/2}$ by eq. (14). For the I–V characteristics of OTFTs in this paper, the power factor would be between 1/2 and 1, and it deceases with pentacene thickness as shown in Fig. 8 because the ratio becomes larger with thicker pentacene thickness.

4. Conclusions

An analytic I–V equation for top-contact OTFTs is derived including the effects of variable series resistance and verified with fabricated OTFTs and MIS capacitors. Based on the analysis of the current flow in the overlap region, the origin of series resistance and its dependence on the gate voltage can be understood. Because only the linear region operation of the device is discussed in this paper, the saturation region operation should be discussed for further modeling of top-contact OTFTs.

Acknowledgment

This work was supported by the Brain Korea 21 (BK21) program.

1) E. Cantatore, T. Geuns, A. Gruijthuijsen, G. Gelinck, S. Drews, and D. de Leeuw: ISSCC Dig., 2006, p. 1042.
2) P. V. Necliudov, M. S. Shur, D. J. Gundlach, and T. N. Jackson: Solid-State Electron. **47** (2003) 259.
3) D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudovc, and M. S. Shur: J. Appl. Phys. **100** (2006) 024509.
4) K. P. Puntambekar, P. V. Pesavento, and C. D. Frisbie: Appl. Phys. Lett. **83** (2003) 5539.
5) P. V. Pesavento, R. J. Chesterfield, C. R. Newman, and C. D. Frisbie: J. Appl. Phys. **96** (2004) 7312.
6) I. Yagi, K. Tsukagoshi, and Y. Aoyagi: Appl. Phys. Lett. **84** (2004) 813.
7) D. Natali, L. Fumagalli, and M. Sampietro: J. Appl. Phys. **101** (2007) 014501.
8) E. J. Meijer, A. V. G. Mangnus, C. M. Hart, D. M. de Leeuw, and T. M. Klapwijk: Appl. Phys. Lett. **78** (2001) 3902.
9) I. Torres and D. M. Taylor: J. Appl. Phys. **98** (2005) 073710.
10) N. Zhao, O. Marinov, G. A. Botton, M. J. Deen, B. S. Ong, Y. Wu, and P. Liu: IEEE Trans. Electron Devices **52** (2005) 2150.
11) S. H. Jin, K.-D. Jung, H. Shin, B.-G. Park, and J. D. Lee: Synth. Met. **156** (2006) 196.