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Analysis of Short-Channel Schottky Source/Drain Metal-Oxide-Semiconductor Field-Effect Transistor on Silicon-on-Insulator Substrate and Demonstration of Sub-50-nm n-type Devices with Metal Gate

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The Schottky source/drain metal-oxide-semiconductor field-effect transistor (MOSFET) has potential for scaling to the nanometer regime, because low electrode resistances with very shallow extension can be realized using metal source/drain. In this study, very short channel n- and p-type Schottky source/drain MOSFETs with silicon-on-insulator (SOI) structure were analyzed theoretically, and n-type devices were demonstrated experimentally. It was shown theoretically that a drivability of the Schottky source/drain MOSFET comparable to that of conventional MOSFETs can be realized with a low Schottky barrier height. The short-channel effect can be suppressed even with a 15-nm-long channel at $t_{OX} = 1$ nm and $t_{SOI} = 3$ nm. The room-temperature operation of sub-50-nm n-type $ErSi_2$ Schottky source/drain MOSFETs on a separation by implanted oxygen (SIMOX) substrate was demonstrated.

KEYWORDS: Schottky source/drain MOSFET, short-channel device, SOI device, $ErSi_2$/Si, metal gate

1. Introduction

As circuits have become more and more highly integrated, a great deal of research interest has been focused on small-geometry transistors. To scale down metal-oxide-semiconductor field effect transistors (MOSFETs), the formation of ultrashallow source/drain (S/D) junctions with low resistance is one of the most important technologies. The Schottky S/D MOSFET has potential for scaling to the nanometer regime,[1–3] because low electrode resistances with very shallow extension can be realized using metal source/drains. Operation of the Schottky S/D MOSFET has been demonstrated with a bulk Si substrate.[4] Recently, 27-nm-long channel PtSi Schottky S/D MOSFETs have been reported.[5]

Although low S/D resistances can be realized by metal S/D junctions in the Schottky S/D MOSFET, the drain current is suppressed by the Schottky barrier. If the S/D is formed with a high Schottky barrier metal, the tunneling resistance of the Schottky barrier increases and the drain current becomes small. If this problem can be solved by choosing the appropriate S/D metal, the Schottky S/D MOSFET will have the same drivability as a conventional MOSFET with a highly doped S/D. In addition, there are several advantages of applying Schottky S/D MOSFETs to integrated circuits. The contact resistance between the S/D and the external electrode is lower. The temperature during the fabrication process is lower, because the process requires no doping. Thus, the metal gate can be easily realized.[6,7]

In this paper, a theoretical analysis of the n- and p-type Schottky S/D MOSFETs with silicon-on-insulator (SOI) structure is described. The relationship between the Schottky barrier height and current drivability is discussed. The characteristics of Schottky S/D MOSFETs in the 10 nm region are discussed and a comparison between the Schottky S/D MOSFET and the conventional SOI-MOSFET is drawn. Sub-50-nm metal gate n-type Schottky S/D MOSFETs were fabricated by electron beam lithography and the self-aligned silicide process.

2. Device Structure and Calculation Model

The device structure is shown in Fig. 1. In this calculation, the single-gate SOI structure was used. The gate oxide thickness was 3 nm, and the SOI layer and buried oxide layer (BOX) thicknesses were 10 and 50 nm, respectively, except in the discussion of the short channel effect in §3.2 below. The S/D junction depth was the same as the SOI layer thickness. In operation, electrons (n-type) or holes (p-type) tunneling through the Schottky barrier from the source to the channel were controlled by the voltage applied to the gate across the gate oxide [Fig. 1(b) for n-type]. The drain current depends on the tunneling resistance of the Schottky barrier and the channel resistance. For a high S/D Schottky barrier, the drain current depends mainly on the tunneling resistance, and for a low barrier, the characteristics become almost the same as those of a conventional MOSFET in which the drain current is determined by the channel resistance.

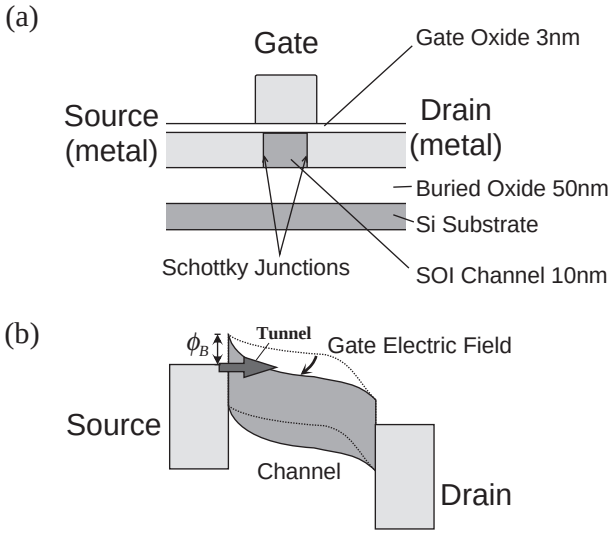

Fig. 1. Device structure of Schottky S/D MOSFET. (a) Cross-sectional structure and (b) band diagram for n-type device.

The device characteristics were analyzed as follows. First, the potential distribution in the device under the application of drain-source and gate-source voltages (V_{DS} and V_{GS}) was calculated by solving Poisson's equation using a finite-element method. The outer material surrounding the device was as-

sumed to be SiO_2. Then, the drain current was calculated using the potential distribution calculated above. The carrier density in the channel affects the potential distribution and the drain current. This carrier density is determined by the drain current. Therefore, the drain current was recalculated to be self-consistent with the carrier density and the potential distribution.

Carrier transport at the Schottky barrier was modeled by a combination of the thermal emission current J_{TH} and the tunneling current J_{TN}, as shown in Fig. 2 for n-type. For the p-type device, the same manners are applied to holes. The thermal emission current is given by[2)]

$$J_{TH} = RT^2 \left[\exp\left(-\frac{e\phi_B}{k_B T}\right) - \frac{N}{n_0} \right], \quad (1)$$

where e is the electron charge, T is the absolute temperature and R is the Richardson constant, which is given by

$$R = \frac{4\pi e m^* k_B^2}{h^3}, \quad (2)$$

where m^* is the effective mass, k_B is Boltzmann's constant, h is the Planck constant and ϕ_B is the Schottky barrier height. In eq. (1), n_0 is the density of carriers with greater energy than the Fermi energy in the metal. This is shown in Fig. 2 and is given by

$$n_0 = n_i \exp\left(\frac{E_g}{2k_B T}\right). \quad (3)$$

In eq. (1), N is the density of carriers which have a greater energy than $e\phi_B$. This is shown in Fig. 2 and is given by

$$N = \frac{RT^2}{eD} \exp\left(-\frac{e\phi_B}{k_B T}\right) \Delta x \exp\left(-\frac{e\phi\,(\Delta x)}{k_B T}\right), \quad (4)$$

where D is the diffusion constant.

The tunneling current through the Schottky barrier J_{TN} is given by[8)]

$$J_{TN} = \frac{e^2 F^2}{8\pi h \phi_B} \exp\left[-\frac{8\pi}{3heF}\sqrt{2m^*(e\phi_B)^3}\right], \quad (5)$$

where F is the electric field at the Schottky barrier.

Barrier lowering due to the image force is included in the calculation using the following equation:[9)]

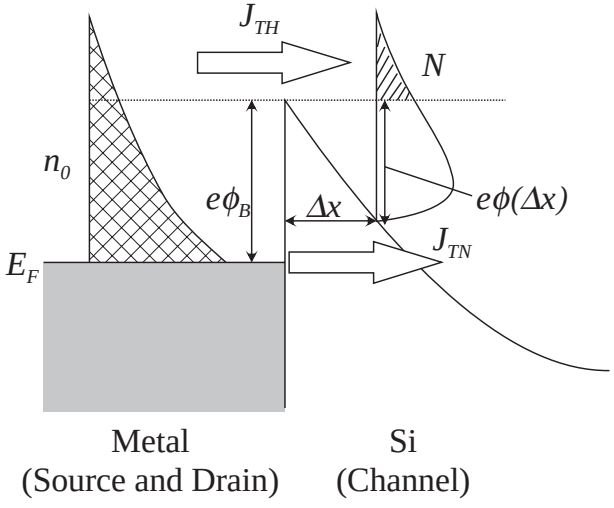

Fig. 2. Model for calculation of the n-type device.

$$\phi_B = \phi_{B0} - \sqrt{\frac{eF}{4\pi\varepsilon}}, \quad (6)$$

where ϕ_{B0} is the Schottky barrier height without an applied voltage and ε is the permittivity.

The current from the source into the channel J_{SB} is given by

$$J_{SB} = J_{THS} + J_{TNS}, \quad (7)$$

where J_{THS} and J_{TNS} are given by eqs. (1) and (5). The current from the drain into the channel J_{DB} is calculated in the same manner. In the calculation of the current, the channel is divided along the channel depth direction. The carrier diffusion between current distribution along the channel depth was neglected, because the total current at the drain is determined by the source Schottky junction and is unchanged even if carrier diffusion occurs in the channel. The current in the channel was calculated using the drift-diffusion model with the drain current $J_D = J_{SB} - J_{DB}$ as boundary values at S/D interfaces. In this calculation, velocity saturation in the channel was neglected, because the built-in electric field in the channel is small due to the Schottky junction.

The constants used for electrons and holes are as follows. For Si the effective masses were $m_e^* = 0.19m_0$ and $m_h^* = 0.15m_0$ for electrons and holes, respectively.[9)] The light-hole effective mass was used. The mobilities of Si used were $\mu_e = 450\,cm^2/Vs$ and $\mu_h = 125\,cm^2/Vs$ for electrons and holes, respectively. These mobilities were for an effective channel electric field of $E_{eff} = 0.4\,MV/cm$,[10,11)] which corresponds to the electric field in the channel at $V_{GS} = 1.5\,V$.

3. Device Characteristics

Figure 3 shows the common-source characteristics calculated at 300 K for various values of V_{GS} for a 50-nm-gate length Schottky S/D MOSFET. The channel length was 35 nm. The Schottky barrier height was assumed to be 0.20 eV for n-type and 0.25 eV for p-type devices. Similarity to conventional MOSFETs, the drain curves for the Schottky S/D MOSFETs saturate.

3.1 Current drivability

The relationship between the channel length L_C and the drain current I_D as a function of the Schottky barrier height ϕ_{B0} is shown in Fig. 4. The applied voltages were $V_{DS} = V_{GS} = -1.2$ and 1.2 V for p-type and n-type devices, respectively. The drain current increases with decreasing Schottky barrier, due to the increased thermal emission and tunneling currents, as shown in eqs. (1) and (5). To compare Schottky S/D MOSFETs and conventional MOSFETs, the drain current of conventional MOSFETs[12,13)] is drawn in the same figure. These results show that for $L_C < 30$ nm, the same drivability as for conventional MOSFETs can be realized using low Schottky barriers, i.e. about 0.25 eV for p-type and 0.1–0.15 eV for n-type devices, respectively. The difference in these values between n-type and p-type devices depends on the effective mass.

Taking these values of the barrier heights into consideration, the appropriate S/D metals are PtSi ($\phi_{Bp} = 0.24$ eV) and IrSi ($\phi_{Bp} = 0.18$ eV)[14,15)] for p-type devices. However, neither pure metal nor silicides meet the above requirement for n-type devices. Although the lowest Schottky barrier silicide is

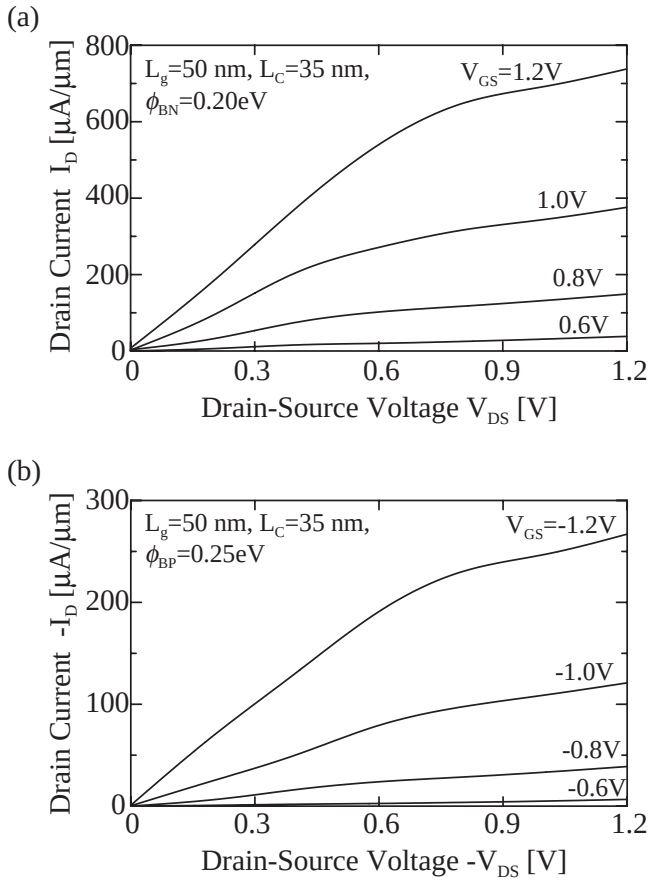

Fig. 3. The drain current curves with common source for a 50-nm-gate length Schottky S/D MOSFET with (a) 0.20 eV S/D Schottky barrier for n-type and (b) 0.25 eV for p-type devices.

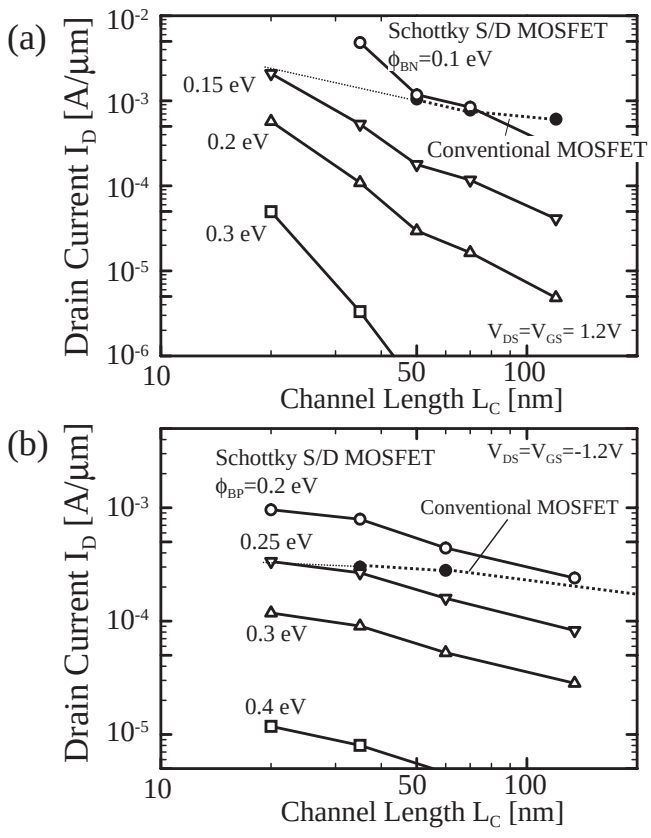

Fig. 4. Drivability of Schottky MOSFETs as a function of Schottky barrier height for (a) n-type and (b) p-type devices.

$ErSi_2$ ($\phi_{Bn} = 0.2$ eV),[16] the drivability of $ErSi_2$ Schottky S/D MOSFETs is ten times lower than that of conventional MOSFETs. One possibility is germanosilicide in which the Schottky barrier heights can be lower than those of silicide.[17,18]

3.2 Short-channel effect

The relationship between threshold voltage shift, subthreshold swing and channel length for a n-type Schottky S/D MOSFET with 0.20 eV S/D barriers is shown in Fig. 5. For comparison between a Schottky S/D MOSFET and a conventional MOSFET, the values calculated by Fiegna *et al.* for conventional MOSFETs with the same device structure are also plotted in the figure.[13] The threshold voltage is defined as the gate bias corresponding to $I_D L_C / W_C = 0.5\,\mu$A.[13] The threshold voltage shift of Schottky S/D MOSFETs is smaller than that of conventional MOSFETs. However, the subthreshold swing of Schottky S/D MOSFETs is larger than that of conventional MOSFETs even with a long channel. In the conventional MOSFET, the drain current is controlled by the gate bias which modulates the channel potential under the gate electrode. In the Schottky S/D MOSFET, the drain current is modulated by the electric field at the source Schottky barrier. The drain voltage strongly affects the potential at the center of the channel. However, the potential near the source is weakly affected by the drain voltage. Therefore, the threshold voltage shift of Schottky S/D MOSFETs is small. Moreover, the region controlled by the gate voltage in Schottky S/D MOSFETs (source/channel interface) is distant from the gate compared to that of conventional MOSFETs (channel region un-

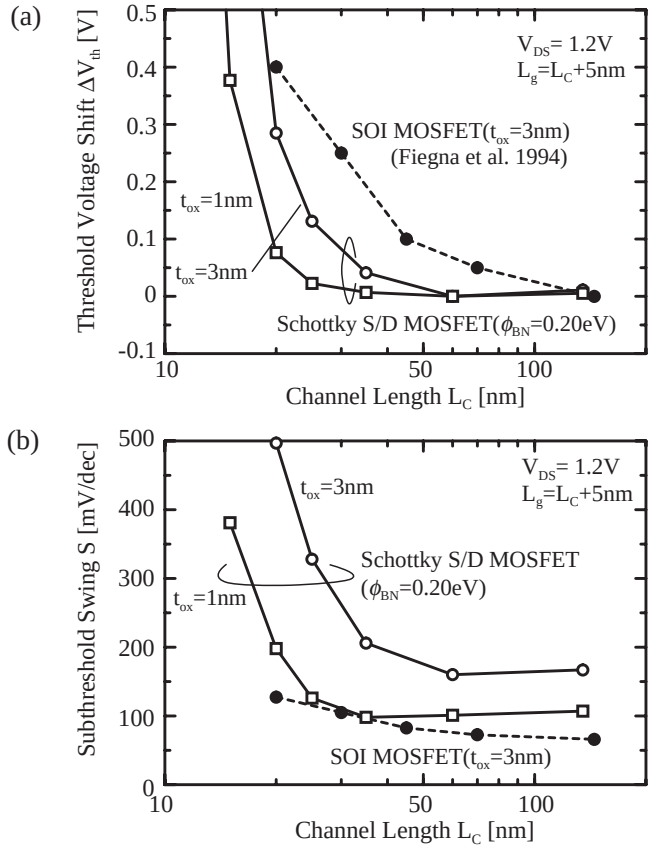

Fig. 5. Relationship between (a) threshold voltage shift, (b) subthreshold swing and channel length of Schottky S/D MOSFETs and conventional SOI-MOSFETs.

der the gate). Therefore, the subthreshold swing of Schottky S/D MOSFETs is larger than that of conventional MOSFETs. To reduce the subthreshold swing, the gate oxide must be thinned, as shown in Fig. 5(b). The relationship between the threshold voltage shift, subthreshold swing and the channel length as a function of SOI layer thickness is shown in Fig. 6. The short-channel effect can be suppressed by thinning the SOI layer, even with a 15-nm-long channel with $t_{OX} = 1$ nm and $t_{SOI} = 3$ nm. Results for n- and p-type devices are almost the same, because the short-channel effect depends primarily on the device structure.

4. Fabrication of n-Type $ErSi_2$ Source/Drain Device with Metal Gate

4.1 Device structure and fabrication process

Very short channel n-type Schottky S/D MOSFETs with metal gates were fabricated by electron beam lithography with a PMMA resist and the self-aligned silicide (salicide) process. Due to the low Schottky barrier height, $ErSi_2$[16] was chosen as the S/D metal. Bulk Si and separation by implanted oxygen (SIMOX) substrates, which were p-type with resistivity of 30 Ωcm, were used. The SOI and BOX layer thicknesses of the SIMOX substrate were 25 and 90 nm, respectively. This thickness of the SOI layer was obtained by thinning via thermal oxidation and wet chemical etching. Although thinning the SOI layer results in better characteristics, it is limited by the present primitive fabrication process. A thin SOI layer can be damaged and partly removed during the salicide process. The junction depths were 25 and 10 nm for bulk and SOI devices, respectively. A 3.5-nm-thick gate oxide layer was grown by thermal oxidation. Then, the metal (Au/Cr) gate was formed by a lift-off process. A SiO_2 film was deposited by argon sputtering, and then the side wall was formed by anisotropic reactive ion etching (RIE) in CF_4. Er was deposited by e-beam evaporation and was then silicided at 400°C in N_2 ambient. The unreacted metals were selectively etched using nitric acid. The isolation layer was SiO_2 and the external electrode was Au/Cr.

The interface between the silicide and the Si remains at the interface between the evaporated metal and the Si for the Si-diffusion-type silicide. For the metal-diffusion-type silicide, the interface sinks into the Si layer. Since $ErSi_2$ is a Si-diffusion type, it is difficult to silicide the total SOI layer thickness, which is effective for suppressing the short-channel effect. To sink the Schottky interface for the $ErSi_2$ MOSFETs, the SOI layer was selectively etched using tetramethyl-ammonium-hydroxide (TMAH)[19] before the deposition of Er. Figure 7 shows a cross-sectional SEM view of an $ErSi_2$ Schottky S/D MOSFET. The Schottky interface is located in the SOI layer. The (111) surface appears at the interface, because TMAH etches Si anisotropically. The gap between the gate and the S/D for the $ErSi_2$ MOSFET is controlled by the side-wall width. In this work, the gap was

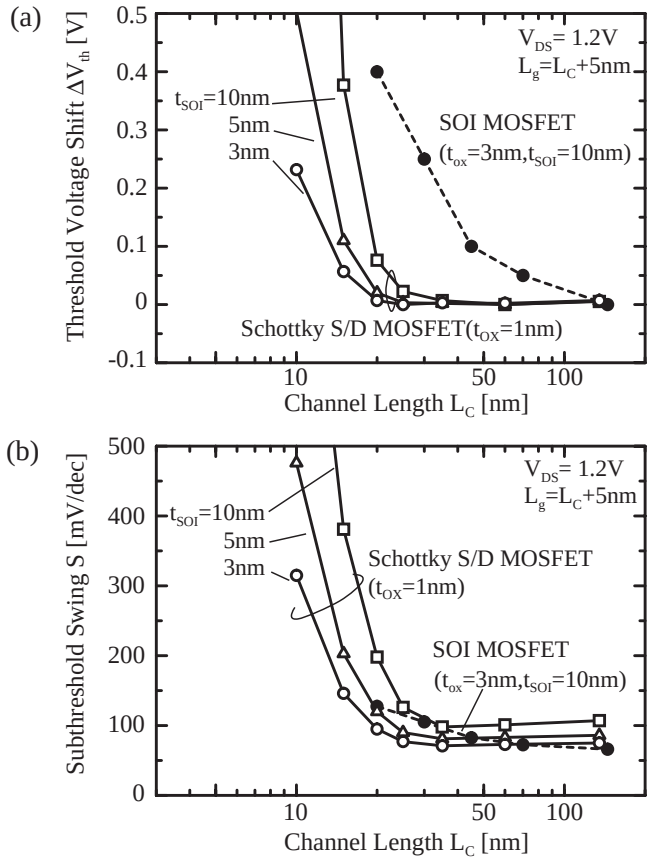

Fig. 6. Relationship between (a) threshold voltage shift, (b) subthreshold swing and channel length of Schottky S/D MOSFETs as a function of SOI layer thickness.

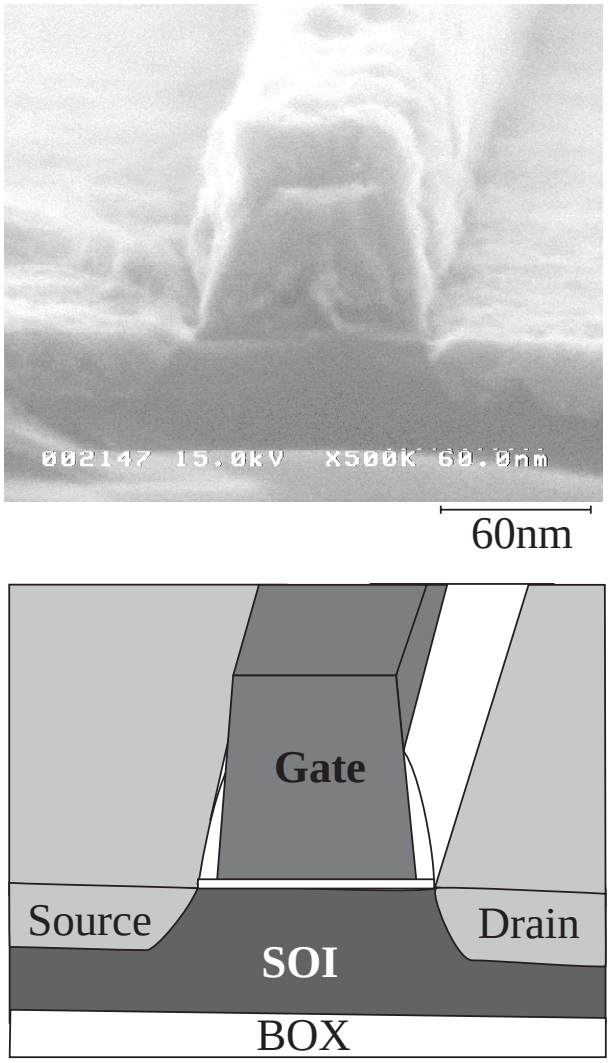

Fig. 7. Cross-sectional SEM view of $ErSi_2$ Schottky S/D MOSFET.

3.5 nm ($L_C = L_g + 7$ nm).

4.2 Measured characteristics and discussion

Figure 8 shows common-source drain curves of a n-type $ErSi_2$ Schottky S/D MOSFET on bulk Si and SIMOX substrates. The measurements were made at room temperature for various gate-source voltage V_{GS}.

At $V_{DS} = V_{GS} = 2$ V, the drain current and the transconductance of the 35-nm-long gate bulk device were 45 μA/μm and 20 mS/mm, respectively, and the drain current was 75 μA/μm and the transconductance was 9.5 mS/mm for the 25-nm-long gate SOI device. The on/off ratios were 6 and $\sim$2 for a 35 nm bulk device and a 25 nm SOI device, respectively. The drain currents for SOI devices have a leakage component which is independent of the gate voltage, as shown in Fig. 8(b). The leakage current flows from the bottom of the source/channel junction to the bottom of the channel/drain junction. The small on/off ratios are due to this leakage and the degradation of the S/D Schottky junction. It is hypothesized that there were many interface traps at the $ErSi_2$ Schottky junction and that the high density of these traps was due to interface roughness and metallic contamination. The roughness was a result of the etching to sink the interface and the RIE in CF_4 for the formation of side walls. The rough SOI surface before S/D metal deposition was observed by SEM. Moreover, the surface roughness was seen to decrease with increasing etching depth. Taking into account these considerations, the characteristics of the n-type $ErSi_2$ Schottky S/D MOSFET can be improved by changing the S/D formation process.

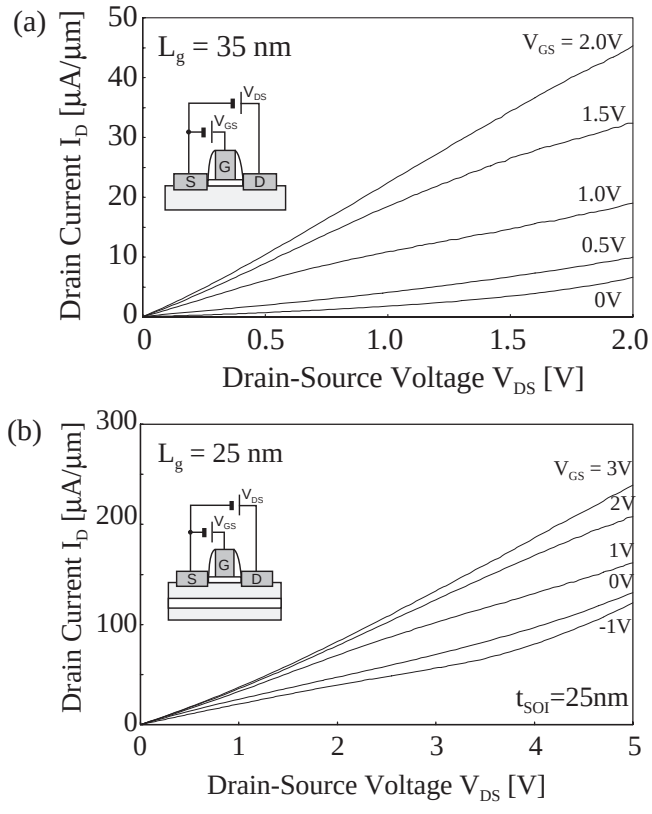

Fig. 8. Common source drain curves for various gate-source voltages V_{GS} of an $ErSi_2$ Schottky S/D MOSFET. (a) A 35-nm-long gate device on bulk substrate and (b) 25-nm-long gate device on SIMOX substrate.

5. Conclusions

Schottky source/drain (S/D) MOSFETs were analyzed theoretically. The current drivability depends on the Schottky barrier height. The drivability of the Schottky S/D MOSFET, whose channel length is less than 30 nm, is the same as that of a conventional MOSFET, when the Schottky barrier height is 0.25 eV for p-type and 0.1–0.15 eV for n-type devices, respectively. The threshold voltage shift of Schottky S/D MOSFETs is smaller than that of conventional MOSFETs, while the subthreshold swing of Schottky S/D MOSFETs is larger than that of conventional MOSFETs. To reduce subthreshold swing, the gate oxide must be thinned. The short-channel effect can be suppressed even with a 15-nm-long channel with $t_{OX} = 1$ nm and $t_{SOI} = 3$ nm.

Room-temperature operation of very short channel n-type Schottky source/drain (S/D) MOSFETs was demonstrated. For 25-nm-long gate n-type $ErSi_2$ Schottky S/D MOSFETs, the drain current was 75 μA/μm and the transconductance was 9.5 mS/mm at $V_{DS} = V_{GS} = 2$ V. The characteristics can be further improved by adopting a cleaning process before the formation of the S/D and the thinning of the SOI layer.

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Appendix A: Derivation of Equation (3)

By considering the thermal equilibrium condition at the interface between the metal and semiconductor in Fig. 2, the carrier density n at the semiconductor side is related to n_0 in the metal side as

$$n = n_0 \exp\left(-\frac{e\phi_B}{k_B T}\right). \tag{A·1}$$

n within the semiconductor side is also written as

$$n = n_i \exp\left(-\frac{E_f - E_i}{k_B T}\right), \tag{A·2}$$

where E_f is the Fermi level at the interface, E_i is the energy level at the center of the bandgap, and n_i is the intrinsic carrier density.

Combining eqs. (A·1) and (A·2) and using the relation $E_f - E_i + e\phi_B = E_g/2$, eq. (3) is derived.

Appendix B: Derivation of Equation (4)

Current density in a semiconductor is given by[9)]

$$J = e\mu\left(nF + \frac{k_B T}{e}\frac{\partial n}{\partial x}\right)$$
$$= \mu n \frac{\partial E_f}{\partial x}, \tag{B·1}$$

where μ is the electron mobility, n is the carrier density, and E_f is the quasi-Fermi level. Near the interface between the

metal and semiconductor in Fig. 2 ($x = \Delta x \simeq 0$), eq. (B·1) is approximated by

$$J \simeq \mu n \frac{E_{\mathrm{fm}} - E_{\mathrm{f}}}{\Delta x}, \tag{B·2}$$

where E_{fm} is the Fermi level of the metal.

J is also given by eq. (1) with $N = n_0 \exp\{(E_{\mathrm{f}} - E_{\mathrm{fm}})/k_{\mathrm{B}}T\}$ as

$$J \simeq RT^2 \frac{E_{\mathrm{fm}} - E_{\mathrm{f}}}{k_{\mathrm{B}}T} \exp\left(-\frac{e\phi_{\mathrm{B}}}{k_{\mathrm{B}}T}\right). \tag{B·3}$$

Combining eqs. (B·2) and (B·3), eq. (4) is derived.

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