Optical Proximity Correction Methodology to Counteract Mask Error Effects in Sub-0.25 μm Lithography Generations

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Optical Proximity Correction Methodology to Counteract Mask Error Effects in Sub-0.25 μm Lithography Generations

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A new methodology for optical proximity correction design is required for sub-0.25 μm device generation, to predict and counteract mask error effects. We applied a new concept of virtual mask technology to design an optical proximity correction (OPC), which involves adding a small dummy mask pattern on a simulation mask layout, to realize mask error effect. The aerial image simulation results for the new methodology suggested a totally different type of OPC. Experimental results were more accurately predicted by the new methodology than the old methodology. For 0.25 μm features hammerhead OPC shows much improved results of intra-field CD uniformity of 20 nm, of 3 sigma, and wide usable process window of 14% exposure latitude and 0.8 μm depth of focus, compared with serif OPC that was selected by the old methodology. This new methodology with virtual mask technology will be applied to sub-0.25 μm generations.

KEYWORDS: optical proximity correction, photolithography, simulation, DUV lithography

1. Introduction

As lithography is being scaled down to sub-0.25 μm dimensions, optical proximity correction (OPC) techniques are becoming increasingly necessary to achieve good pattern fidelity, sufficient overlay margin and improved device characteristics such as low leakage current.[1,2] Lithography simulation software is a very powerful tool for designing an OPC. We can normally select some suitable OPC candidates from different dimensions or shapes of OPCs by simulation study, without performing time-consuming experiments and analysis.[3] However, simulation predicts actual experimental results with limited accuracy because we still do not have an accurate photoresist simulation model. This is an especially serious issue in deep UV (DUV) lithography simulation due to difficulty in obtaining an accurate photoresist simulation model for the DUV chemically amplified photoresist. A chemically amplified DUV photoresist shows complex chemical reaction mechanisms like acid diffusion and post expose bake (PEB) dependence[4,5] making it very difficult to build an accurate resist simulation model. The most common method used to design an OPC for DUV has been aerial image simulation, although this indirect method is less accurate than direct photoresist simulation. We think that an improved methodology of OPC design is necessary to overcome the accuracy problem of aerial image simulation method.

The methodology should include calibration of the aerial image to the actual response of the photoresist and design of experiment (DOE) of an aerial image simulation to determine the critical dimensions of the OPC from the viewpoint viewpoint of actual photoresist bridging and process window change. Figure 1 shows our old methodology, excluding the gray box, for OPC design by aerial image simulation that has been used for our 0.35-μm static RAM (SRAM).

This methodology has been used to exactly predict the actual resist pattern for a 0.35-μm SRAM processed by I-line stepper and photoresists. However, we faced serious problems when this methodology was applied for 0.25-μm DUV lithography processes, even though our simulation model was calibrated to the DUV photoresist process. This discrepancy of OPC design results between 0.35-μm and 0.25-μm generation motivated us to look for a new methodology for sub-0.25 μm OPC design.

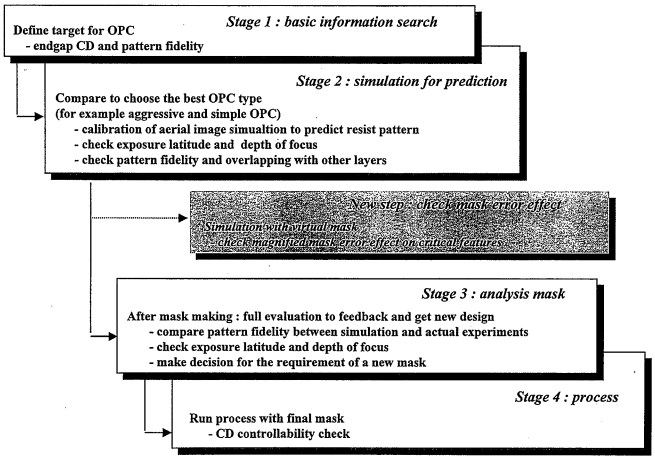


Fig. 1. Current and new methodologies after including a step to check for mask error effect by virtual mask techniques.

The main objectives of this paper are to review the design failure mode of our current methodology and to discuss a new methodology that can be applied to OPC design for sub-0.25 μm device generation.

2. OPC Design by Current Methodology and Experiment

2.1 *Requirement of OPC for 0.25-μm SRAM device*

Severe line-end shortening and rounding effect of the photoresist pattern of gate-poly are observed without OPC. The CD of the small space between two gate-poly ends (end-gap) must be tightly controlled with good pattern fidelity to achieve a better overlay margin between isolation and gate-poly or gate-poly and contact layer, as shown in Fig. 2. The end-gap CD was 0.33 μm without OPC. This is inconsistent with our specification, which is 0.27 μm$\pm$0.04 μm. The rounding of photoresist pattern in the absence of an OPC is another critical issue. It generally causes poor electrical characteristics such as low leakage margin, as well as poor overlay margin. OPC is obviously required to solve those issues. An OPC design is mainly required to achieve an exact target end-gap CD and good pattern fidelity without rounding.

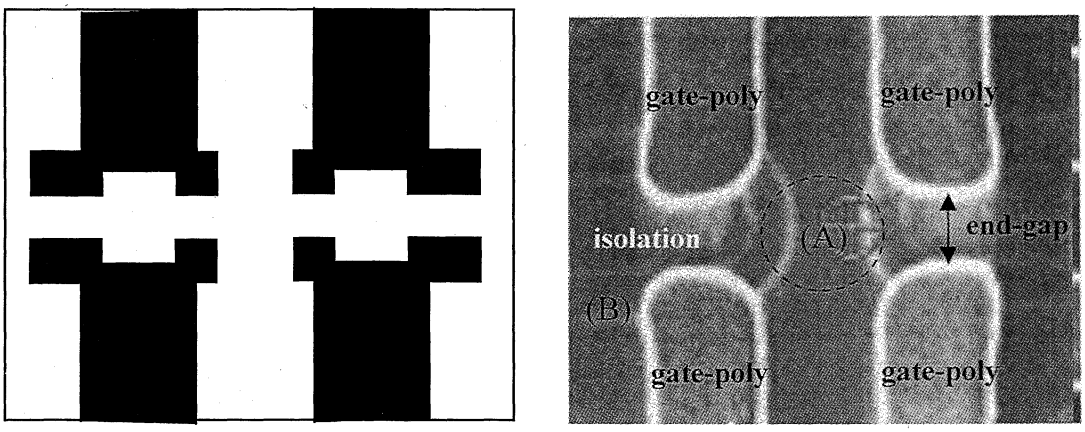


Fig. 2. Mask layout and gate-poly pattern on wafer after adding serif type OPC for 0.25 μm gate-poly.

2.2 *OPC design for 0.25 μm gate-poly layer by current methodology*

In order to design a new OPC, we followed our current OPC design methodology steps of which are shown in Fig. 1. This methodology has been used successfully for our 0.35-μm process. The first step of the methodology is collecting information of requirements such as CD and pattern fidelity. The second step is calibration of an aerial image simulation model by actual experimental data of photoresist exposure tests to get an exact aerial image simulation model. As mentioned before, we calibrated an aerial image simulation model to our current DUV photoresist. A 0.3-aerial image contour approximately makes the resist pattern under our process condition.

The next step is investigation of the aerial image profile change as a function of different OPC types and dimensions. Some suitable candidates could be selected after initial simulation. After more detailed simulation, we chose the serif type OPC shown in Fig. 2 for our gate-poly layer. The next step is more detailed simulation to check aerial image profile change at underdose and defocus conditions to ascertain that there is no bridging at end-gap which would reduce the process window size. Our simulations predicted 0.27 μm$\pm$0.04 μm end-gap CD with good resolution and process window using serif OPC.

2.3 *Experimental results and analysis*

After designing the OPC, we fabricated an actual mask to check photoresist pattern fidelity and process window. An ASM PAS5500/300 DUV stepper (maximum 0.57 NA and 0.8 σ) was used as the exposure tool. Shipley UV6, a positive-tone chemically amplified DUV resist, and Shipley AR2, an organic bottom anti-reflective coating (BARC), were coated on product wafers having actual isolation topography. CD measurements for generating ED windows were carried out by OPAL CD-SEM.

First of all, we checked pattern fidelity at the end-gap of the gate-poly by top-down SEM. As shown in Fig. 2, the pattern fidelity of the photoresist was much improved by serif OPC. End-gap CD was on target at 0.26 μm, even though it was slightly smaller than the CD predicted by aerial image simulation. The overlapping ED window of the end-gap and gate-poly was 0.8 μm DOF and was exposure latitude 14%, consistent with our requirements for CD control.

However, we found two serious problems, namely intra-field CD nonuniformity of end-gap as shown in Fig. 3, and reduction of process window as shown in Fig. 4(a). The range of intra-field CD nonuniformity of gate-poly and end-gap was beyond out specification of 15 nm as 3 sigma. They showed systematic variation from top to bottom through stepper field. We exposed more wafers by rotating the mask to separate mask variation effect and lens aberration effect. However, a similar trend of systematic CD variation was observed. This means that the systematic CD variation was mainly contributed to by mask error rather than stepper lens effect. Another problem was reduction of ED window due to end-gap bridging at underdose process condition. At the underdose condition, the end-gap CD at the bottom of the mask was too small to be resolved by stepper, even if the end-gap and gate-poly CDs were still within the specified range at the center of the mask. In Fig. 4(a), the gray background area denotes the end-gap bridging area at the bottom of the mask. The gray background area overlapped some portion of the usable process window area of the rectangular box of 14% exposure latitude and 0.8 μm depth of focus. Therefore the actual usable process window was significantly reduced due to end-gap bridging.

2.4 *Analysis to determine root cause*

Full inspection of the mask by top-down SEM was carried out to understand the root cause of this problem. The result is shown in Fig. 5(a). We can see that the actual mask pattern fidelity was very different from the mask layout that was used for aerial image simulation. We see a highly rounded corner between serif and gate-poly. Furthermore, our mask inspection results by top-down SEM revealed that curvature of rounding and size changed from top to bottom in the mask. It was generally correlated to the intra-field CD nonuniformity that we found in our experiments, even though we must still determine a more detailed correlation between mask CD and wafer CD. Another bad sign is that the influence of this mask error seems to be magnified under defocus and underdose conditions. We tried a new aerial image simulation after adjusting the simulation mask layout to approximately the

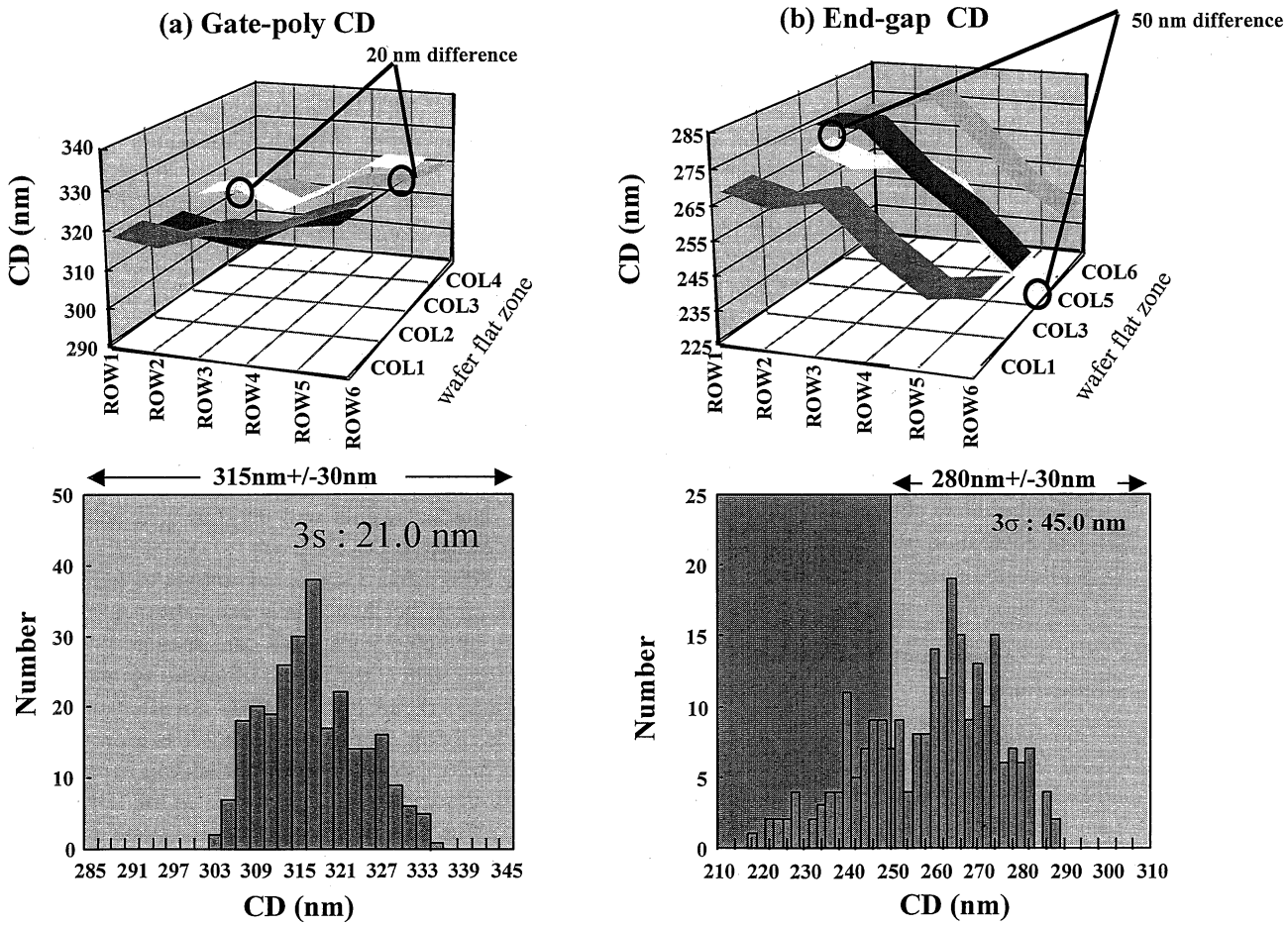


Fig. 3. Intra-field CD uniformity of gate-poly and end-gap of serif type of OPC.

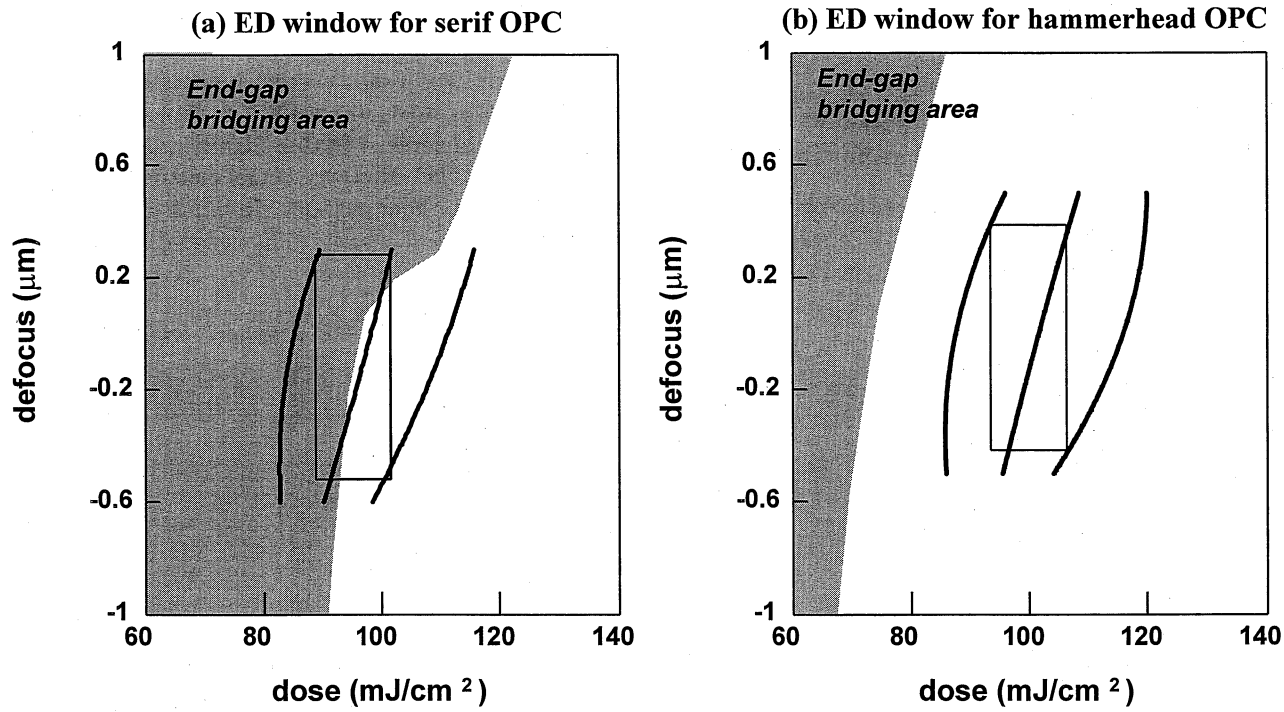


Fig. 4. ED window of gate-poly and end-gap by serif and hammerhead OPC.

actual mask pattern with rounded edges instead of vertical edges. As shown in Fig. 6(a), we added some small triangular mask patterns at the corners of the serif and gate-poly to realize mask error effect.

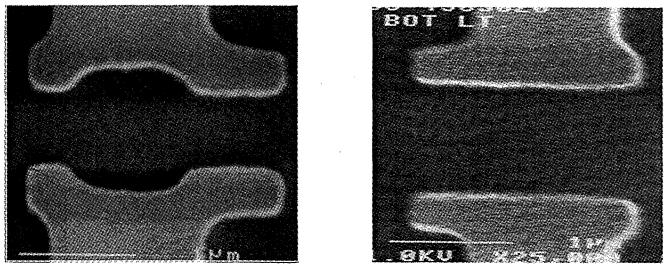
Figure 6(b) shows the simulation results of the new mask layout. At a defocus of 0.5 μm, the 0.4 aerial image intensity contour line which would define the actual photoresist pattern at the underdose condition was bridged, consistent with actual experimental results. We may conclude that the current OPC design methodology will not be applicable for 0.25-μm DUV lithography because it does not include the mask error effect. A new methodology to design an OPC for sub-0.25 μm lithography processes, including the mask error effect, definitely needs to be constructed to overcome these issues. The virtual mask concept, by the addition of some small triangular mask patterns to realize mask error effect, is very useful to simply and exactly predict the actual photoresist pattern for an OPC design for 0.25-μm generation processes. Fig. 1 shows the new methodology after including the additional simulation step with virtual mask layout, as shown in the gray box.

3. OPC Design and Experimental Results with New OPC Design Methodology

3.1 Hammerhead: new simple OPC

After developing our new OPC design methodology, we tried a new simulation to design a new OPC. We changed our mask layout from the serif type of OPC, used for 0.35-μm devices, to the simple OPC design of "hammerhead" as shown in Fig. 7(a). The reason is that the simulation results with the virtual mask layout show that we cannot achieve better results using the serif OPC, from the viewpoint of end-gap resolution across the full field and intra-field CD uniformity, even though the serif gives us good pattern fidelity at some locations of the mask. Another of our new test masks has various dimensions and locations of both hammerhead and serif type OPC, to check mask error effect such as how a wafer CD is changed by small variations of feature size and location on the mask. The results with this test mask explicitly show that the serif type of OPC is very sensitive to variations of size and location of the serif even if they are changed within mask manufacturing specifications. However, hammerhead shows only a small change of CD when mask CD and hammerhead location are changed within mask manufacturing specifications. The detailed results will be shown in another paper after further evaluation.

This new design has a strong advantage of being insensitive to mask error, because it promises absence of mask error between gate-ploy ends. We can imagine only a small mask rounding effect at the corner of gate-poly and the backside of the hammerhead, areas that will not affect end-gap CD variation or bridging. End-gap bridging was examined at underdose and defocus conditions, after adding expected mask errors on the simulation mask layout as in the left mask pattern shown in Fig. 7(a). Approximately the same aerial image profile was obtained by a virtual mask. We can clearly see the identical aerial image profile between ideal mask pattern having no mask error and virtual mask having mask errors. These results imply that the hammerhead OPC has a stable aerial image profile, even in the presence of when mask errors.

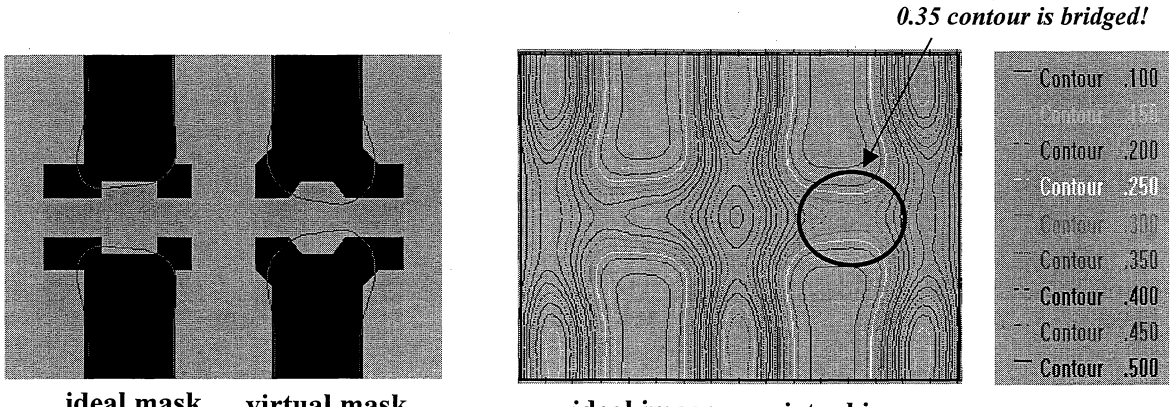


(a) serif type OPC (b) hammerhead OPC

Fig. 5. Top-down inspection results of serif and hammerhead OPC.

3.2 Enhancement of intra-field CD uniformity and process window by hammer-head OPC

The experimental results with the hammerhead OPC mask are shown in Figs. 4(b), 5(b) and 8. The photoresist pattern fidelity of the hammerhead OPC is slightly more rounded than that of the serif OPC. However, actual electrical performance was equivalent for both methods. In terms of intra-field CD



(a) mask (b) aerial Image

Fig. 6. Aerial image comparison of serif OPC without mask error (ideal mask) and with mask error (virtual mask).

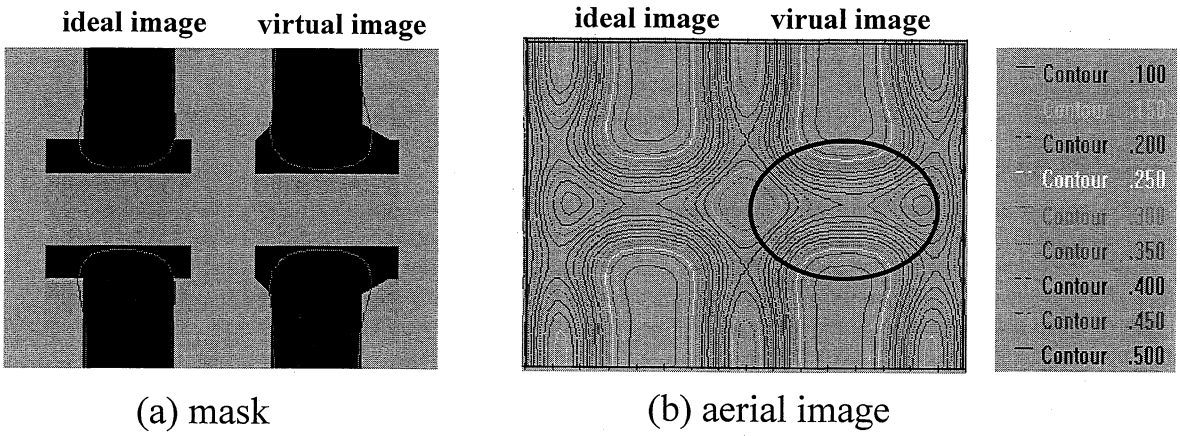


Fig. 7. Aerial image simulation results of hammerhead OPC without mask error (ideal mask) and with error (virtual mask).

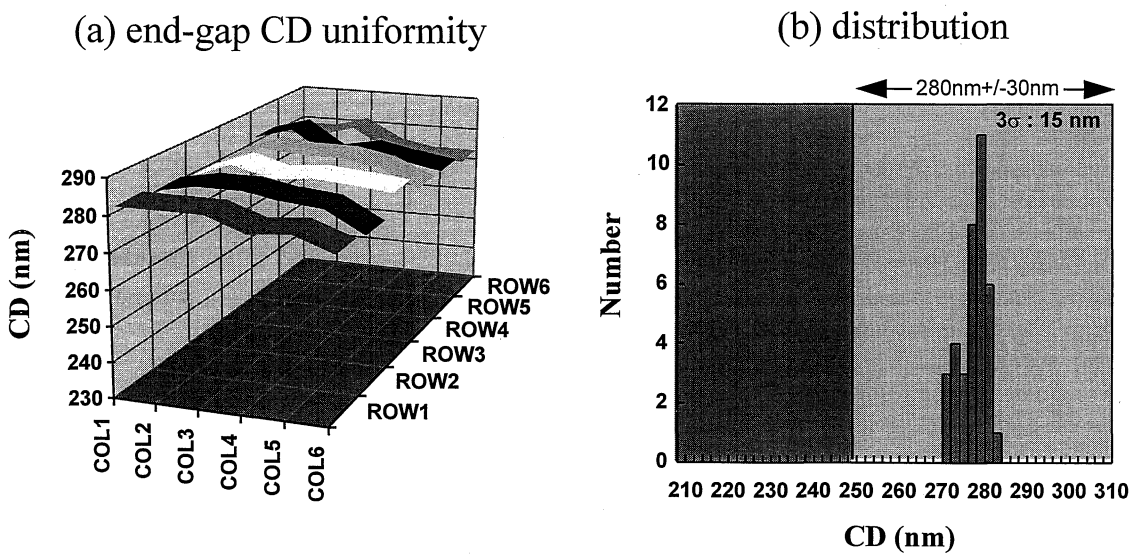


Fig. 8. Intra-field end-gap CD uniformity and distribution of hammerhead OPC.

uniformity, the hammerhead gave significantly improved results, as shown in Fig. 8. We think that this improvement is due to the small mask variation of the hammerhead. The mask pattern of the hammerhead OPC shows a very small variation as can be seeing Fig. 4(b). It is almost the same for all mask locations. This advantage directly improves intra-field CD uniformity. The ED window of a hammerhead OPC is very similar to that of serif OPC. However, we can resolve the end-gap through the process window across the entire mask. Therefore, there is no reduction of ED window size due to end-gap bridging, as seen with serif OPC. The usable ED window of the hammerhead is larger than that of the serif OPC.

4. Conclusion

In order to design an OPC for 0.25-μm gate-polys of SRAM devices, we applied our old methodology that was suitable for 0.35-μm generation devices. However, we obtained worse intra-field CD uniformity and reduced process window due to end-gap bridging, despite good photoresist pattern fidelity. Using the new methodology that included a virtual mask simulation to account for mask errors, we designed a new OPC of the hammerhead type. That hammerhead shows much improved results for intra-field CD uniformity and process window. We think that this new methodology, including the virtual mask technology, will be applicable to sub-0.25-μm device generation.

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