Use of Indium and Gallium as P-Type Dopants in Si 0.1 μ*m* MOSFETs

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Use of Indium and Gallium as P-Type Dopants in Si 0.1 μm MOSFETs

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Devices with a channel length of 0.1 μm, employing In and B as p-type channel dopants, were fabricated to investigate the short channel effect. In this study, the benefits of using In instead of B are investigated with respect to the suppression of the short channel effect, the gate quality, the mobility and the long channel threshold voltage value. It is concluded that the use of In causes no direct complications. The advantage of using In lies in the suppression of the short channel effect. In this way, the conventional planar bulk device employing In as a channel implant can be scaled further at least for one generation of metal oxide semiconductor transistors without loss in current driveability. The feasibility of Ga as an ultra shallow p-type extension is also investigated.

KEYWORDS: indium, gallium, short-channel effect, retrograde channel profile, shallow junctions

1. Introduction

Indium and gallium have been studied in the past for possible use in Si metal oxide semiconductor field effect transistor (MOSFET) technology. Although both dopants were considered to be disadvantageous because of their low solid solubility, recently a new interest has arisen in using indium for channel implantation. In the past few years a lot of effort has been devoted to solving the problems involved in scaling down the silicon MOSFET to the 0.1 μm region. Several publications[1–3] have shown that the planar bulk technology with careful S/D and channel engineering is a good candidate for ULSI systems. In particular the implementation of shallow extensions and the ground plane (GP) concept are effective in suppressing the short channel effect (SCE)[4,5] while maintaining a high current drive. They reduce the SCE by restoring the 1 dimensional potential profile under the gate, which gives rise to vertical electric field vectors. It is indeed preferable to have a way to pull down the channel electric field vertically because this prevents the lateral drain field from penetrating through the channel into the source region. The penetration of the lateral drain field lowers the barrier against diffusion of particles from the source into the channel and increases the off-state current. This is well known as drain induced barrier lowering. The use of indium as a channel profile to mimic the GP concept in an n-channe' MOS transistor has been shown several times. The feasibility of gallium as an extension in p-channel MOS transistors will be investigated here.

2. Indium as p-Type Channel Profile in nMOSFETs

Indium as a p-type dopant in Si has been studied and used in the past for infra-red detectors.[6] Antoniadis, *et al.*[7] argued on the basis of a strong oxidation-enhanced diffusivity and a rapid outdiffusion through the SiO_2 that In is not a viable alternative to B as a field region implant in a complementary MOS technology. Recently, the use of In to form a ground plane in the channel region has been demonstrated by fabricating devices. However, a more fundamental study on the impact of In on the behaviour of the nMOST has not yet been reported.

2.1 *Short channel effect*

As channel length decreases below 0.5 μm, the power supply also decreases for several reasons. As a result, the threshold voltage V_T must decrease as well in order to maintain sufficient overdrive and noise margin. The main parameter used to reduce V_T is the substrate doping N_{sub}. However, it is well known in scaling theory that, in the case of a uniform doping profile, reducing N_{sub} reduces the resistance to the short channel effect as shown in Fig. 1(a). This figure shows V_T as a function of channel length for high (N_{sub2}) and low (N_{sub1}) substrate doping. This incompatibility can be overcome by employing a highly nonuniformly doped substrate instead of a uniformly doped substrate. Whereas B gives a rather uniform channel profile because of its low mass and high diffusion constant, In gives a narrow implanted profile with a low surface concentration and a high subsurface concentration as shown in Fig. 1(b). This offers the design engineer two degrees of freedom (dose and en-

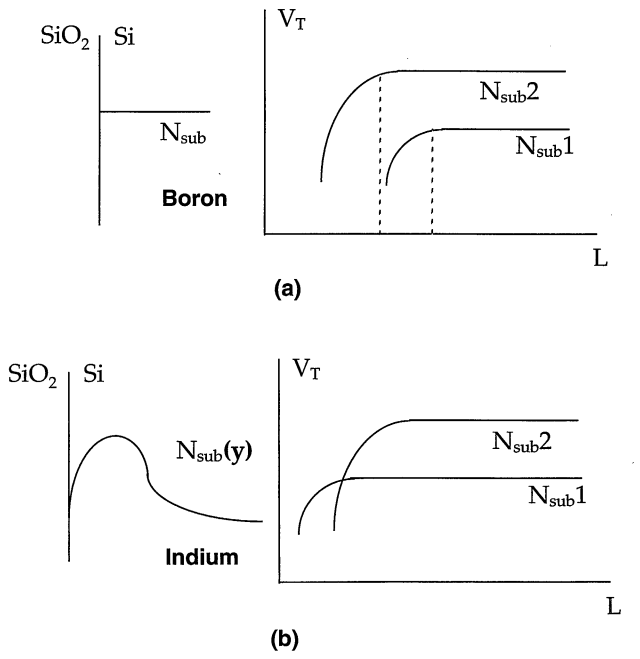


Fig. 1. (a) Threshold voltage V_T versus channel length for low (N_{sub}) and high (N_{sub2}) uniform substrate profiles. (b) Threshold voltage V_T versus channel length for uniform (N_{sub2}) and nonuniform (N_{sub1}) substrate profiles.

ergy of implantation) in the case of In compared to one (dose) in the case of B. Since after all temperature steps B gives a more or less uniform profile, the influence of the implantation energy is lost. The result of using In on V_T is shown in Fig. 1(b).

The suppression of the short channel effect in Fig. 1(b) can be understood as follows. For a uniformly doped substrate, the electrostatic behaviour is determined by the Poisson equation

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}=\frac{qN_{\mathrm{sub}}}{\varepsilon_{\mathrm{si}}} \tag{1}$$

with a constant N_{sub}, where x is the lateral and y the vertical direction. Long channel device behaviour (or V_T independent of L) is characterised by the condition $\partial^2\psi/\partial x^2=0$. The dependence of V_T on L comes from the 2-dimensional charge sharing or in mathematical terms $\partial^2\psi/\partial x^2 \sim \partial^2\psi/\partial y^2$, which means that the two terms on the left-hand side of the Poisson equation become of the same order of magnitude. To restore the 1-dimensional vertical field in the channel region, one has to increase the $\partial^2\psi/\partial y^2$ term. This can be accomplished by using nonuniform substrates, in other words, replacing eq. (1) by

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}=\frac{qN_{\mathrm{sub}}(y)}{\varepsilon_{\mathrm{si}}} \tag{2}$$

which includes a y-dependence in the right-hand side. This explicit dependence of N_{sub} on y with the specific profile as shown in Fig. 1(b) promotes the increase of the $\partial^2\psi/\partial y^2$ term and consequently reduces the short channel effect.

2.2 *Oxide quality*

In our nMOS run,[1] capacitors with an area of 14529 μm^2 and a perimeter of 508 μm on (100) Si implanted with In (10^{13} cm^{-2}, 190 keV) or B (1.5×10^{13} cm^{-2}, 35 keV) were fabricated. The thickness of gate oxide grown at 800°C is 5.5 nm. All wafers were oxidised together in the same furnace. Figure 2 shows the tunnelling characteristics for both dopants, *showing a higher breakdown field in the case of In.*

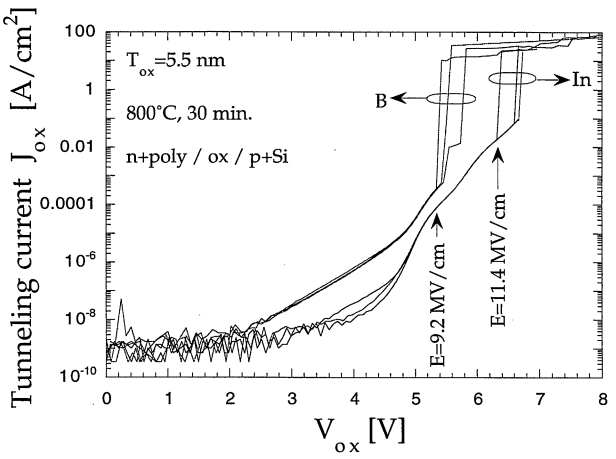


Fig. 2. Measured tunnel current density as a function of applied bias through thin gate oxide on B- and In-implanted samples.

2.3 *Effective mobility*

Figure 3 shows a plot of the effective mobility of In and B transistors against an effective field $E_{\mathrm{eff}}=(0.5Q_{\mathrm{inv}}+Q_{\mathrm{bulk}})/\varepsilon_{\mathrm{si}}$. For high E_{eff}, a universal mobility curve[8] is obtained. For lower fields, the non-universal roll-off is observed because of the oxide charges ($Q_{\mathrm{ox}}=7\times10^{10}$ cm^{-2})[9,10] which increase the Coulomb scattering. From this graph, it can be concluded that *In can safely replace B in the channel region without any loss of current drive.*

2.4 *Long channel threshold voltage*

Of particular concern is the electrical activation of the In dopants. The activation energies (E_A-E_V [eV]) for the p-type dopants are 0.046 eV (B), 0.065 eV (Ga) and 0.16 eV (In). It is apparent that In is a rather deep acceptor with a large activation energy which might lead to an incomplete ionisation of the dopant ensemble. The number of ionised dopants N_A^- can be calculated by[10]

$$N_A^-=\frac{P_\xi}{2}\left(\sqrt{1+\frac{4N_A}{P_\xi}}-1\right)$$

with

$$P_\xi=\frac{N_V}{g_A}\exp\left(\frac{E_V-E_A}{kT}\right) \tag{3}$$

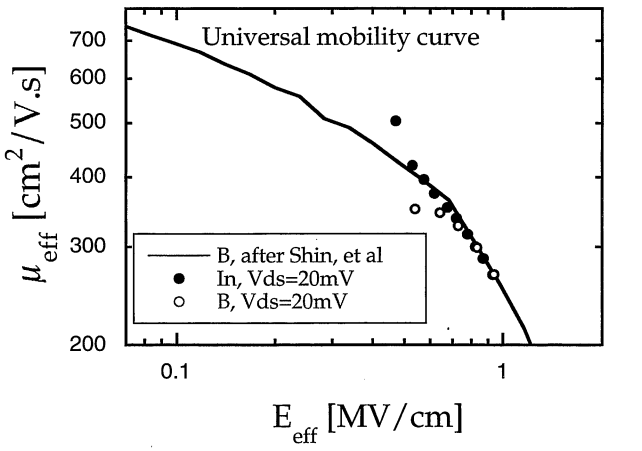


Fig. 3. Measured effective mobility for B and In devices. The solid line is the universal mobility after Shin, *et al.*[14]

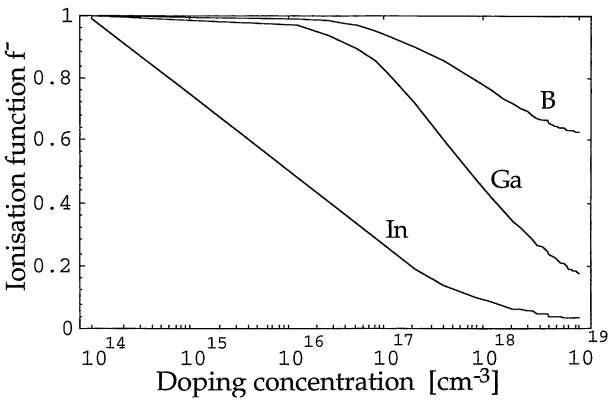


Fig. 4. Ionisation factor f_- for B, Ga and In.

with N_A being the total number of substitutional dopants and g_A the degeneracy factor ($g_A = 4$). It is assumed however that there are no interactions between the dopant ions and that there are no electric fields present.

In Fig. 4, we plot $f^- = N_A^-/N_A$, the ionisation factor, versus N_A. One can see for instance that for $N_A = 10^{18}$ cm^{-3} only 15% of the implanted dopants are ionised. It is only this portion which can apparently contribute to V_T and to the 'ground plane'-action to reduce the SCE. To verify this, we carried out a spreading resistance profiling (SRP) and a secondary ion mass spectroscopy (SIMS) measurement on an annealed Si sample implanted with In.

Figure 5 compares the SRP and SIMS measurements as well as the model for N_A^- (using the SIMS results as N_A). Clearly an inadequate ionisation (the peak concentration is reduced by a factor of 7) is observed. In this analysis, the ionisation energy E_A was considered to be constant. It has been experimentally observed for B that $E_A - E_V$ decreases[11] with increasing concentration for $N_A > 10^{18}$ cm^{-3}. For In, such a decrease is also present but less pronounced because of its low solubility. In the model we compensated for this effect by using $g_A = 1$.

However, one important issue which we ignored so far is that in a MOSFET the value of $E_A - E_F$ and consequently the number of free carriers is modulated by the gate electrode as well. The modulation makes $E_A - E_F$ negative and the exponential in the Fermi-Dirac statistic for the dopants becomes nearly equal to zero, resulting in N_A^- approaching N_A[7] and f^- approaching 1. We investigated the exact influence of the gate on the degree of ionisation by using the 2D simulator MEDICI to calculate the long channel value of V_T. Figure 6(a) shows the numbers of holes (N_{h+}) and electrons (N_{e-}) for $E_A - E_F = 0$ eV (~B) and for $E_A - E_F = 160$ mV (In), together with the chemical concentration N_A. A remarkable difference in N_{h+} for B and In is observed. N_{e-} in the case of In is a factor of 3 higher at the surface.

Figure 6(b) shows the resulting electrical potential for both cases. One can observe an increase in surface potential of about 35 mV for In, which leads directly to a reduction of V_T by nearly the same amount, or for a targeted V_T of 0.4 V that is less then 10% which can easily be accomodated for. Therefore, *the fact that In is a deep level impurity does not pose a serious problem for the V_T control.*

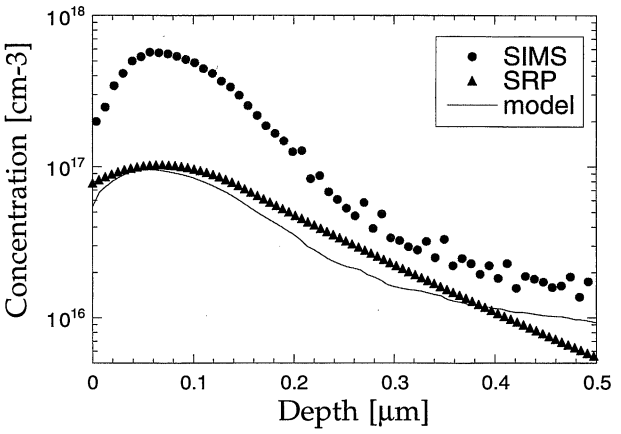
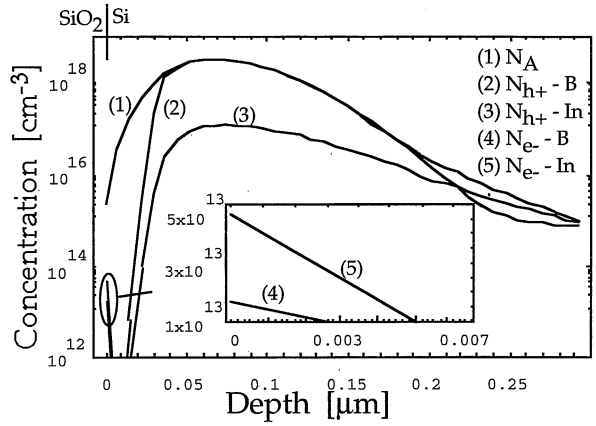


Fig. 5. Measured SIMS and SRP profiles of an In (1.5×10^{13} cm^{-2}, 190 keV, annealed in N_2 850°C 40 min)-implanted Si bulk sample to verify the model (3).

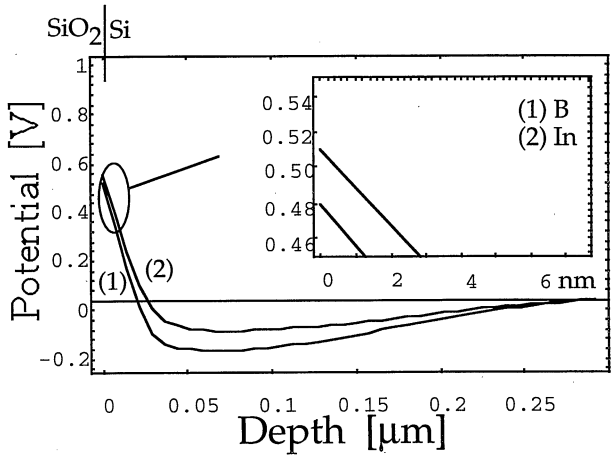
3. Gallium as Ultrashallow p-Type Extension in pMOSFETs

Gallium as a p-dopant in Si has been studied and used in the past for the fabrication of thyristors. It has had relatively little importance in CMOS because Ga has a rather low solubility in Si (2×10^{19} cm^{-3} at 1000°C)[12] and is not masked by SiO_2. The diffusion in SiO_2 was investigated in ref. 13 and it was concluded that annealing in an ambient which contains traces of H_2 significantly increases the diffusion. Furthermore, a considerable amount of dopant is evaporated except when the Ga-doped layer is capped by a Si_3N_4 layer. Therefore, in a modern planar 0.1 μm CMOS process with a reduced overall temperature budget, clean processing and nitride spacers, *Ga might again be considered for ultrashallow extensions* ($N_{ext} \leq 2 \times 10^{19}$ cm^{-3}). Because its mass is higher than that of B, it gives shallower implanted profiles and thus shallower extensions.

A concern with Ga is the evaporation from the Si lat-



(a)



(b)

Fig. 6. (a) MEDICI simulation of hole and electron concentrations for a given B or In channel profile N_A. (b) MEDICI simulation of the corresponding electrical potential.

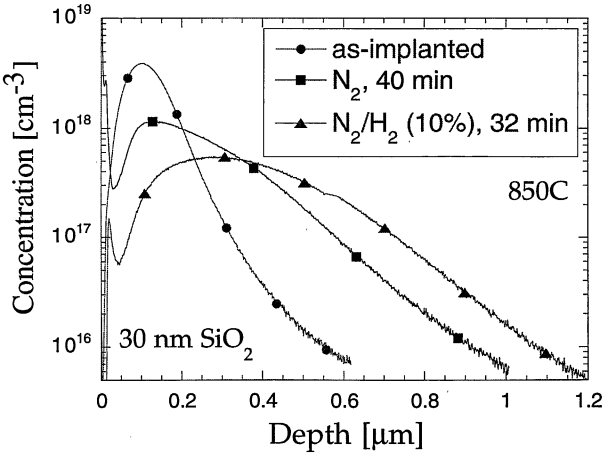


Fig. 7. Experimental curves of Ga implanted at 200 keV, 5×10^{13} cm^{-3}, annealed in N_2 and N_2/H_2.

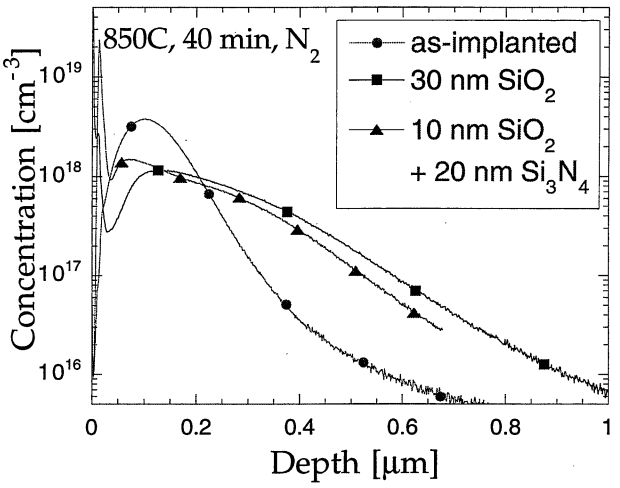


Fig. 8. Experimental curves of Ga implanted at 200 keV, 5×10^{13} cm^{-3}, annealed in N_2, with and without nitride capping.

tice. Figure 7 shows the results of an experiment where we annealed the Si substrate at 850°C for 40 min in N_2 and 32 min in forming gas with 10% H_2 to observe the evaporation. The implantation was done at 200 keV through a 10 nm thermal implantation oxide with a dose of 5×10^{13} cm^{-2}. The evaporation is calculated by integrating the curves, which gives the net doses. The results are that in the case of forming gas, 50% of the Ga dopants evaporated while only 25% were lost in N_2. Figure 8 shows the results of a similar experiment but the samples were capped by either 30 nm thermal oxide or 10 nm oxide plus 20 nm Si_3N_4. Annealing in N_2 at 850°C for 40 min results in a loss of 25% in the case of only thermal oxide while only 3% evaporates if the sample is capped by Si_3N_4. This indicates that the use of a Si_3N_4 capping layer is necessary to minimise the evaporation, together with low-temperature processing.

4. Conclusions

The advantages and disadvantages of In in comparison to B with respect to gate quality, mobility and threshold voltage were investigated. It is concluded that the gate quality of In devices is as good as or even better than that of B devices. Concerning the mobility, the much heavier element In seems to yield equally good mobility curves. Furthermore, it was shown that, although In forms a rather deep impurity level, it reduces V_T by less than 35 mV. The feasibility of Ga as a p-type extension was investigated and it was concluded that Ga can only be used in a low-temperature-budget process with Si_3N_4 spacers.

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