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2D Materials

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Electrical characterization of 2D materials-based field-effect transistors

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Abstract

Two-dimensional (2D) materials hold great promise for future nanoelectronics as conventional semiconductor technologies face serious limitations in performance and power dissipation for future technology nodes. The atomic thinness of 2D materials enables highly scaled field-effect transistors (FETs) with reduced short-channel effects while maintaining high carrier mobility, essential for high-performance, low-voltage device operations. The richness of their electronic band structure opens up the possibility of using these materials in novel electronic and optoelectronic devices. These applications are strongly dependent on the electrical properties of 2D materials-based FETs. Thus, accurate characterization of important properties such as conductivity, carrier density, mobility, contact resistance, interface trap density, etc is vital for progress in the field. However, electrical characterization methods for 2D devices, particularly FET-related measurement techniques, must be revisited since conventional characterization methods for bulk semiconductor materials often fail in the limit of ultrathin 2D materials. In this paper, we review the common electrical characterization techniques for 2D FETs and the related issues arising from adapting the techniques for use on 2D materials.

1. Introduction

Two-dimensional (2D) van der Waals materials or layered materials are characterized by materials with an anisotropic electronic and chemical structure of strong covalent bonds along the in-plane direction and weak van der Waals bonds along the out-of-plane direction. Among such materials, graphene has been studied most extensively, due to its high mobility, widely tunable carrier concentration, and the occurrence of phenomena such as the quantum Hall effect in atomically thin samples prepared by a simple Scotch tape exfoliation method [1–3]. Subsequently, the development of large-scale chemical vapor deposition (CVD) graphene synthesis has enabled the fabrication of wafer-scale electronic and photonic devices [4, 5]. Meanwhile, theoretical studies on carrier transport in graphene have inspired experimental research in the fields of condensed matter physics, semiconductor nanoelectronics, photonics, and energy storage [6–8].

In addition to graphene, other 2D materials have been investigated with great intensity for future electronic and optoelectronic applications [9–14], as these materials offer a range of bandgaps with high carrier mobility and efficient electrostatic control. These properties, combined with mechanical flexibility [15–18] and tunability of electronic properties, make 2D materials especially promising as a channel material in high-performance 2D field-effect transistors (FETs), which could be operated in emerging future mobile and IoT environment [19–23]. In light of this, accurate characterization of 2D FETs and extraction of important device parameters, such as resistivity, carrier density, mobility, contact resistance, charge trap densities,

dielectric permittivity, and anisotropy in carrier transport, are essential to explore 2D materials and to correlate them with the performance of 2D FETs [24–27].

A mainstay of 2D materials-based semiconductor device research focuses on developing FETs with high ON/OFF ratios, high conductivity, high carrier mobility, and low power consumption [24, 25, 28–30]. It is critically important to understand the electrical properties of such devices, since the use of conventional electrical characterization methods can produce unreliable results when applied to ultra-thin 2D layered materials. For example, room-temperature electrical conductivity in a bulk semiconductor is directly related to charge carrier density. However, conventional implanted substitutional doping cannot be performed on 2D materials due to their atomic thinness. Instead, different methods, such as charge transfer doping, are predominantly used to generate electron and hole carriers in 2D materials [31–33], and in few-layer materials, the charge density falls off rapidly away from the surface, rather than being uniform as in conventional semiconductor materials.

Furthermore, the pristine surface of 2D materials forms weak van der Waals bonds with adjacent materials and presents challenges to the creation of low-resistance contacts, by introducing a tunnel barrier for charge carrier transport, whereas the formation of stronger bonds requires disruption of the 2D crystal structure, which introduces defect states. Therefore, it is important to accurately characterize the properties of metal contacts, e.g., contact resistance and metal-semiconductor Schottky barrier [34]. Interfaces between 2D semiconductors and metals are subject to Fermi level pinning due to the tunnel barrier at the interface, defect-induced interface states, and orbital overlap between adjacent heterogeneous materials, requiring precise characterization of the Schottky barrier and Fermi level pinning, which could severely increase the contact resistance at the interfaces [35].

In this review, conductivity, carrier density, mobility, Schottky barrier height (SBH), contact resistance (R_C) and trapped charges are discussed as key parameters for the electrical characterization of 2D devices, constituting the main sections below. Figure 1 illustrates the representative parameters that can be extracted by various electrical characterization methods, including current–voltage (I–V), Hall effect, capacitance–voltage (C–V), and 4-point probe (4PP) measurements, as well as the transmission line method (TLM). Moreover, we also address the correlation between these macroscopic device parameters and the nanoscale properties of 2D materials, visualized using scanning probe microscopy (SPM) techniques.

2. 2D devices

2.1. 2D FETs

The basic structure of a FET comprises of a metallic gate, a semiconductor channel between the source and drain electrodes, and an insulating gate oxide (the barrier between the channel and gate). The current flow in the semiconductor channel (drain current, I_D) is established by the source–drain voltage (V_{DS}) and is modulated by the applied gate voltage (V_{GS}) by changing the conductivity of the channel region. Figure 2(a) shows schematic and circuit diagrams of a typical back-gated 2D FET with metallic source and drain contacts and hexagonal boron nitride (hBN) encapsulation [36]. Unlike conventional bulk semiconductor FETs, the presence of metallic electrodes at the source–drain junctions results in Schottky contacts due to a lack of efficient doping techniques. Moreover, back-gated 2D FETs currently in the research stage consist of thick gate-oxides (e.g. ~300 nm) that require large gate voltages (e.g. >10 V) to switch the device from the OFF to ON states. Besides, back gating affects both the channel and contact regions in a convoluted manner that complicates the gating characteristics of 2D FETs. In this section, we discuss the output and transfer characteristics of back-gated 2D FETs and provide insights into the extraction of fundamental device parameters.

2.2. Current–voltage characterization

I–V measurement is the fundamental electrical characterization technique for understanding the working principle of FETs. Also, I–V measurements allow for qualitative and quantitative understanding of intrinsic semiconductor properties such as mobility and carrier density, along with external properties such as interface states and contact resistance. Here, we discuss typical I–V measurement of a 2D FET; the performance of the FET is characterized primarily by measuring the output (I_D as a function of V_{DS}) and transfer (I_D as a function of V_{GS}) characteristics.

2.2.1. Output characteristics

To measure the output characteristics of a FET, the drain current is measured as a function of V_{DS} at different V_{GS}. The output characteristics with a small V_{DS} (figure 2(b)) allow the extraction of important FET parameters as the device acts as a linear resistor in this region. Assuming channel-dominated behavior, the I_D for an n-type 2D FET in the linear regime can be expressed as

$$I_D = \frac{\mu_n W C_{ox}}{L}\left[\left(V_{GS} - V_{TH}\right) V_{DS}\right], \qquad (1)$$

where L, W, μ_n, C_{ox}, and V_{TH} are the channel length, channel width, channel electron mobility,

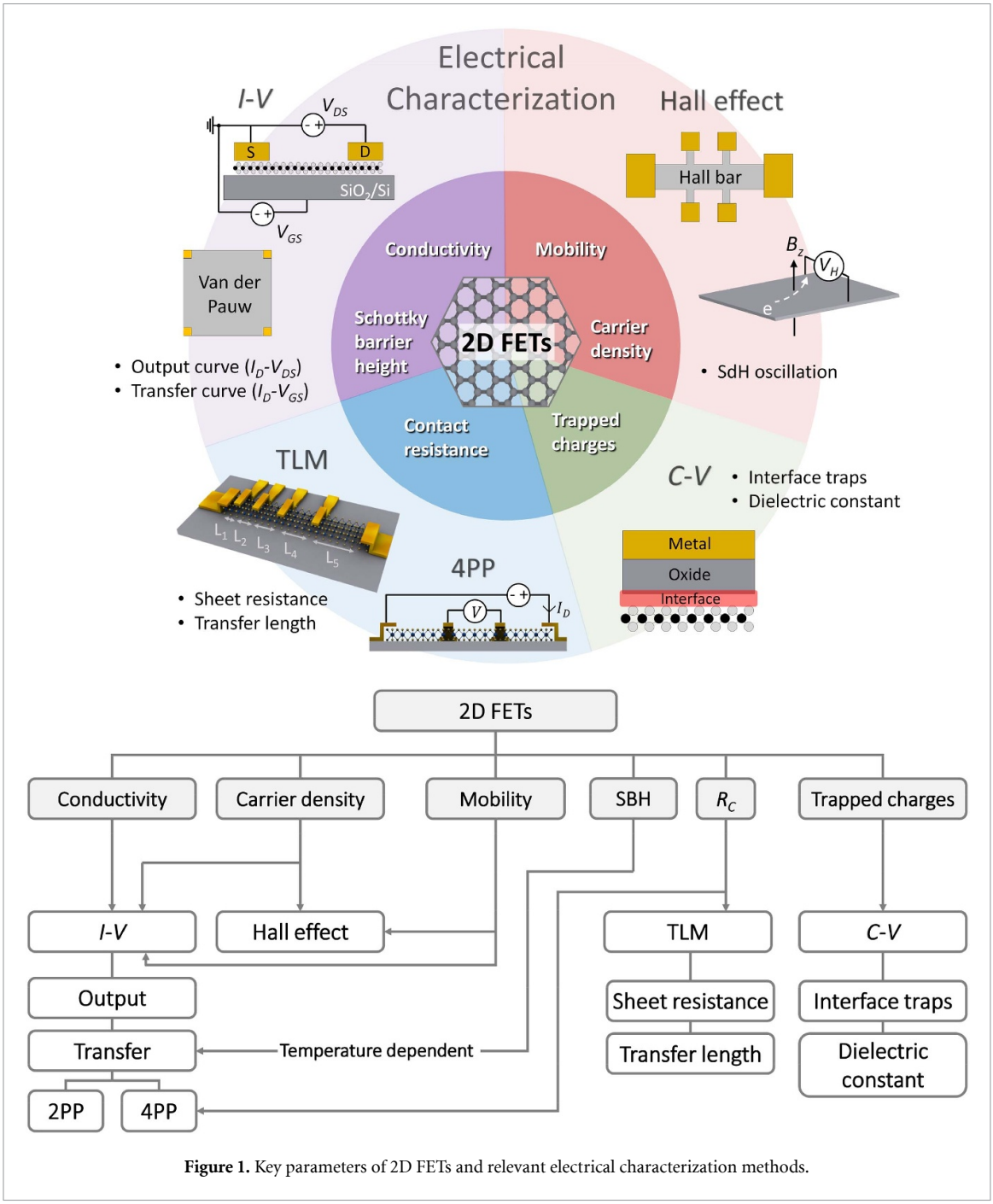

Figure 1. Key parameters of 2D FETs and relevant electrical characterization methods.

oxide capacitance, and the threshold voltage, respectively. We discuss the use of equation (1) to extract the channel mobility and carrier density in the following sections.

In the presence of R_C, only a portion of V_{DS} drops across the channel; thus, equation (1) needs to be further modified to address this issue. The effect of R_C can be included straightforwardly by replacing V_{DS} with

$$I_D = \frac{\mu_n W C_{ox}}{L}\left[(V_{GS} - V_{TH})\left(V_{DS} - I_D \cdot 2R_C\right)\right] \quad (2)$$

Here, $2R_C$ refers to the contact resistance for the source and drain junction at small V_{DS}. However, the presence of a global back gate (V_{BG}) in 2D FETs results in simultaneous gating of the contact region, making R_C, a function of V_{GS} and V_{DS}. Thus, the linearity of the output characteristics can be used as a simple yet important check to determine the effect of contact resistance on FET performance. Note that, due to the simultaneous gating of the contact and channel regions, contacts can show different behavior (Ohmic or Schottky) at different gate voltages. However, the linear behavior does not provide any information regarding the mechanism behind the Ohmic nature of contacts as doped (gated) Schottky contacts can resemble Ohmic characteristics due to enhancement of the tunneling component at the source junction

[37]. Thus, proper extraction of μ_n, V_{TH}, and R_C is essential to understanding current flow in 2D FETs. The extraction of these parameters is discussed in the following sections.

For use of 2D FET in analog, digital, and high power applications, observations of current saturation over a large V_{DS} window is crucial [39, 40]. The current saturation region is characterized by a constant I_D independent of V_{DS}, as shown in figure 2(c); I_D initially increases linearly with V_{DS} (linear regime) and then saturates at higher V_{DS}. Although several reports have demonstrated current saturation in various transition metal dichalcogenide (TMDC) (e.g. MoS_2, WSe_2, WS_2) FETs [28, 41–44], obtaining saturation in 2D devices at desirable values of V_{DS} still remains elusive due to large contact resistance, low channel mobility, and high-field scattering. The application of high electric field without those effects was realized by employing ionic gated transistors [45, 46], although it is difficult to use the ionic transistors for practical purposes. Lack of bandgap, weak electrostatic control, and interfacial phonon scattering in graphene are responsible for the poor current saturation seen in graphene FETs (shown in figure 2(d)), which limits their usability in radio frequency applications [38, 47, 48].

2.2.2. Transfer characteristics

The other way to assess the electrical performance of a FET is by utilizing the transfer characteristics that can be obtained by measuring I_D as a function of V_{GS} at constant V_{DS}, as illustrated in figure 2(e). These characteristics are used to extract the parameters, such as transconductance ($g_m = \frac{dI_D}{dV_{GS}}$), threshold voltage ($V_{TH}$—the gate voltage at which the FET turns on), and subthreshold swing (SS—the value indicating the sharpness of switching behavior of the 2D FET), as shown in figure 2(f). For an n-channel FET (n-FET), the transfer characteristics display ON-state current (I_{ON}) for $V_{GS} = V_{DD} > V_{TH}$ (V_{DD} is the maximum voltage supplied to the device) and OFF-state current (I_{OFF}) for $V_{GS} < V_{TH}$, and vice versa for a p-FET. Various methods are employed to extract the V_{TH} from the transfer characteristics, such as linear region extrapolation, transconductance linear extrapolation (V_{GS} versus g_m), second-derivative of transconductance, and Ghibaudo's method (intercept of V_{GS} versus $I_D/g_m^{0.5}$) [49]. The right y-axis in figure 2(f) displays the g_m curve as a function of V_{GS}.

Scaling down the power supply voltage is critical for energy-efficient electronics, and one of the most effective ways to control the power density is to lower the supply voltage. To reduce power consumption, it is necessary to overcome the abruptness (thermionic limit of 60 mV/decade) that originates from the thermal carrier injection mechanism, i.e., thermionic emission (TE). The abruptness of a FET is measured by SS, which is defined as the inverse of the slope of $\log(I_D)$ versus V_{GS} curve. The SS determines the gate efficiency of tuning the energy barrier at the source terminal. A small SS over a wide range of current is required to achieve, since it indicates a large I_{ON}/I_{OFF} ratio for small supply voltages.

In the subthreshold regime or OFF state ($V_{GS} < V_{TH}$), the subthreshold current is limited by thermal injection of carriers at the source junction and can be expressed as:

$$I_D \sim e^{\frac{q(V_{GS}-V_{TH})}{k_B T}} \tag{3}$$

where q is the elementary charge, k_B is Boltzmann's constant, and T is temperature. The SS can be obtained from (3), as follows:

$$SS = \frac{dV_{GS}}{d(logI_D)} = \ln(10)\frac{k_B T}{q}\left(1 + \frac{C_{CH}}{C_{ox}}\right) \tag{4}$$

where $\frac{k_B T}{q}$ is the thermal voltage, C_{CH} is the channel capacitance and C_{ox} is the oxide capacitance. For an ideal 2D FET, $C_{CH} \ll C_{ox}$ in the subthreshold region and thus SS is ~60 mV/decade at room temperature. However, most 2D FETs are fabricated on thick SiO_2 substratewith large interface trap density, yielding large SS values (> a few hundred mV/decade). Although unrealistic in practical applications, large C_{ox} can be realized by using ionic gated transistors that results in SS values very close to 60 mV dec^{-1} despite using 2D Schottky devices [46, 50] and also mobility values close to the limitation by phonon scattering [51], making the ionic transistors efficient to quantitatively characterize the electronic properties of 2D materials. The interfacial traps between 2D channels and SiO_2 also induce unwanted hysteresis in the transfer characteristics [52, 53]. This can be improved by stacking or encapsulating of the 2D materials with an insulating 2D material such as hBN [54–58]. Moreover, a sub-thermionic transistor mechanism such as quantum mechanical band-to-band tunneling can exhibit a steep turn-on with low SS values far below the thermionic limit [59, 60].

3. Conductivity (resistivity)

3.1. Conductivity in 2D materials and devices

In an isotropic three-dimensional (3D) material, the electrical resistivity (ρ) and conductivity (σ) are defined as $\rho = \frac{1}{\sigma} = R \times \left(\frac{A}{L}\right)$ [Ω·cm], where R, A, and L are the total resistance, cross-sectional area ($= W \times t$, where W is the width and t is the thickness of the material), and distance between the measuring points, respectively. Conductivity measurements in bulk semiconductors can be made without fabricating any electrical contacts using standard multipoint resistance measurements; however, the very nature of 2D materials necessitates the formation of electrical contacts in 2D devices to determine resistivity or conductivity [61]. Several studies on thick 2D materials-based devices have demonstrated superlinear behavior ($\sigma \propto t^{-k}$) of electrical conductivity as

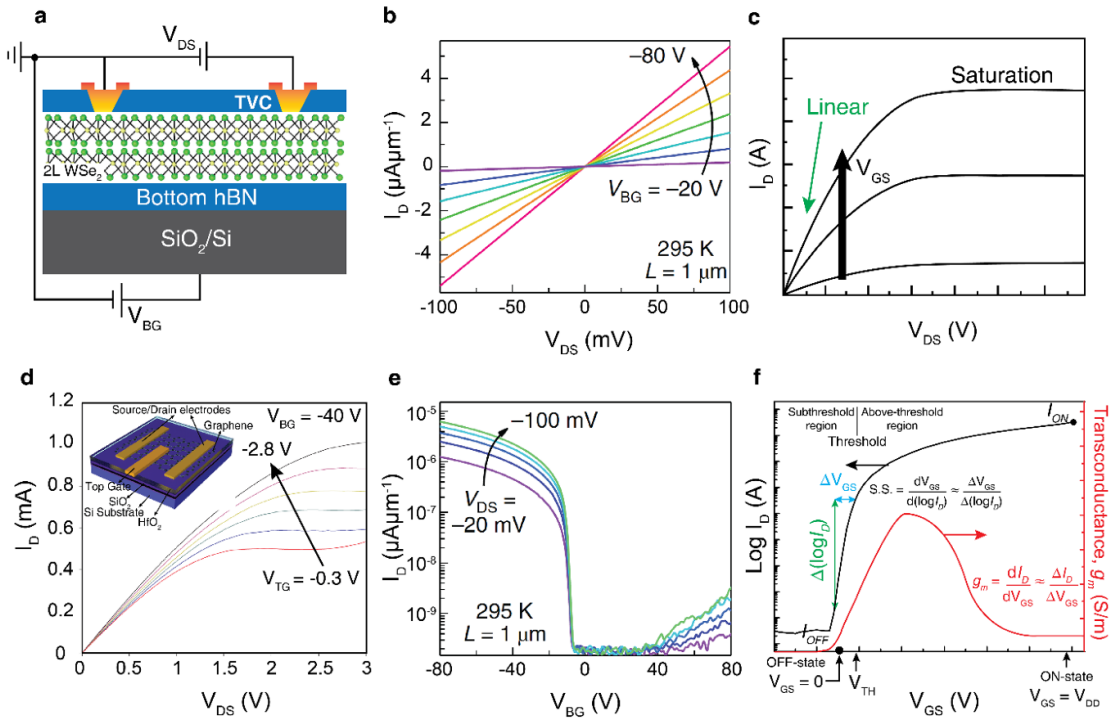

Figure 2. (a) Schematic diagram of a typical back-gated bilayer WSe_2 device with Pt transferred via contacts (TVCs). (b) 2-probe output characteristics measured at different gate voltages. The linear trend indicates the presence of Ohmic contacts at higher gate voltages [36]. (c) Illustration of the ideal output characteristics (with increasing V_{GS}) of an n-type FET displaying drain current saturation. (d) I_D as a function of V_{DS} for top gate voltage (V_{TG}) = − 0.3 V, − 0.8 V, − 1.3 V, − 1.8 V, − 2.3 V, and − 2.8 V at V_{BG}= − 40 V for the graphene FET shown in the inset [38]. (e) Transfer characteristics of the WSe_2 device showing good subthreshold swing and low drain-induced barrier lowering [36]. (f) Transfer curve (left) and transconductance (g_m) (right) characteristics of an ideal *n*-type FET with respect to V_{GS}. For a better FET switch-on characteristic, the slope in the subthreshold region ($V_{GS} < V_{TH}$) should be sharp. The transistor is switched on when V_{GS} is equal to the maximum voltage supplied to the device, V_{DD}.

a function of sample thickness [62, 63]. The super-linear behavior in such structures is attributed to the non-uniform current distribution in thick 2D materials that results from gate-dependent carrier density profile and interlayer resistance [37]. This is further accentuated at the limit of 2D materials (~10 layers in the study cited here) where conductivity is observed to exhibit non-monotonic thickness dependence due to the interplay between mobility and carrier density [64]. Besides, conductivity in 2D materials also shows a large degree of inter-sample variation due to unintentional doping from substrate , ambient surroundings, and sample preparation methods [65–68]. Therefore, the conductivity/resistivity of few-layer 2D devices is determined in terms of channel resistance (R_{CH}) or sheet resistance (R_{SH}), which is a more straightforward way to evaluate current flow in 2D materials. Typically, R_{CH} and R_{SH} can be determined by fabricating 2D FETs and measuring the output/transfer characteristics at varying V_{GS} using either a 2-point probe (2PP) or 4PP technique, as discussed in the following sections.

3.2. 2-point probe measurements

Standard 2PP measurements refer to measurements in which the current and voltage are assessed and applied by the same terminals. Over time, 2PP measurement has become a standard method of obtaining the output and transfer characteristics of a 2D FET. Figure 3(a) displays the individual components of the total resistances (R_{Total}) in a ReS_2-based 2D FET; the corresponding 2PP output characteristics at different V_{GS} are illustrated in figure 3(b) [69]. Assuming $R_{CH} > R_C$ along with linear I_D *vs.* V_{DS} characteristics, R_{CH}, R_{SH}, and σ can be determined by using the following relationship:

$$R_{CH} = R_{SH}\frac{L}{W} = \frac{1}{\sigma\, t_{CH}}\frac{L}{W} \tag{5}$$

where t_{CH} refers to the thickness of the 2D semiconducting channel. The presence of back gate results in gate voltage-dependent R_{CH} values indicating the gating behavior of channel conductivity. Similar results can also be obtained from the transfer characteristics, which provide gate-dependent R_{CH} at constant V_{DS}. However, in many cases, the contact resistance in back-gated 2D FETs is either comparable to or higher than the channel resistance, resulting in significant errors in the R_{CH} value extracted using 2PP measurements [72]. This issue can be resolved by using 4PP method, which can deconvolute the effect of R_C on the extracted R_{CH} and R_{SH} values [73, 74].

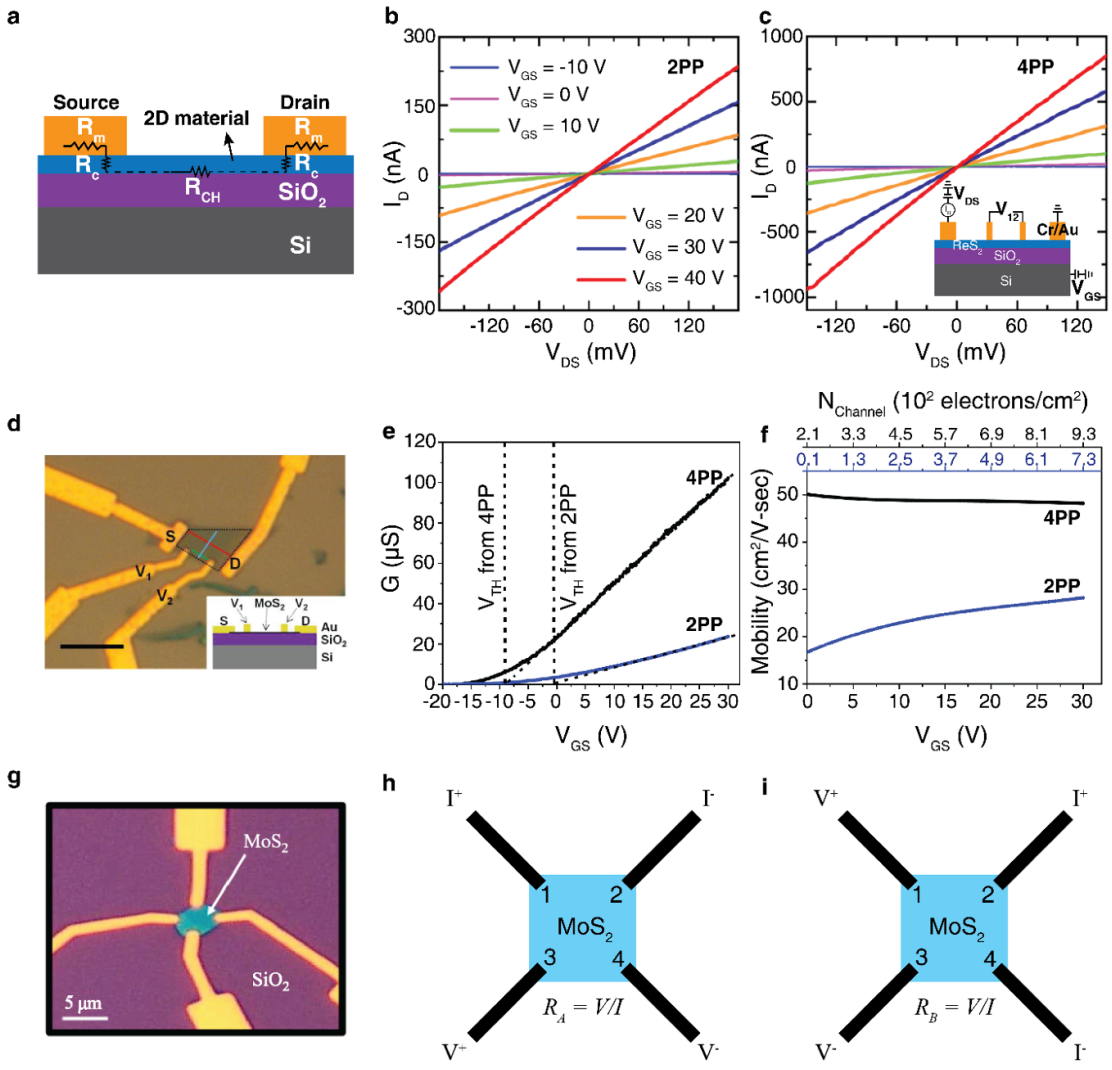

Figure 3. Differences between 2PP and 4PP measurements. (a) Schematic illustration of the R_{Total} in the 2D transistors, which consists of the R_{SH}, R_C, and resistance of the metal (R_m). (b), (c) Comparison between 2PP and 4PP measurements, respectively, of I_D as a function of the V_{DS} for a few-layered ReS_2-FET device [69]. (d) Schematic of a monolayer MoS_2 device with 4PP contact configuration. (e) 2PP and 4PP conductance, which shows different V_{TH} readings due to differences in channel and contact gating. (f) Higher mobility in 4PP measurements illustrating the impact of contact resistance [70]. (g) Schematic of a multilayer MoS_2 device with van der Pauw contact configuration [71]. (h), (i) Different van der Pauw configurations for measuring the sheet resistance of the same MoS_2 device at different gate voltages.

3.3. 4-point probe measurements

As discussed above, 2D devices suffer from large contact resistances, which make it difficult to explore channel-dominated behavior and result in wrong inferences. Here, 4PP measurements are used to measure R_{CH} independent of R_C. Figure 3(c) shows the output characteristics of a ReS_2 device obtained using 4PP measurements, which reveal a higher device current at the same V_{DS} when compared to 2PP measurements. The inset in figure 3(c) illustrates the schematic and equivalent circuit of the 4PP structure used for the measurement. Accurate conductivity measurements using the 4PP method are typically enabled by the Hall bar and van der Pauw geometry, as addressed below, which can be extended further to determine carrier density and mobility from magneto-transport measurements.

3.3.1. 4PP measurements with hall bar geometry

Generally, 4PP measurements in 2D materials-based devices are done on devices in which the contacts and channel region are patterned in a Hall bar geometry, as shown in figure 3(d) [70]. In this structure, the voltage probes (other than the source and drain contacts) minimally affect the current flow in the channel material and thus act like perfect voltmeters. The source and drain (S/D) probes are used to source/measure I_D, and V_1 and V_2 between S/D are used to sense the voltage difference ($V_{12} = |V_2 - V_1|$); in turn, these measurements are used to evaluate the intrinsic transport properties of 2D materials by deconvoluting the effects of R_C. Compared to the 2PP measurements, the 4PP measurements result in smaller R_{CH} as only a portion of applied V_{DS} drops across the channel region. Here, R_{CH} can be extracted from

the 4PP I–V characteristics by using the following relation:

$$R_{CH} = \frac{V_{12}}{I_D}\frac{L}{L_{12}} \tag{6}$$

where L_{12} is the distance between voltage probes in the middle of the device. Consequently, R_C-corrected R_{SH} and σ values can be calculated from equations (5) and (6). Finally, the 4PP characteristics can also be used to calculate R_C by subtracting the extracted R_{CH} value from R_{Total}. Thus, 4PP measurements provide an easy and efficient means of extracting both R_{CH} and R_C.

The 2PP and 4PP measurements of the transfer characteristics of a 1L-MoS_2 device are shown in figure 3(e). These measurements provide different values of V_{TH} (using the linear extrapolation method), which implies different gating properties of the channel and the contact regions due to differences in the band movements in the channel and contact regions [75]. Figure 3(f) shows higher 4PP- than 2PP-mobility due to the presence of substantial contact resistance. The results show that 4PP measurements are necessary to accurately calculate the intrinsic conductivity, unveiling true channel mobility, carrier density, and contact resistance as discussed in later sections.

3.3.2. 4PP measurements with van der Pauw geometry

Because exfoliated 2D materials come in irregular shapes, 4PP measurements with Hall bar geometry generally require reshaping of the channel material; this involves fabrication steps that could alter their intrinsic properties as 2D materials are highly sensitive to surface treatments. In this respect, the van der Pauw method is advantageous for measuring the sheet resistance of graphene and 2D materials as it does not require channel patterning in regular shapes [76].

In van der Pauw measurements, four contacts are placed at the edges (periphery) of a flake as shown in figures 3(g)–(i); a constant current flows between adjacent pair of contacts (1–2 or 2–4), and the voltage drops are measured between another adjacent pair of contacts (3–4 or 1–3). Although van der Pauw measurements for bulk semiconductors do not require channel reshaping, typical Van der Pauw measurements for 2D materials often utilize regular-shaped flakes (or flakes patterned in regular shapes, e.g. square, rectangular, or circular shapes) due to the convenience in analyzing experimental results. For a square channel geometry, two sets of measurements are performed to include vertical and horizontal conduction in the flake , resulting in the following sets of resistances:

$$\begin{aligned}
&\text{Set A (horizontal)}: R_{12,34} = \frac{V_{34}}{I_{12}}, R_{21,43} = \frac{V_{43}}{I_{21}},\\
&R_{34,12} = \frac{V_{12}}{I_{34}}, R_{43,21} = \frac{V_{21}}{I_{43}}\\
&\text{Set B (vertical)}: R_{13,24} = \frac{V_{24}}{I_{13}}, R_{31,42} = \frac{V_{42}}{I_{31}},\\
&R_{24,13} = \frac{V_{13}}{I_{24}}, R_{42,31} = \frac{V_{31}}{I_{42}}
\end{aligned} \tag{7}$$

Then, an average resistance is calculated for sets A and B, which can be expressed as:

$$\begin{aligned}
R_A &= \frac{(R_{12,34} + R_{21,43} + R_{34,12} + R_{43,21})}{4},\\
R_B &= \frac{(R_{13,24} + R_{31,42} + R_{24,13} + R_{42,31})}{4}.
\end{aligned} \tag{8}$$

Finally, sheet resistance and conductivity are calculated using the following relation:

$$e^{-\pi R_A/R_{SH}} + e^{-\pi R_B/R_{SH}} = 1 \text{ and } \sigma = \frac{1}{R_{SH}\cdot t_{CH}} \tag{9}$$

Similar expressions can be obtained for other channel shapes [77]. Since contact resistance is usually large in TMDC 2D FETs, accurate extraction of R_{CH} and R_C using van der Pauw measurements becomes highly difficult even after reshaping the flakes in regular forms. Thus, the 4PP measurements using Hall bar geometry are more prevalent in the 2D community.

3.4. Challenges of 4PP measurements

Although 4PP measurements are a powerful tool for the electrical characterization of 2D materials-based devices (electrical conductivity in this section), certain experimental considerations need to be satisfied to ensure accurate measurements and data extraction.

(i) Accurate 4PP measurements require the channel region to be patterned (reshaped) in a way that avoids the impact of voltage probes on the current flow in the channel region, e.g. Hall bar or van der Pauw (square, circle, cloverleaf, etc) structures [78]. This requirement is especially critical for few-layer 2D devices, where the presence of voltage probes directly on the channel (as in the case of TLM) can severely affect the current flow in the underlying channel. Similarly, in 4PP measurements with a non-Hall bar patterned channel, the intrusion of voltage probes into the channel region affects the local electric field and current flow in the channel region and thus can result in erroneous extraction of R_{CH}, R_{SH}, and R_C [79].

(ii) Another consideration in measuring a 2D FET using differential measurements (such as lock-

in amplifier-based measurements) is understanding the role of the common-mode rejection ratio (CMRR) [80]. In 4PP measurements, the drain voltage is often biased at high drain bias ($V_{DS} > 1$ V) compared to the source, which is often held at ground voltage. In the presence of large R_C, this leaves the middle voltage probes measuring a small differential voltage on top of a large background common voltage of $\frac{V_{DS}}{2}$. Thus, the rejection of this common voltage is crucial for accurate 4PP measurements. This limits the utility of the 4PP measurements in 2D devices biased at low gate voltages. For example, a typical CMRR of 100 dB with $V_{DS} = 1$ V results in ± 5 μV of common mode voltage. This limits the voltage range for the middle probes to, at minimum, ± 100 μV to achieve >95% accuracy.

(iii) A logical yet often ignored consideration in 4PP measurements is the extremely small magnitude of the voltage drops across the voltage probes due to the presence of large $R_C$at the source and drain junctions, especially when the device is in the OFF state. In the OFF state, both source and drain regions are completely depleted and thus the contact resistance is substantially high. Almost all of the source–drain bias is dropped across the source and drain regions, so the voltage probes have to measure extremely small voltages. These voltages are difficult to measure with most standard source measuring units. As a result, contact and channel resistance measurements in the OFF state are often erroneous.

(iv) Since Ohmic contacts are essential for calculating accurate sheet resistance using van der Pauw measurements, a reciprocity check needs to be conducted to ensure proper van der Pauw measurements in the case of 2D Schottky contact devices. The $\frac{R_A}{R_B}$ ratio is often calculated to determine the reliability of van der Pauw measurements [81, 82].

4. Carrier (doping) density

4.1. Doping in 2D materials and devices

Electrical conductivity is further related to extracting charge carrier density using the relation $\sigma = 1/qn\mu$, where q is the elementary charge, μ is the carrier mobility, and n is the carrier density. Carrier density in a semiconductor can be tuned with substitutional doping; however, substitutional doping is very difficult in 2D materials due to their nanometer-scale thickness. Despite this limitation, there have been a few reports on substitutional doping in 2D materials. For example, group-V elements such as niobium and group-VII elements such as rhenium can be substitutionally incorporated during growth into the crystal lattice of group-VI TMDCs, yielding p-type and n-type semiconductors, respectively [83, 84]. However, the doping density is significantly limited by the solid solubility, thickness, and binding energy of the 2D materials [85]. For example, although a high substitutional Nb dopant concentration up to 10^{14} cm^{-2} (10% Nb concentration) has been achieved in monolayer CVD grown WS_2, the estimated active dopant density according to the electrical properties was only ~6×10^{12} cm^{-2} (approximately 0.06 charges induced per dopant), as evidenced by non-degenerate behavior of transfer curves [86]. Furthermore, charge transfer doping of 2D materials, which is based on their interaction with adlayers, atoms, or molecules, has also been widely studied as an alternative [31–33, 41, 44, 87–96].

Generally, in conventional semiconductors, the doping concentration at room temperature is assumed to be the same as the free carrier concentration, because free carriers such as electrons or holes are generated from fully ionized dopant atoms, which are embedded in the semiconductors by an ion implantation process followed by an activation process using high-temperature annealing. Therefore, doping concentration in bulk semiconductors can be estimated by various methods, e.g. secondary ion mass spectroscopy, X-ray photoelectron spectroscopy, and $I-V$ ($C-V$) characterization. By contrast, doping density in 2D materials is either induced by electrostatic gating or charge transfer, which directly modulates the free carrier density in the material and therefore is primarily determined by electrical characterization.

4.2. Doping density from current–voltage characterization

The carrier density of a semiconductor can be modulated by electrostatic gating in a FET configuration. In this configuration, the two metal electrodes (source and drain, S/D) are used to monitor its conductivity, while the third electrode (gate, G) induces free carriers in the channel material across a gate dielectric material. Here, the carrier density above V_{TH} can be estimated by

$$n = C_{ox}\frac{V_{GS} - V_{TH}}{q}, \tag{10}$$

where C_{ox} is the oxide gate capacitance per area (for example, 11.5 nF cm^{-2} with 300 nm SiO_2 [84]). Note that equation (10) assumes that the device is channel-dominated for $V_{GS} > V_{TH}$; however, it is not operated in a quantum-capacitance dominated regime. For a channel-dominated WSe_2 device with low R_C, good linearity in the transfer curve for a WSe_2 FET is observed for $V_{GS} > V_{TH}$ and thus the carrier density extracted from the equation at high V_{GS} (1.6–4.3 $\times$ 10^{12} cm^{-2}) is in good agreement with that measured using the Hall effect (1–6 $\times$ 10^{12} cm^{-2}) [36]. For 2D materials, the doping density is nearly equal to the free carrier density, since it is mainly induced by the application of

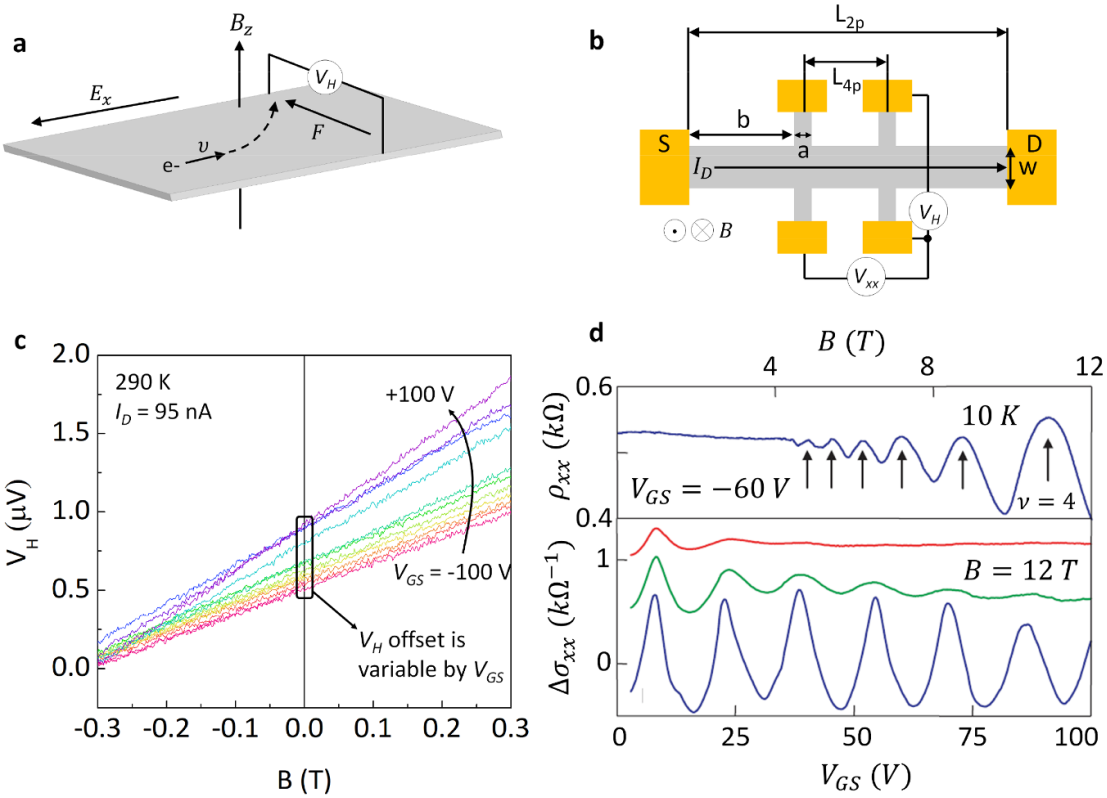

Figure 4. Hall effect measurements of a bridge-type Hall bar structure. (a) Illustration of the Hall effect of an electron. (b) Circuit configuration of a typical bridge-type Hall bar structure device. (c) V_H versus B-field of a graphene device dependent on V_{GS}. (d) SdH effect in graphene showing oscillatory behavior of ρ_{xx} and σ_{xx} in the presence of B-fields [3].

gate biases without external doping. When the doping is generated by external processing instead of gate biasing, the induced doping density can be determined by the shift in charge-neutral points (CNPs) or threshold voltages in the transfer curve according to $\Delta n = C_{ox}(\Delta V_{CNP\,or\,TH})/q$ [97, 98].

4.3. Hall effect measurements

Hall effect measurements are widely carried out to extract the intrinsic material properties of a semiconductor such as carrier density, type, and mobility. Figure 4(a) illustrates how an electron moves in a conductive channel under applied longitudinal electric and perpendicular magnetic fields. The underlying principle of the Hall effect is based on the Lorentz force [99]. An electron flows (in the opposite direction to the current) along the channel in the presence of an electric field E_x with drift velocity υ. When a perpendicular magnetic field B_z is applied, the electron experiences Lorentz force, resulting in a voltage difference (Hall voltage, V_H) transverse to the flow of the electron. The sign of V_H depends on carrier type (electron or hole), and the value of V_H varies depending on the carrier density, current, and magnetic field.

Two typical device structures are used for Hall effect measurements: (1) van der Pauw structure (see figures 3(g)–(i)), and (2) Hall bar structure. Figure 4(b) shows a typical bridge-type Hall bar structure device, which is widely used for Hall measurement of 2D materials. ASTM International provided a guideline for the device geometry of a six-contact device: $L \geq 5\ W$, $W \geq 3\ a$, $b \geq 2\ W$ [100]. It requires that $1.0 \leq L_{2p} \leq 1.5$ cm, although it is very difficult to achieve a centimeter-sized device with good uniformity when working with 2D materials.

Hall effect measurements are usually conducted with a sinusoidal AC or DC drain current, I_D, flowing through the channel of the device (figure 4(b)), and V_H is measured while B-field is swept at a fixed V_{GS}, as shown in figure 4(c). It should be noted that the use of AC measurement with lock-in amplifiers often has a significant advantage over the DC measurement, since V_H is usually in the range of 1–10 μV with a current of 100 nA and a B-field of 1 T, which cannot be observed with conventional DC source measuring units. To make the DC measurements possible, a higher current is required at the same B-field, which in turn results in many unfavorable effects due to threshold voltage shift, Joule heating-induced breakdown, and phase transition [101–103]. Furthermore, the sheet carrier density is calculated from the following equation:

$$n_{2D} = \frac{I_D}{q}\frac{\Delta B_z}{\Delta V_H}. \tag{11}$$

This is a simplified equation by taking the Hall scattering factor (r, generally between 1 and 2) as unity; it should be multiplied by r to the equation

depending on the type of scattering (see section 5.2) [30]. It should be noted that n_{2D} can also be determined from the van der Pauw structure by measuring differential voltages along diagonal direction (e.g. V_{14} and V_{23} in figures 3(h) and (i)) under the presence of a magnetic field. Without the Hall scattering factor, the extracted n_{2D} for undoped 2D semiconductors typically ranges from 0.5–6 $\times$ 10^{12} cm^{-2} with back gate voltages applied across 300 nm SiO_2 at room temperature [36, 104]. The advantage of this method is that any geometric non-uniformity in the devices can be eliminated by extracting the inverse of the slope of a linear curve. As shown in figure 4(c), non-zero V_H at zero B-field due to the non-symmetric geometry, carrier inhomogeneity, and contact resistance can be observed in typical measurements, which can vary depending on the applied V_{GS}. The R_{SH} and Hall mobility (μ_H) values extracted from the Hall effect measurements are described in section 5.1 below.

Apart from Hall effect measurements, the carrier density in 2D materials can also be determined by observing the Shubnikov-de Hass (SdH) effect where the oscillatory behavior of ρ_{xx} is observed in the presence of magnetic fields, as shown in figure 4(d). For 2D devices with moderate electron/hole mobilities, SdH oscillations are usually observed at ultra-low temperatures (a few kelvins) and in the presence of a large magnetic field [2, 3]. Over the years, techniques such as van der Waals-based assembly [105], full device encapsulation, and clean contact fabrication have enabled the observation of SdH oscillations at moderate magnetic fields (<5 T) from graphene [106, 107] and other 2D semiconductor-based devices [108, 109]. In this regard, the SdH effect has become an important measurement tool to determine important material parameters: (i) Quantum mobility (μ_q) from the relation, $\mu_q \approx \frac{1}{B_q}$ where B_q is the magnetic field referring to the onset of SdH oscillation [57]; and (ii) carrier (electron) density from the slope of 1/B versus index of SdH minima by the relation $n = \frac{2q}{h\Delta\left(\frac{1}{B_m}\right)}$, where B_m is the magnetic field at minimum ρ_{xx} and h is Planck's constant. Thus, the Hall effect measurement along with SdH oscillation is a very powerful and effective technique to characterize carrier density in 2D materials.

5. Mobility

Two forms of mobility are typically extracted in 2D devices—Hall effect mobility and MOSFET mobility. Both extraction techniques have their pros and cons. μ_H extraction has an advantage in that it independently measures both resistivity and carrier concentration. Its key disadvantage is that it requires a specialized Hall bar structure (or other suitable geometries with small contacts at the edges of the structure) and the Hall scattering factor (r), is often unknown and simply assumed to be one. MOSFET mobility, on the other hand, comes in many flavors—effective mobility, field-effect mobility, and saturation mobility—depending on how it is extracted. Its main advantage is that MOSFET mobility is extracted in a region of operation that more closely resembles true device operation; however, much care must be taken to ensure that the model used for mobility extraction correctly models the device current and the carrier density of the channel.

5.1. Hall effect mobility

The standard procedure to measure the μ_H is to pattern the semiconductor into a Hall bar structure with contacts placed on the fingers, as shown in figure 4(b). In the typical approach for measuring the μ_H in 2D devices, a constant current is flowed between the source and drain contacts, while a magnetic field is applied normal to the plane of the semiconductor. Hall effect mobility measurements benefit from the independent extraction of the carrier concentration in the channel. In quasi-equilibrium, zero current flows along the width of the device. Therefore, the total force along the width must be zero, satisfied when the Lorentz force is zero, which gives $E_y = v_x B_z$, where x is along the length, y is along the width, and z is perpendicular to the 2D semiconductor channel. The general expression for current flow is given by $I_D = qWv_x n_{2D}$. By defining the Hall voltage as $V_H \equiv E_y W$, we find that $V_H = \frac{I_D B_z}{q n_{2D}}$, (see equation (11) for n_{2D}). From the measurement of V_{xx} shown in figure 4(b), the R_{SH} of the channel can be determined by

$$R_{SH} = \frac{V_{xx}}{I_D}\frac{W}{L_{4p}}. \tag{12}$$

Using $R_{SH} = \frac{1}{q\mu_n n_{2D}}$, we find the Hall effect mobility to be

$$\mu_H = \frac{V_H}{V_{xx}}\frac{L_{4p}}{W}\frac{1}{B_z}, \tag{13}$$

where the value of n_{2D} is given by equation (11) and $\mu_n = \mu_H$ is assumed (which is only valid for a Hall scattering factor of 1). This assumption is further discussed in the following section. As discussed in the previous section, the quantum mobility can also be obtained from the onset of SdH oscillations by Hall effect measurements (e.g. the onset of SdH oscillation occurs at $B = 1$ T, $\mu_q = 10\,000$ cm^2 $V{\cdot}s^{-1}$) [57].

5.2. Challenges of Hall effect measurement

In principle, the measurement of μ_H is straightforward, but in practice, several difficulties arise, complicating the measurement on 2D materials. The first challenge is that the Hall effect measurement requires a specialized structure, ideally following the guidelines of ASTM Standard F76 [100]. The structure should be designed such that the contacts lie as close to the edge of the sample as possible. The flakes

can be etched into the desired geometry, but doing so has a negative consequence that the lithography and etch process may adversely decrease the mobility from its value in a pristine state. This is especially concerning for the mobility measurement of ultra-thin samples, where surface contamination can greatly affect the material's mobility.

Another practical challenge for measuring Hall mobility in 2D materials is that V_H can be quite small, making measurement difficult. V_H is proportional to current per unit width, which is often less than 1 $\mu A\ \mu m^{-1}$ for ultra-thin samples. V_H can have an offset (i.e. $V_H \neq 0$ for $\vec{B} = 0$ as shown in figure 4(c)) due to asymmetry in a Hall bar geometry so the difference in Hall voltage at different B-fields must be used instead of a single B-field measurement. A specialized probe station is typically required to obtain a large B-field, often involving the use of a cryostat with a cryogenic superconducting magnet. The AC Hall effect measurements, where a coil is used to generate the AC magnetic field, which is advantageous over DC measurement as it enables fast and low field measurements <0.1 T, can also be used [110].

Although it is not often done for 2D materials, the sample (mostly graphene) can also be measured while placed atop a permanent magnet that is flipped between measurements to give a positive and negative B-field [111, 112]. Unfortunately, many back-gated devices that are pervasive across the 2D-materials community show significant hysteresis [52, 113] (or even worse, device degradation) from measurement to measurement, which makes the differential extraction between the positive and negative B-field measurements prone to hysteretic error. A solution to overcoming this problem is to perform repeated measurements, switching back and forth between $+B_z$ and $-B_z$, to verify that the data is stable.

Another, often overlooked, error in the measurement of μ_H arises from the assumption of energy-independent scattering in the semiconductor, which is generally only valid at very high magnetic fields ($\gg$1 T) or for neutral impurity scattering. Energy-dependent scattering is captured in the Hall scattering factor, $r = \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2}$ $(1 < r < 2)$, where τ is the mean time between carrier collisions and $\langle \tau \rangle$ is the average over energy. The Hall scattering factor can be determined at a specific B-field by $r = \frac{R_H(B_z)}{R_H(B_z = \infty)}$. Including this factor, the carrier concentration becomes

$$n_{2D} = r\frac{I_D B_z}{q V_H}, \tag{14}$$

and the conductivity mobility equals

$$\mu_n = \frac{\mu_H}{r}. \tag{15}$$

Therefore, the μ_H can over-predict the conductivity mobility by up to a factor of 2. All in all, Hall effect measurement is a powerful technique to measure carrier mobility in 2D materials; however, the technique is not without challenges and complications.

5.3. MOSFET mobility

In contrast to μ_H, MOSFET mobilities can be extracted from the measured transistor characteristics. MOSFET mobilities come in two flavors: effective mobility and field-effect mobility. Figure 5 illustrates the MoS_2 MOSFET characteristics employed to extract the effective and field-effect mobilities [114].

5.3.1. Effective and field-effect mobilities

Effective mobility is extracted from the drain conductance of a MOSFET biased in the linear regime. A general expression for the drain current of a MOSFET with a negligible diffusive current at small V_{DS} can be written as

$$I_D \approx \frac{W}{L}\mu_{eff} Q_n V_{DS}, \text{ for } V_{GS} > V_{TH} \text{ and } V_{DS} \ll (V_{GS} - V_{TH}), \tag{16}$$

where $Q_n = C_{ox}(V_{GS} - V_{TH})$ is the sheet charge density of the channel, μ_{eff} is the effective mobility, and kT is the thermal energy. Ideally, Q_n is determined through independent capacitance or Hall effect measurements of the MOSFET structure; however, given the small size of many exfoliated samples, the capacitance of 2D MOSFETs is not typically measured as the signal is much too small and complex to reliably detect using conventional techniques. For an ideal device, effective mobility is then given by

$$\mu_{eff} = \frac{g_d}{Q_n}\frac{L}{W}, \tag{17}$$

where g_d is the drain conductance given by $g_d \equiv \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{constant\ V_{GS}}$, as shown in figure 5(a). If the output characteristics do not exhibit a linear dependence on V_{DS} around the bias point for which the mobility is extracted, the extracted mobility is suspect since the device characteristics do not follow equation (16) from which μ_{eff} is derived. Similarly, if the transfer characteristics do not exhibit a linear dependence on V_{GS} around the bias point for which the mobility is extracted, the use of the equation to determine Q_n is highly suspect since the device behavior does not fit the charge model.

Field-effect mobility is derived from the transconductance $g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{constant\ V_{DS}}$ of a MOSFET biased in the linear regime as shown in figure 5(b), which is given by

$$\mu_{FE} = \frac{g_m}{C_{ox} V_{DS}}\frac{L}{W}. \tag{18}$$

For conventional MOSFETs, extracted μ_{FE} is often less than the μ_{eff} due to effective-field dependence of

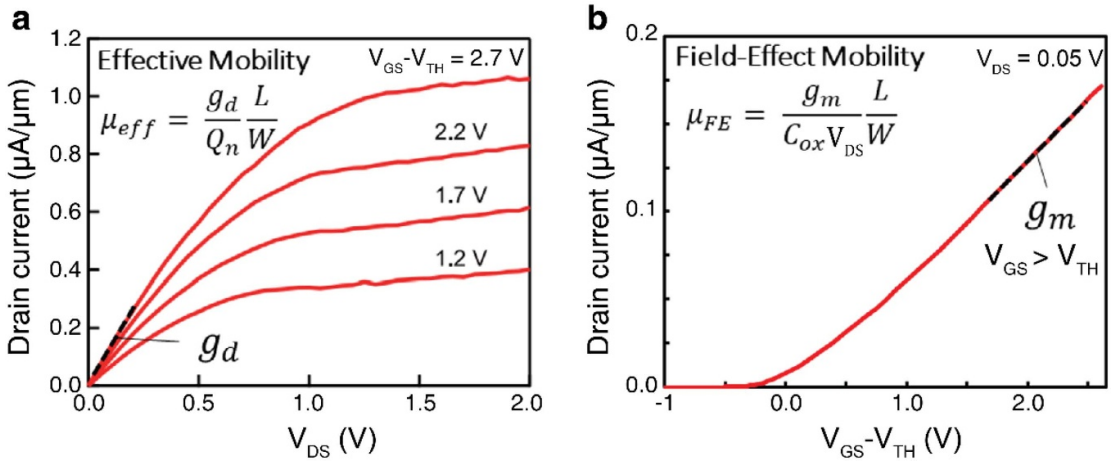

Figure 5. Effective mobility and field-effect mobility. (a) Effective mobility is extracted from the drain conductance near the origin of the output characteristics. For both mobility extraction techniques, both the transfer and output characteristics should show linear behavior around the extraction bias point. (b) Field-effect mobility extracted from the transconductance of a MOSFET, biased in the linear regime [114].

the mobility. When considering this dependence, the transconductance becomes

$$g_m = \frac{W}{L} C_{ox} V_{DS} \left(\mu_{eff} + (V_{GS} - V_{TH}) \frac{\partial \mu_{eff}}{\partial V_{GS}} \right). \quad (19)$$

Since μ_{eff} decreases with increasing effective field, $\frac{\partial \mu_{eff}}{\partial V_{GS}}$ is negative and the measured transconductance is less than what would ideally be expected. The dependence of the μ_{eff} on V_{GS} is often expressed in terms of the effective vertical field,

$$\mu_{eff} = \frac{\mu_o}{1 + (\alpha \varepsilon_{eff})^{\gamma}}, \quad (20)$$

where μ_o, α, and γ are constants, and ε_{eff} is the effective (vertical) field in the semiconductor channel. However, the change in μ_{eff} with V_{GS} is proportional to the change in ε_{eff} with V_{GS}, which is small for back-gated 2D devices with thick oxides. Furthermore, for ultra-thin few-layer 2D MOSFETs, the majority of the channel charge is already present near the channel surface [37], which further suggests that the gate-dependence of μ_{eff} will be less than that of conventional devices.

5.3.2. Errors due to contact resistance

Large contact resistance is a common problem in 2D devices that limits the accurate extraction of MOSFET mobilities. In conventional MOSFETs, R_C is often determined from TLM structures, and the extracted mobilities can be corrected for degradation due to R_C. In principle, the same TLM can be applied to 2D MOSFETs; however, often large device-to-device variations make it difficult to achieve reliable and trustworthy results when applied to 2D materials. Moreover, the mobility extraction from the contact-limited devices can be problematic since V_{TH} is not the onset voltage where the channel is depleted which gives inaccurate charge density Q_n. One way to circumvent the problem of R_C is to fabricate four-probe structures similar to those used for Hall effect measurements as shown in figure 4(b). In such a structure, the voltage drop between the middle contacts is measured (V_{xx}), while V_{DS} is applied between the source and drain contacts. This four-probe drain conductance is defined as $g_d^* = \left.\frac{\partial I_D}{\partial V_{xx}}\right|_{constant\ V_{GS}}$. The measured potential is changed by varying the applied V_{DS}. In this way, the effect of the contacts is removed from the extraction procedure.

The measured potential across the channel may be quite small and perturbation of potential distribution due to the device geometry (e.g. size of voltage sensing probes [115]) may affect the ability to accurately determine the modified drain conductance. The dual-gate structure makes it more complicated due to the contact turn-on effect tending to overestimate mobility unless thorough characterization to minimize measurement artifacts and systematic simulation are considered [116]. Nevertheless, due to the often large and variable R_C in 2D MOSFETs, four-probe measurement presents the best technique to accurately determine channel mobility for both Hall effect and MOSFET mobility measurements.

6. Contact resistance (R_C) and Schottky barriers

6.1. Contact resistance in 2D devices

Lack of simple, efficient, and controllable doping techniques for 2D materials results in large R_C at the metal-semiconductor junction. R_C depends on the nature of the barrier, i.e., its width and height, since barrier sensitively affects carrier transport across it. For the conventional semiconductors, e.g. Si and GaAs, R_C is known to approach near the quantum mechanical limit [117]. Also, there was an early-stage experimental report on R_C in graphene devices by varying contact lengths, in which R_C much larger

than quantum limit was consistently obtained from various device configurations including 2PP and 4PP measurements [118]. However, 2D semiconducting materials with a sizable bandgap in the range of 0.5 ~ 2 eV, e.g., TMDCs, show very high R_C >10 times that of the conventional semiconductor materials [117, 119]. The large R_C at the metal-semiconductor interface is attributable to the formation of Schottky barriers due to mid-gap Fermi level pinning arising from intrinsic material defects and processing conditions [36, 120]. These Schottky barriers not only limit the ON current of the 2D FETs, but also determine their polarity [121, 122]. Moreover, weak Van der Waals bonding between high work function metals such as gold (Au) and palladium (Pd) and 2D materials results in additional tunnel resistance and therefore higher R_C. In addition, typical back-gated 2D devices allow simultaneous gating of contact and channel regions, which convolutes the underlying physics. Since R_C in 2D devices is often much larger than R_{CH}, the output and transfer characteristics of such FET devices represent contact properties rather than channel properties, as discussed in the conductivity section [61, 123–127]. This limits the performance of scaled 2D FETs and affects extraction of important device parameters such as field-effect mobility and V_{TH}, as discussed in the previous sections. Thus, accurate estimation of R_C is critical for understanding, improving, and benchmarking 2D devices.

In this section, we discuss the widely employed TLM technique used to estimate contact resistance in 2D FETs. We discuss the advantages and disadvantages of the method and highlight important considerations that should be taken into account when applying it to 2D materials. We also discuss the temperature-dependent Arrhenius method for extracting SBHs in 2D devices.

6.2. Transmission line method

The TLM/transfer length method is conventionally used to determine R_C for metal contacts on bulk semiconductors, such as Si and Ge [78, 128]. In this method, multiple devices are fabricated with TLM geometry (shown in figure 6(a)), where the channel length/spacing (denoted by L1, L2, etc) is varied between different contacts, while the contact length is kept constant. As shown in the inset of figure 6(a), R_{Total} between any two contacts can be expressed as a linear combination of R_C and the length-dependent R_{CH} of the semiconductor in between the contacts, i.e.

$$R_{Total} = R_{CH}(L) + 2R_C \tag{21}$$

which, using equation (5), can be further rewritten as

$$R_{Total}W = R_{SH}L + 2R_CW. \tag{22}$$

Equation (22) is the fundamental relationship that is used to extract R_C in TLM. Note that the term R_CW is sometimes used to refer to R_C in literature, where it represents width-normalized R_C. Several 2-probe resistance measurements are made between an adjacent pair of contacts with different channel lengths and R_{Total} is plotted as a function of channel length. Figure 6(b) shows a typical plot of R_{Total} versus L from which R_C can be extracted by finding the y-intercept using a linear fit. Other relevant parameters are also highlighted in the plot. Furthermore, low source–drain voltages (< 1 V) are recommended for accurate TLM to avoid Joule heating [103] and impact ionization [129] in channel 2D materials.

Figure 6(c) shows a schematic of a typical TLM structure with a 2D material as the channel material and conventional back-gated geometry. Unlike bulk semiconductors, 2D materials generally do not conduct well without gating due to large R_C. Thus, equation (22) needs to be modified to show the effect of global back gating, in which case both the channel and contact regions are modified simultaneously, i.e.

$$R_{Total}(V_{GS})\,W = R_{SH}(V_{GS})\,L + 2R_C(V_{GS})\,W \tag{23}$$

Figure 6(d) illustrates the use of TLM to extract contact resistance for Au contacts on a bilayer MoS_2 where the channel length was varied from 200 to 1000 nm [130]. The measured total resistance ($R_{Total}W$) was plotted as a function of channel length; the corresponding y-intercept provides the contact resistance (R_CW). As discussed earlier, the contact resistance shows clear gate voltage dependence (highlighted by carrier density in the channel using equation (10)), as contact resistance decreases with an increase in gate voltage.

6.2.1. Transfer length and contact resistivity extraction

TLM also provides a simple way to study the scaling properties of contacts, which is crucial to determine the fundamental limits to scaling of 2D materials-based FETs. As the channel length is scaled to enable better electrostatics and achieve higher device density, a large portion of total resistance corresponds to the contact resistance resulting in contact-dominated behavior of scaled devices. Using a distributed resistive network model for the contact region (figure 7(a)), analytical expressions for contact resistance can be obtained in terms of specific contact resistivity (ρ_c), sheet resistance under contact (R_{SK}), and transfer length (L_T):

$$R_CW = \sqrt{\rho_c R_{SK}}\coth\left(\frac{L_C}{L_T}\right); \tag{24}$$

$$L_T = \sqrt{\rho_c/R_{SK}}. \tag{25}$$

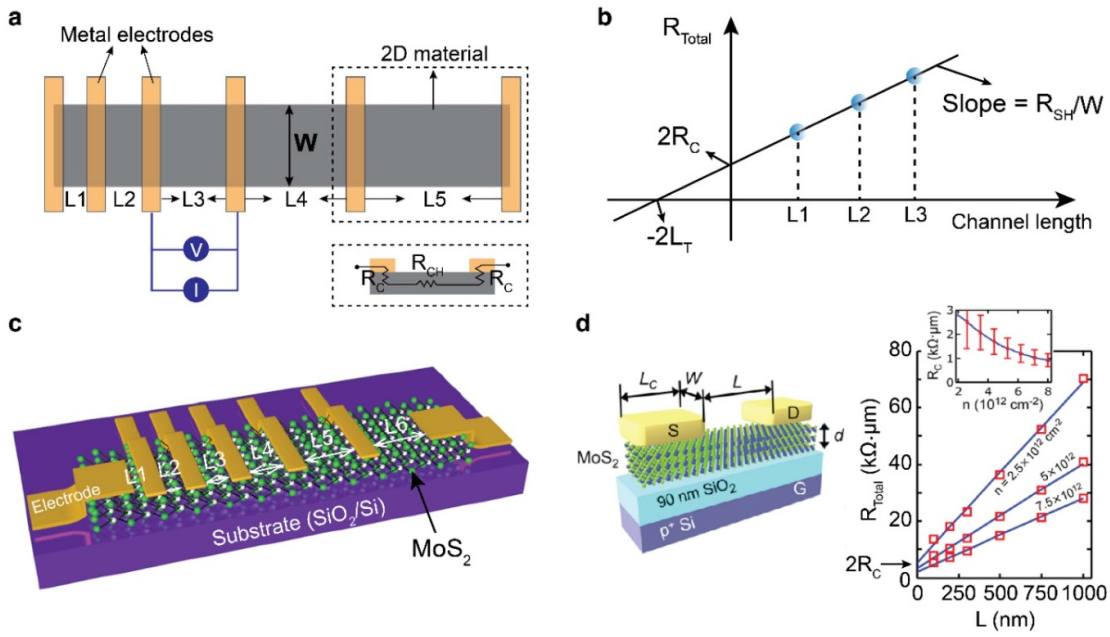

Figure 6. (a) Top view of the TLM configuration showing different channel lengths (L_1, L_2, ...). The enlarged view shows the distribution of total resistance in terms of R_C and R_{CH}. (b) A linear fit of the plot of R_{Total} versus channel length giving rise to R_C, R_{SH}, and L_T. (c) Schematic of a MoS_2-based TLM device with back gating through SiO_2. (d) Schematic of a bilayer MoS_2 device and the TLM plot for the device showing the linear trend of R_{Total} versus channel length as a function of carrier density (gate voltage). The inset shows the extracted R_C values as a function of carrier density, demonstrating contact region gating [130].

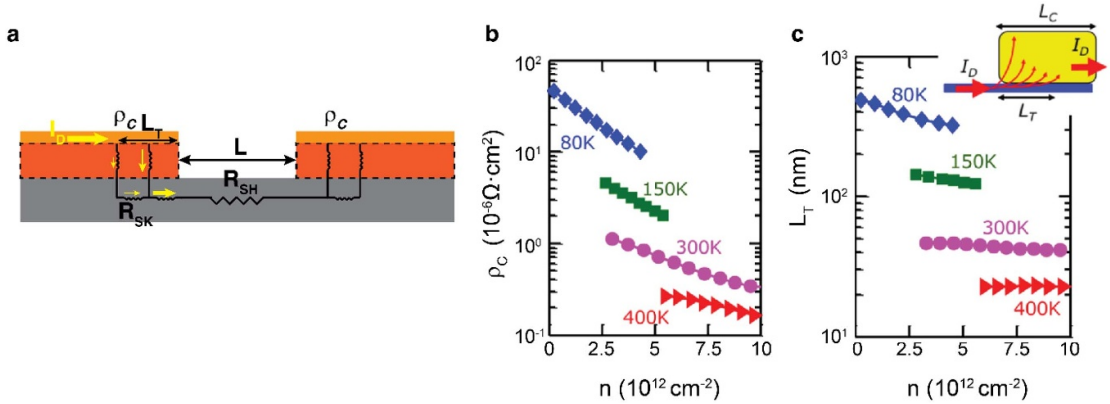

Figure 7. Extraction of R_C and L_T. (a) Side view showing the resistive network used to calculate L_T. (b, c) Extracted ρ_c and L_T in a bilayer MoS_2 as a function of carrier density (gate voltage) at different temperatures [130].

Here, L_C is the physical contact length and L_T represents the current crowding at the metal-semiconductor junction and is defined as the effective length over which a majority of charge transfer/current transport occurs beginning at the edge of the junction ($x = 0$). Further insight can be gained by considering two limiting cases:

$$(i)\ L_C \gg L_T : R_C W = \sqrt{\rho_c R_{SK}} = L_T R_{SK} \qquad (26)$$

$$(ii)\ L_C \ll L_T : R_C W = \frac{\rho_c}{L_C} \qquad (27)$$

Experimentally, these parameters are extracted from TLM by assuming that $R_{SK} = R_{SH}$ and $L_C \gg L_T$ which allows us to extract L_T by finding the x–intercept of the curve of R_{Total} versus L. Once L_T is determined, ρ_c can be determined by either equations (26) or (27). Figures 7(b) and (c) show the extracted ρ_c and L_T values, respectively, for the device presented in figure 6(d).

6.3. Challenges with TLM

Over time, the TLM has become the most commonly employed method of determining R_C and R_{SH} in 2D materials-based devices due to the ease of device fab-

rication and straightforward nature of the analysis. Moreover, the method is generally material agnostic; it does not require any prior knowledge of effective mass, dielectric constant, bandgap, etc.. Furthermore, the TLM has an advantage over 4PP as current transport is not disrupted by the presence of inner electrodes, which are used as voltage probes in typical 4-probe measurements, as discussed in the previous sections [115, 131, 132]. However, a few potential pitfalls must be considered when applying TLM to 2D FET analysis:

(i) Reliable TLM requires linear dependence of channel resistance on channel length and low spatial variation of contact resistance. Fabrication issues such as irregular device geometry due to non-patterned 2D flakes, inhomogeneous non-laminar current flow due to polymer contamination, lithography-induced damage, and unknown contributions from sample edges, can cause deviation from linear scaling of channel resistance and therefore result in erroneous contact resistance measurements [120].

(ii) TLM is also problematic when contact resistance is substantially higher than channel resistance, since a small amount of inter-device variation in contact resistance can cause large errors in the linear fit. Moreover, for Schottky contacts with non-linear I–V characteristics, R_C becomes bias-dependent, which needs to be carefully considered when examining scaling behavior. The impact of non-linearity in the plot of R_{Total} versus L is severe when the extracted transfer lengths are small. TLM is most successful at high back gate voltages, where the channel resistance is substantially larger than the contact resistance and it is clear that total resistance scales linearly with channel length [130].

(iii) Extracting transfer length and specific contact resistivity requires that $R_{SK} = R_{SH}$ holds true, which is hard to justify for few-layer devices. Unlike conventional semiconductors, in which lateral transport occurs far (~10–100 nm) from the metal-semiconductor interface, transport in 2D materials occurs right at the interface and the material properties are substantially changed by the metal contacts (e.g. contact doping, fabrication-induced damage, and change in bandgap). Recent studies have shown significant differences in R_{SK} and R_{SH}, which calls for use of complementary methods for accurate extraction of L_T, ρ_C and R_{SK} such as contact-end and cross-Kelvin bridge methods [133]. Future work on modeling and analysis of metal contacts on 2D materials needs to take this into consideration, helping to come up with accurate methods of extracting L_T, ρ_C and R_{SK}.

6.4. Schottky barrier heights and Fermi level pinning

As discussed above, the large contact resistance in 2D devices can be attributed to the presence of Schottky junctions at the metal-2D semiconductor interfaces. Schottky junctions are characterized by SBHs, the relative values of which determine the current transport at the metal-semiconductor interface affecting the polarity, magnitude, and switching characteristics of the injected charge carriers. Figure 8(a) shows the SBH and conceptual band diagram of a metal-2D semiconductor interface. For an ideal metal-2D semiconductor junction, the SBH for n-type (ϕ_{Bn}) or p-type (ϕ_{Bp}) semiconductors is given by:

$$\text{For } n \text{ - type: } \phi_{Bn} = \phi_m - \chi, \tag{28}$$

$$\text{For } p \text{ - type: } \phi_{Bp} = \chi + E_g - \phi_m, \tag{29}$$

where ϕ_m is the work function of a metal, χ is the electron affinity and E_g is the 2D semiconductor bandgap. For such ideal systems, the SBH for electrons increases linearly with the metal work function, thus satisfying the Schottky–Mott rule as shown in figure 8(b). However, non-ideal states such as interface and gap states at the metal-semiconductor interface can cause severe deviation from the Schottky–Mott rule, making it difficult to control electron/hole SBH by varying the metal work function. Quantitatively, we can interpret this deviation by introducing a pinning factor (S) and charge neutrality level (CNL, ϕ_{CNL}) [134, 135]:

$$\begin{aligned} n-\text{type: } \phi_{Bn} &= S(\phi_m - \phi_{CNL}) + (\phi_{CNL} - \chi) \\ &= S\phi_m + b, \end{aligned} \tag{30}$$

$$p-\text{type: } \phi_{Bp} = S(\phi_{CNL} - \phi_m) + \left(E_g + \chi - \phi_{CNL}\right) \tag{31}$$

Here, S is defined as the slope $S = \frac{\partial \phi_{Bn}}{\partial \phi_m}$ and can be calculated from the linear fit of ϕ_{Bn} versus ϕ_m plot. $S = 1$ represents an ideal metal-semiconductor interface whereas $S = 0$ represents almost no variation in SBH with a change in the metal work function, indicating a completely pinned interface at the charge neutrality level. The CNL for n-type can be estimated by the relation

$$\phi_{CNL} = \frac{\chi + b}{1 - S}. \tag{32}$$

For $S < 1$, the semiconductor Fermi level is fixed near the CNL, which results in similar SBHs for different metal contacts, that is, 'Fermi level pinning', as shown in figure 8(c). Fermi level pinning is often attributed to metal-induced gap states (MIGS) and defect-induced gap states (DIGS); however, the exact physical mechanism still remains an open question.

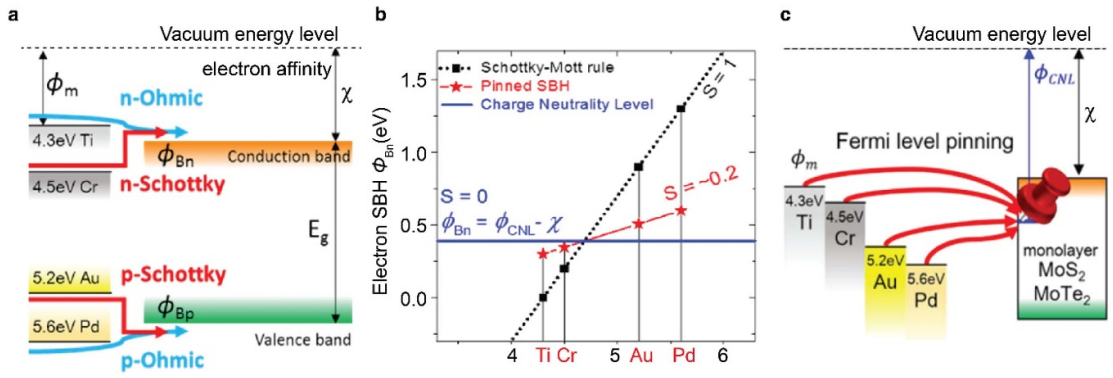

Figure 8. Schottky barrier height and Fermi level pinning. (a) Band diagram of a metal-semiconductor junction. (b) SBH versus metal work function showing the Schottky–Mott rule and Fermi level pinning. (c) Schematic image of Fermi level pinning [35].

6.4.1. SBH extraction in 2D devices

Accurate extraction of SBH for any metal-2D semiconductor junction is essential for understanding the underlying physics of 2D devices and deducing the pinning factor and CNL. Generally, for bulk semiconductors, SBH is determined by fabricating Schottky diodes with different metal contacts; however, the large contact resistance at the metal-2D semiconductor interface makes it almost impossible to construct a proper Schottky diode . For this reason, the standard back-gated FET structure is more commonly used to extract SBH. The most prevalent method of determining SBH is the Arrhenius technique, which depends upon analyzing the temperature-dependent transfer or output characteristics of a back-gated 2D FET [34, 61].

As shown in figure 9(a), current transport at the reverse-biased source junction of a 2D FET consists of two distinct components: (i) TE, where charge injection occurs over the barrier, and (ii, iii) tunneling transport, where the charge injection occurs through the barrier [136, 137]. Tunneling transport can be further divided into thermionic field emission (TFE) and field emission (FE), where TFE denotes tunneling at an energy level higher than the source Fermi level and vice-versa. The relative contribution of these three components can be tuned by changing the applied gate bias. In the OFF state, the conduction band edge is higher than the actual SBH and is completely dominated by TE. In this regime, the current can be expressed as

$$I_{2D}(V_{GS}) = WA^*_{2D}T^{\frac{3}{2}} \exp\left(-\frac{q\phi_{B,eff}(V_{GS})}{k_BT}\right)\left[1-\exp\left(\frac{-qV_{DS}}{k_BT}\right)\right] \quad (33)$$

where $\phi_{B,eff}(V_{GS})$ is the gate voltage-dependent effective barrier height, $A^*_{2D} = \frac{q\sqrt{8\pi m^* k_B^3}}{h^2}$ is the modified Richardson constant, T is temperature and m^* is the effective mass. In TE regime the current is strongly influenced by temperature and gate voltage due to its exponential dependence on these parameters. At a certain gate voltage, termed flat-band voltage (V_{FB}), the conduction band is perfectly aligned with the SBH at the source end, i.e. $\phi_{B,eff} = \phi_{Bn}$. For $V_{GS} > V_{FB}$, the tunneling current starts to dominate the overall current transport resulting in weaker temperature dependence. Thus, the actual barrier height can be extracted by identifying the effective barrier corresponding to the flat band voltage by analyzing the temperature-dependent transfer characteristics as shown in figure 9(b).

To extract the SBH, the temperature-dependent transfer characteristics are modeled with the thermionic current equation and replotted in an Arrhenius manner, shown in figure 9(c). From here, the effective barrier for current flow can be extracted by linearly fitting the Arrhenius curves, and can be expressed as

$$\phi_{B,eff}(V_{GS}) = \frac{k_B}{q}\left[\frac{\Delta \ln\left(I_D(V_{GS})/T^{\frac{3}{2}}\right)}{\Delta T^{-1}}\right]. \quad (34)$$

Finally, as shown in figure 9(d), $\phi_{B,eff}$ is plotted as a function of applied gate bias, and the actual SBH (ϕ_{Bn}) can be determined by identifying the gate voltage at which the curve of $\phi_{B,eff}$ versus V_{GS} deviates from its initial linear slope [34, 61]. This gate voltage corresponds to the flat band voltage and the corresponding $\phi_{B,eff}$ is recognized as ϕ_{Bn}.

6.5. Challenges with the Arrhenius method of SBH extraction

Even though the Arrhenius method is widely used to extract SBH in 2D materials, its applicability is often questioned, because it requires several assumptions that are not generally satisfied in 2D devices. Here, we discuss the assumptions and their impact on the extracted SBH.

(i) Need for a clear transition from the thermionic regime to the tunneling regime: Since the Arrhenius method depends upon proper identification of the flat band voltage, the device

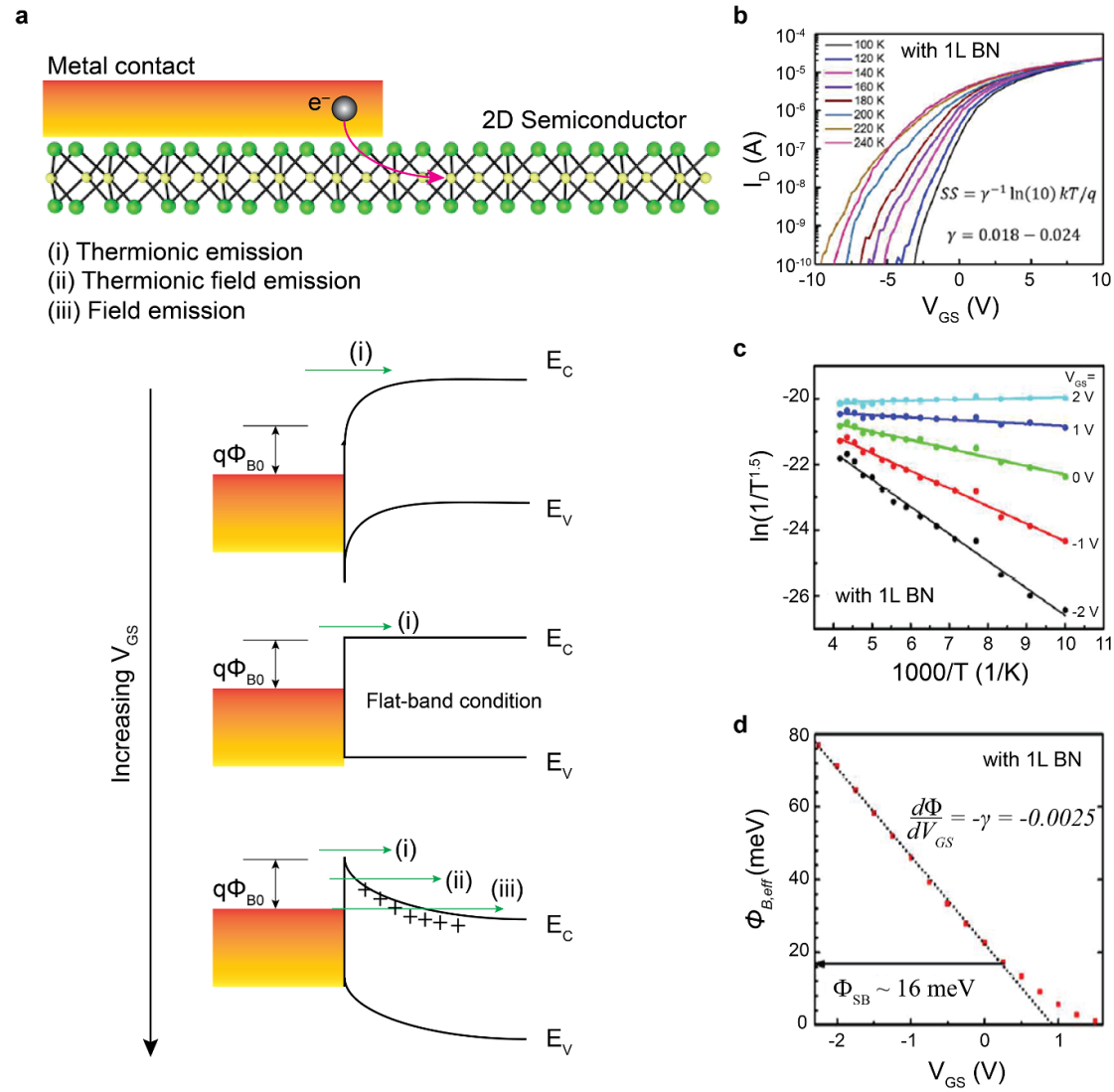

Figure 9. Extraction of SBH from a temperature-dependent transfer curve. (a) Different transport regimes at the source contact as a function of gate voltage. Thermionic emission dominates in the OFF state ($V_{GS} < V_{FB}$), and tunneling current begins to dominate in the ON state. Here, $q\phi_{B0}$ is equivalent to the n-type SBH ($q\phi_{Bn}$) at flat-band condition [61]. (b) Transfer curve of monolayer MoS_2 with a 1 L-hBN/Co contact in the temperature range from 100 K to 240 K. (c) Richardson plot ($ln\ I/T^{1.5}$ versus $1000/T$) of (b). (d) SBH as a function of gate voltage [104].

needs to show a clear transition from a thermionically dominated regime to a tunneling regime. However, this transition is often poorly defined in 2D devices due to the presence of non-idealities such as traps, non-homogenous doping due to surface contaminants, and van der Waals gap [138–140]. Moreover, for doped contacts, devices with thick (>2 nm) tunnel barriers, and few-layer (>5) devices, the assumption of pure thermionic current is difficult to verify due to the high tunneling current arising from the channel region underneath the contact [121, 137, 141–144].

(ii) Weaker thermionic current at lower temperatures: More often than not, the Arrhenius method for SBH extraction in 2D materials involves temperatures below 100 K. At such temperatures, the thermionic component is substantially smaller than the usual leakage floor for any considerable SBH (ϕ_{Bn} > 100 meV). For example, a contact-dominated 2D FET with an SBH of 0.3 eV should result in a maximum thermionic current of 6 nA at flat band condition at 300 K, which is reduced to less than 1 fA for T < 77 K. Thus, it is extremely difficult to measure any thermionic current at low temperatures below 100 K. This means that the currents observed at such temperatures usually come from TFE or FE components that show weak temperature dependence [35, 145] and therefore leading to erroneous SBH extraction.

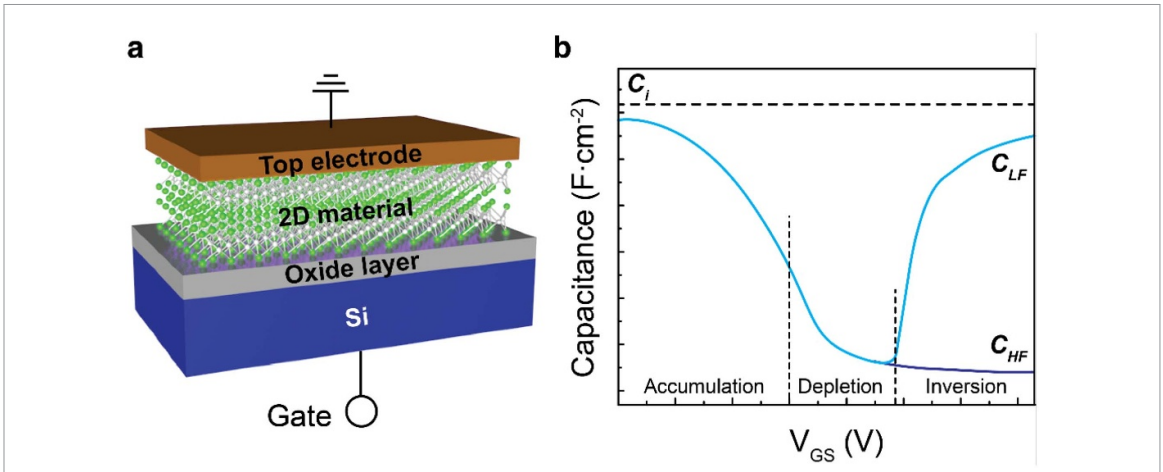

Figure 10. (a) Schematic illustration of a 2D MOS capacitor. (b) Ideal *C–V* characteristics of a MOS capacitor at low and high frequencies indicating different regimes (accumulation, depletion, and inversion).

7. Trapped charges and dielectric constant

7.1. Capacitance–voltage characterization

C–V measurement is a robust electrical characterization method used to assess the properties of defects in insulating and semiconducting materials and to probe the variation in the space charge distribution in a semiconductor with applied gate voltage. It can be used to measure various parameters, such as insulator capacitance (C_i) or oxide capacitance (C_{ox}), flat band voltage, dopant concentration, interface traps, and dielectric border traps, which are typically analyzed from metal-oxide-semiconductor (MOS) or metal-insulator-semiconductor (MIS) structures. The basic structure of a MOS capacitor consists of metal, oxide, and a 2D semiconductor material (*n*- or *p*-type) as shown in figure 10(a). When performing the *C–V* measurements of 2D materials, a large gated area (i.e. channel area) with high signal-to-noise ratio and low parasitic resistances is required to ensure the reliability of the measurements and analysis. From a device perspective, a 2D material-based MOS capacitor has two distinct interfaces: metal/semiconductor interface (top) and semiconductor/oxide interface (bottom). Both interfaces are crucial to examine as they are coupled to each other. The ideal *C–V* curve of different regions of a MOS capacitor is illustrated in figure 10(b). The working condition of a MOS capacitor depends on the applied V_{GS} and can be divided into three different regimes: (i) accumulation, in which majority carriers (electrons) are accumulated near the 2D semiconductor-dielectric interface; (ii) depletion, in which majority carriers become depleted at the interface; and (iii) inversion, in which the density of majority carriers continues to decrease while that of minority carriers increases.

When attempting to fabricate the 2D MOS (or MIS) vertical capacitors, various issues can be encountered. For vertical stacking of 2D materials, a polymer, e.g. polydimethylsiloxane (PDMS) stamp is often used to mechanically exfoliate the 2D crystals and to transfer them to desirable substrate. But the polymer residues from PDMS stamp degrade the properties of transferred 2D materials via the formation of interfacial bubbles and wrinkles, which results in contaminants trapped at the interface between the substrate and the 2D material. To avoid and minimize the formation of residues at the interface during the stacking of such materials, alternative polymers, such as poly(propylene) carbonate, can be used [146]. Afterfabricating clean 2D MOS capacitors, the electrical measurements are conducted using a semiconductor parameter analyzer and an LCR meter. Care should be taken to ensure that the instruments are used with the lowest possible external impedance to minimize the parasitic capacitances. Although 2D materials have attracted a great deal of interest for advanced electronic applications due to their tunable bandgaps and high surface-to-volume ratios [147–149], the device performance is strongly affected by various 2D materials-related processing issues, such as the adsorption of H_2O molecules from the environment, structural defects (vacancies, grain boundaries, dislocations, etc.), and the interface charge traps due to the interactions with dielectric materials (e.g. SiO_2, Al_2O_3, HfO_2), which results in hysteresis in *C–V* (*I–V*) characteristics and degradation of electron and hole mobilities [150–154]. Zhu *et al* studied the interfacial properties of a HfO_2/monolayer MoS_2 using *C–V* measurements and observed a double-hump feature in the *C–V* curve characterized to different gate voltages and frequencies, revealing traps in CVD-grown MoS_2 [155].

When working with 2D materials, due to their inert surfaces and the absence of dangling bonds, it is difficult to form a uniform and high-quality dielectric film, but this goal can be realized with proper surface functionalization [156, 157]. Pretreatment of the 2D material surface (e.g. MoS_2) with oxygen plasma (O_2) or ultraviolet/ozone (UV/O_3) has been considered

to enhance reactivity before high-k deposition to decrease the density of interface traps [158–161]. Previously, the quartz substrates were used for the fabrication of MIS capacitors to eliminate the parasitic capacitances between the metal pads and the substrates [162]; the *C–V* measurements of intermediate (WSe_2, 1.2 eV) and narrow bandgap (black phosphorus, ~0.3 eV) materials showed high-frequency (unipolar) and low-frequency (ambipolar) behavior, respectively.

7.2. Trapped charges in 2D materials

High-quality interfaces are crucial for high-performance 2D devices due to the large surface-to-volume ratio of 2D materials [163–166]. Charges trapped in the interface, either positive or negative, originate from structurally induced defects at the gate-dielectric and dielectric-semiconductor interfaces that are capable of trapping and de-trapping charge carriers. The trapped charges in 2D device structures have been quantitatively analyzed using the capacitance and AC conductance measurements [155, 163, 167]. The density of interface traps can be determined by $D_{it} = \partial N_{it}/\partial E$ (cm^{-2} eV^{-1}), where D_{it} is the interface trap density, N_{it} is the number of interface traps per unit area, and E is the energy. Figure 11(a) illustrates various origins of interface states in a high-k/MoS_2/oxide structure [168].

Researchers have employed different methods for interface analysis and extracted different types of trapped charges, such as interface trapped charges and dielectric border trapped charges (or oxide charges) [158, 161, 168–170]. For example, the band diagrams of the interface and border traps in HfO_2/MoS_2 are shown in figure 11(b). The interface traps in MoS_2 bandgap dominate the *C–V* response in the depletion region, whereas the border traps in HfO_2 dominate in the accumulation region. The interface traps were investigated and the D_{it} was extracted using frequency-dependent *C–V* measurements. The typical mid-gap D_{it} at the SiO_2 gate dielectrics/Si interface is ~10^{10} cm^{-2} eV^{-1}, while the D_{it} of the high-k dielectric/Si interface ranges from 10^{11} to 10^{12} cm^{-2} eV^{-1} [171]. One study examined the density distribution and dynamics of trap states in CVD-grown MoS_2 using capacitance measurements; the traps were shown to colonize the mid-gap (Type M trap) and band edge (Type B trap) regions (figure 11(c)) [155].

The influence of high interface state density D_{it} on high-k/2D device characteristics has inspired extensive research on passivation of the high-k/2D interface to reduce D_{it} [158–161]. D_{it} most likely originates from the oxygen atoms that fill the sulfur vacancies during UV/O_3 functionalization treatment [160]. D_{it} can be calculated with the conventional high-low frequency and multi-frequency methods using the following equations

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}, \quad (35)$$

$$D_{it} = \frac{C_{it}}{q}, \quad (36)$$

where C_{it} is the capacitance of interface traps when all the traps react with AC signal at low frequency, and C_{LF} and C_{HF} are the capacitances measured at low and high frequencies, respectively [158, 172]. Liu *et al* evaluated D_{it} (10^{13} cm^{-2} eV^{-1}) in BP and WSe_2-based MIS capacitors with Al_2O_3 as a dielectric using the parallel conductance (G_p), which is extracted from capacitance and conductance measurements [162], given as

$$G_p = \frac{\omega^2 G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}, \quad (37)$$

where ω is the measurement frequency, C_m is the capacitance of the device, and G_m is the conductance. D_{it} is calculated using [155, 162, 170],

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{peak}. \quad (38)$$

A significant decrease in D_{it} was reported in a 2D hBN capacitor [162]. A low-temperature high-k deposition method led to the formation of traps associated with the dielectric known as border traps or near-interfacial oxide traps [173]. These defects responded to a change in V_{GS} in the gate dielectric at some distance from the interface, and therefore induce hysteresis in *C–V* measurements and are responsible for the frequency dispersion in the accumulation region. There have also been studies that determined the density of border traps, as distinct from interface traps, using multi-frequency *C–V* characteristics of HfO_2/MoS_2 and HfO_2-Al_2O_3/MoS_2 top-gate stacks (figure 11(d)) [159, 160].

7.3. Dielectric constants of 2D materials

The dielectric constant (ε) of a material is a fundamental electrostatic property that can be used to determine the capacitance, charge screening, and energy storage capacity of electronic devices. ε also plays a significant role in defining the active interactions that take place between charged particles in the material and contains information about the collective oscillations of electron gas, plasmons, excitons, and quasiparticle band structures [174, 175]. The unique structure of 2D layered materials leads to anisotropic physical properties between the in-plane and out-of-plane directions, e.g. inhomogeneous dielectric strength and Coulomb interaction strength characterized by ε; this is unlike conventional isotropic materials such as silicon. The theoretical dielectric property of 2D materials such as graphene and MoS_2 is anisotropic owing to the different nature of bonds in the in-pane and out-of-plane directions

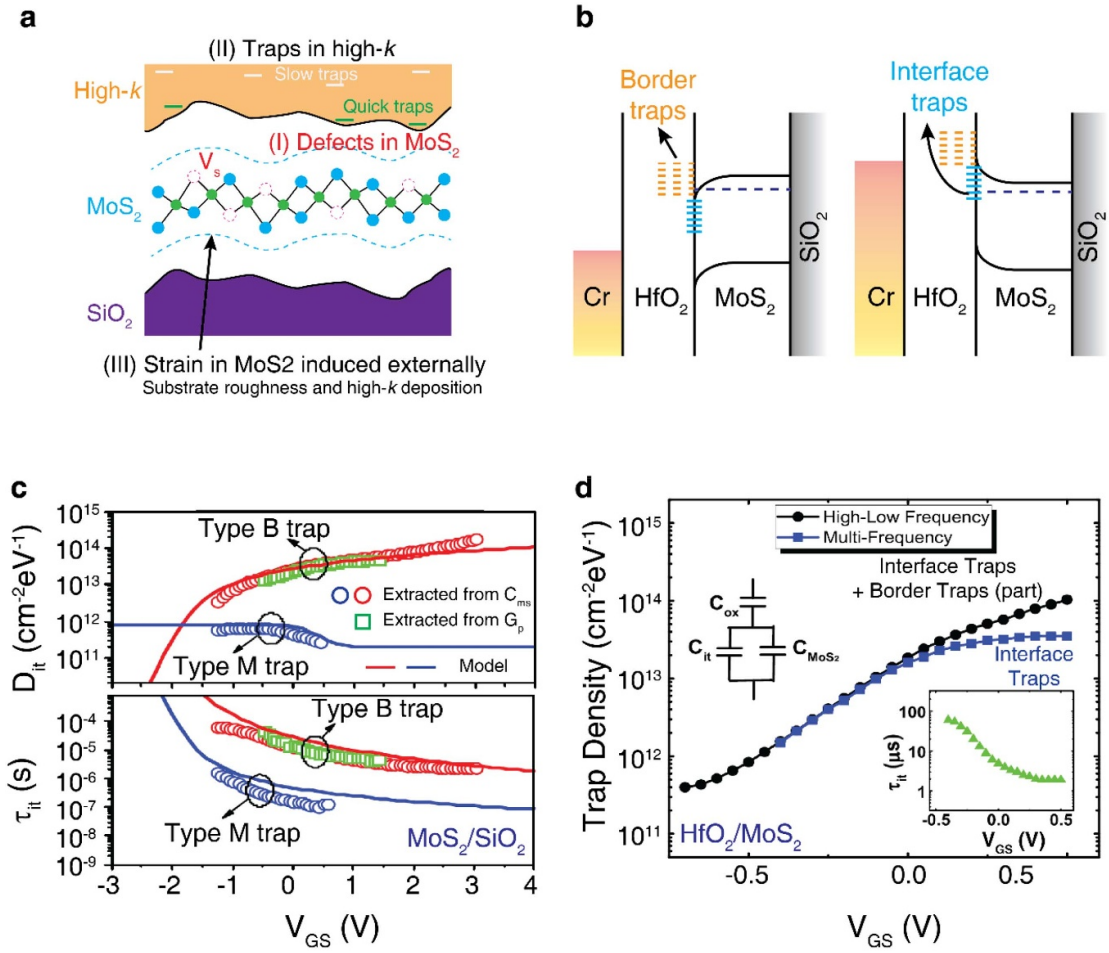

Figure 11. Interface and border trapped charges. (a) Representation of various origins of interface states in a high-k/MoS_2/oxide structure, where V_S is sulfur vacancies. (b) Schematic illustration of the energy band diagrams of interface and border traps distributed in HfO_2/MoS_2. (c) D_{it} and time constant of trap states (τ_{it}) as a function of V_{GS} of CVD-grown MoS_2 on a SiO_2/Si substrate [155]. (d) Comparison of high-low frequency and multi-frequency methods of measuring border trap density (N_{bt}) and D_{it}. The difference in trap density shown between 0 and 0.5 V is caused by the border trap response at lower frequencies. The left and right inset figures show the equivalent circuit including C_{it} and the extracted τ_{it}, respectively [159].

($\varepsilon_{||}$ and $\varepsilon_{\perp}$) [176–178]. Chen *et al* experimentally extracted the ε of MoS_2 from C–V measurements based on vertical MIS capacitor structures by using the following relation:

$$\varepsilon_{MoS_2} = \frac{d_{MoS_2}}{\left(C_{min}^{-1} - C_g^{-1}\right)}, \tag{39}$$

$$C_{min} = \left(\frac{d_{MoS_2}}{\varepsilon_{MoS_2}} + \frac{1}{C_g}\right)^{-1} \tag{40}$$

where C_{min} is the minimum capacitance measured at $V_{GS} < 0$ V, d_{MoS_2} is the thickness of MoS_2, ε_{MoS_2} is the dielectric constant of MoS_2, $C_g \left(= \left(\frac{1}{C_{BN}} + \frac{1}{C_{in}}\right)^{-1}\right)$ is the geometric capacitance, C_{BN} is the geometric capacitance of hBN, and C_{in} is the interlayer capacitance originating from the interlayer spacing between hBN and MoS_2 (figure 12(a)) [179].

The ε as a function of the frequency (dielectric dispersion) of an hBN-based metal-insulator-metal (MIM) capacitor was demonstrated using time-domain reflectometry, where the ε of hBN decreases with an increase in frequency (figures 12(b) and (c)) [180]. The confined nature of atomically thin 2D crystals associated with the anisotropic dielectric screening has created long-term debates whether the dielectric constant truly represents the dielectric features of such low-dimensional systems. The ε values accounted for by both theoretical and experimental approaches vary by more than an order of magnitude [181]. Therefore, future developments that allow reliable and precise measurements of ε are needed.

8. Correlating device parameters to nanoscale material properties

Until this section, we have described the extraction of electrical parameters in the macroscopic transport of 2D devices, mainly focusing on FET structures. The device properties and performance are largely affected by both intrinsic (vacancies, anti-sites, substitutions, and grain boundaries in polycrystalline samples) and extrinsic (strains due to surface roughness

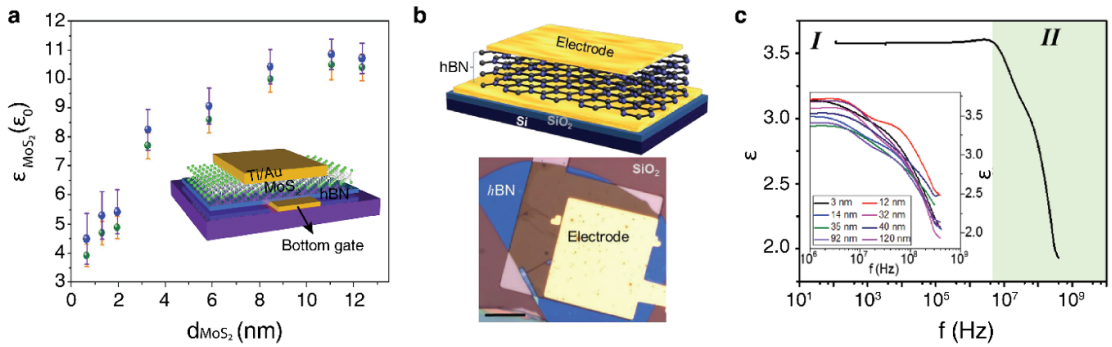

Figure 12. Extraction of the dielectric constants (ε). (a) The ε of MoS_2 (ε_{MoS_2}) with (blue dots) and without (green dots) counting the interlayer capacitance as a function of MoS_2 thickness (d_{MoS_2}) [179]. (b) A schematic illustration (top) and an optical microscope (OM) image (bottom) of a 32 nm-thick hBN-based MIM capacitor (scale bar of in the OM image: 20 μm). (c) The extracted ε of hBN as a function of applied frequency. ε remains stable at low frequencies (region I), whereas ε appears smaller at higher frequencies (region II) since the charges are allowed less time to orient themselves in the direction of the alternating field. The inset shows the dispersion characteristics of hBN flakes with different thicknesses [180].

and ripples, electron-hole puddles caused by charge impurities in a SiO_2 substrate, chemical adsorbates, polymer residues, etc) disorder [105]. For example, the grain boundary in a graphene device can affect the sheet resistance depending on the grain size according to the equation $R_{SH} = R^G_{SH} + \frac{\rho_{GB}}{l_G}$, where R^G_{SH} is the average sheet resistance of the graphene grains, ρ_{GB} is the average grain boundary resistivity, and l_G is the average grain diameter [182]. The charge inhomogeneity induced by the SiO_2 substrate gives rise to carrier density fluctuation of up to ~4.5×10^{11} #/cm^2 at the sub-10 nanometer-scale length, as shown in figure 13(a) [183, 184]. Mechanical and surface morphology (e.g. a crested substrate)-induced strain can engineer the local bandgap and mobility of 2D materials [185, 186]. The influences of the disorder are very difficult to characterize solely by macroscopic transport unless nanoscale characterization techniques are utilized. In this section, we introduce various SPM techniques as supporting methods that enable local characterization of 2D materials correlated with the electrical parameters discussed in the previous sections. Detailed reviews on SPMs of nanomaterials and nanoelectronics are also provided in [187, 188].

Kelvin probe force microscopy (KPFM) is a widely used SPM technique for nanomaterials and nanoelectronics. KPFM measures contact potential differences (V_{CPD}) to provide a quantitative measure of the work function difference between a sample and a probe tip. Figure 13(b) shows a schematic illustration of a KPFM measurement setup for graphene in which AC (V_{AC}) voltage generates oscillating electrical forces and DC (V_{DC}) voltage is applied to nullify the oscillating electric forces when $V_{DC} = V_{CPD}$ [189, 190]. The ΔV_{CPD} (contact potential difference between electrode and sample) is used to obtain the work function of graphene, which is correlated with the Fermi energy (E_F) of graphene, a relative energy level with respect to the charge neutral point (CNP), as shown in figure 13(c). For graphene, the carrier density can be calculated using the following equation, $n = \frac{1}{\pi}\left(\frac{E_F}{\hbar v_F}\right)^2$, where $\hbar$ is the reduced Planck constant, and v_F is the Fermi velocity of graphene [191, 192]. A space charge region in a 2D semiconductor, which can be capacitively coupled with the air gap between the tip and sample, should be carefully considered for the measurements. Scanning capacitance microscopy, which measures local differential capacitance, allows for mapping of the carrier (doping) density and polarity profile, as well as the measurement of trapped charges and quantum capacitance [187, 193, 194].

Scanning tunneling microscopy (STM) has become a core technique for exploring the emergent physics of newly discovered materials. Since the discovery of 2D materials, this technique has been widely employed to locally map the atomic structure and electronic properties of various 2D materials [198–200]. Due to the wide application of STM, it has become an ideal tool to reveal the intrinsic atomic defects in 2D materials due to the low energy of the tunneling electron, which should leave the intrinsic defect structure to remain unaffected. Figure 13(d) shows the basic working principle of the STM technique, in which the STM tip (platinum-iridium blend) scans the surface of a sample and measures the tunneling current as a function of the distance (d) between the tip and the surface of the sample. The equation of governing tunneling current is written as $I(d) \propto eV_b \times e^{-\frac{2d\sqrt{2m\Delta\phi}}{\hbar}}$, where m is the electron mass, $\Delta\phi$ is the work function difference, $\hbar$ is the reduced Planck constant and V_b is the offset bias voltage. The STM imaging technique has been applied on various 2D materials, including graphene, black phosphorus and TMDCs, to reveal the electronic nature of intrinsic defects such as point defects, surface defects, dopant impurities, dislocation, and grain boundaries in bulk as well as in atomically thin monolayers [201–206]. An example of

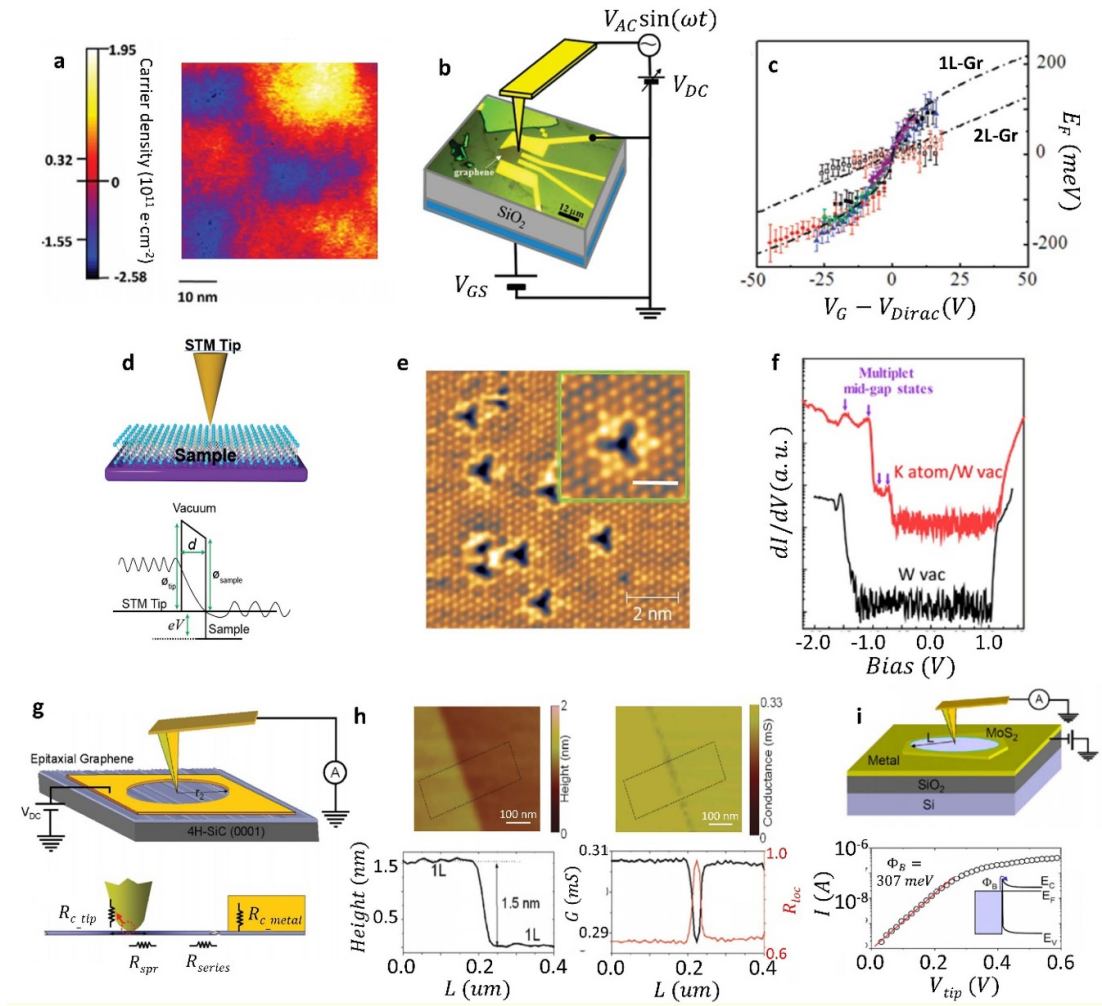

Figure 13. (a) Charge density map obtained from an STM dI/dV spectrum revealing charge fluctuation in graphene induced by a SiO_2 substrate [183]. (b) Schematic illustration of KPFM measurement setup and (c) the extracted E_F of graphene depending on the applied gate voltages [189]. (d) Schematic model of the working principle of the STM system. (e) Atomically resolved STM image of intrinsic tungsten (W) vacancies in multilayer WSe_2. Inset shows an enlarged image. (f) Logarithmic dI/dV spectra for K/W_{vac} (red) and intrinsic W_{vac} (black) in multilayer WSe_2 [195]. (g, h) Device schematic and resistance distribution in the CAFM measurement of the local conductivity of graphene on SiC due to differences in SiC topography [196]. (i) SBH measurement of metal-MoS_2 contacts using the CAFM technique. The technique allows nanoscale mapping of SBH [197].

an STM image of WSe_2 is given in figure 13(e) and the corresponding dV/dI spectra showing the bandgap and defect-induced mid-gap states are depicted in figure 13(f).

Another important surface and electrical characterization methodology used in the field of 2D materials is conductive atomic force microscopy (CAFM). The lateral resolution of CAFM sits right between that of STM and conventional electrical probes. CAFM uses an ultrasharp conductive tip to apply electrical stress on the sample of interest. Typical CAFM systems can provide a lateral resolution of ~10 nm, which is adequate for characterizing small channel (sub-100 nm) 2D devices. In the field of 2D materials, CAFM is generally used to map the lateral inhomogeneity in current transport that arises from several intrinsic and extrinsic factors, such as charge puddles, polymer residues, grain boundaries, and trap states. Giannazzo *et al* used CAFM to determine the substrate-dependent conductivity of epitaxial graphene on a SiC substrate [196]. The device structure is shown in figure 13(g); epitaxial graphene was grown on a 4H-SiC substrate using sublimation and then scanned with a Pt-coated Si tip. The local current in this device differs on the $(11\bar{2}n)$ facets compared to the (0001) basal plane terraces, which indicates that the local conductivity of graphene can vary significantly depending on the facets of SiC, as shown in figure 13(h). Another novel application of CAFM is to investigate current transport at nanoscale metal-TMDC interfaces, as shown in figure 13(i) [197]. The CAFM tip makes small area contacts with TMDCs such as MoS_2, the surface of which can be then scanned on the surface to produce a map of the nanoscale contact resistance and SBHs. Given the difficulty in fabricating high-quality contacts in 2D materials, CAFM offers a simpler means of characterizing current transport at the metal-2D material interface and has the additional advantage of producing area scans [207].

9. Outlook and conclusion

Electrical characterization methods for atomically thin 2D electronic devices must be revisited since the techniques used for conventional 3D-based semiconductors do not properly model 2D devices. Also, challenges remain concerning the characterization of the electrical properties of anisotropic 2D layered materials, which show different carrier transport behavior between the in-plane and out-of-plane directions due to the tunnel barrier formed only along the out-of-plane direction. Electrical characterization techniques unique to surface-dominant 2D semiconductors with layered materials need to be developed, which are separate from the techniques used for conventional semiconductors. For example, electrical response-based surface characterization techniques such as SPMs can detect localized charge distribution, doping density, defects, SBHs, mid-gap states, and bandgap, as discussed in the last section. These methods can also be advantageous in analyzing charge traps, which give rise to Fermi level pinning and leaky device performance. However, most SPMs do not provide straightforward information about the correlation between localized effects such as charge puddles and macroscopic electrical quantities such as mobilities and contact resistances; thus, collaborative efforts involving material and device engineers are needed.

One of the challenges in ensuring the reliability of electrical contacts to 2D semiconductors is the Schottky barrier with the metal contact, which is unlike the conventional contacts on highly doped bulk semiconductors. We find that the TLM used to measure contact resistance for Ohmic contact devices brings about large errors for some 2D devices showing Schottky current transport behavior. It is worth mentioning that *C*–*V* measurements have been significantly limited in characterizing 2D devices compared to the conventional Si devices, despite the fact that these can provide valuable information on the device properties such as interfaces, semiconductor junctions, dielectric characteristics, as well as charge traps. Although it is difficult to conduct *C*–*V* measurements for 2D devices fabricated with mechanically exfoliated small-sized 2D materials, it is clear that these methods will accelerate the development of future 2D devices, particularly when large-scale 2D materials are more widely available. Last but not least, the reliability of the electrical characterization of 2D devices needs to be ensured, particularly given the presence of non-uniform interfaces and surfaces that are affected by device process-generated residues and air ambience.

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