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Fault tolerant methods to reconfigure Multilevel level inverter for single and multiple open circuit switch faults

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Abstract.Device ratings limitations of two-level inverters restricted their applications and increased the demand for Multilevel inverters (MLI) for various high-power medium-voltage applications. However, it is not just the low device ratings that have enhanced the impact of MLI, but there are other key factors such as less good harmonic profile (filter size) and fault tolerance. Fault tolerance of MLI sustaining the various internal and external faults contributes to inverter reliability and plays a vital role to enhancing practical feasibility. However, achieving fault tolerant operation of MLI by control its switching operation rather than involving any external/auxiliary hardware is the most economical solution. Thus, considering the most popular modular redundant classical MLI i.e., Cascaded H-Bridge, this paper presents the simplest fault tolerant strategies practically used to reconfigure CHB from open circuit (oc) switch fault(s). The fault tolerant operation (FTO) is demonstrated considering three-phase eleven-level CHB in MATLAB/Simulink environment

1. Introduction

Multilevel inverters such as DCMLI, FCMLI and CHB are preferred to high-power two-level inverters due to their reduction in device rating, dv/dt, THD, EMI and common mode voltage. The demand for MLI inverters and gathered attention on classical MLIs from academia and industry has provoked their wide market penetration. However, the Increased switch count of MLIs at higher levels, has not only increased circuit complexity but also created reliability concern. Increased component count of these MLI topologies has increased the probability of fault occurrence and raised the issue of reliability of the inverter [1]. Thus, identification, diagnosis and supressing of faults on MLI emerged as a significance objective for various applications. This has driven the necessity to investigate fault behaviour and, their effect on operation & performance of MLIs [2-6].

There are various internal and external causes for fault occurrence in power converters. Even though the appeared is temporary or permanent, in common all the faults either end with open circuit (OC) or short circuit of the switch (SC) temporary or permanently. A fault is said to be temporary if, it

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settles down in less than two cycles without creating any hazardous effect on the current and voltage flowing through the device. If not, it can be considered as permanent fault. Permanent fault often ends up created either partial/complete temporary/permanent physical damage on the device [6-7]. Supressing/elimination of SC faults mandatorily requires hardware components such as fast acting relays, circuit brakers and fuses to avoid dangerous current flowing in, contributing to over-current protection. Therefore, this paper presents the investigation on fault tolerant operation of MLI for OC faults. In literature, various methods are reported to detect the type and location of the fault. Fault identification by switch voltage/current measurement and output voltage/current measurement are reported. In contrast to the above, fault tolerant topologies which doesn't require any fault detection methods are also reported. These topologies involve fast acting fuses and bidirectional switches such as TRIAC or protection device such as relays to detect and isolate the fault [8-10]. Few topologies with auxiliary equipment are reported, which has the capability of suppressing the fault, however it should be detected by external means. Topologies with additional redundant phase-leg unit/phase are reported to obtain fault tolerant operation. It is to be noted that, switching redundancies play a vital in reconfiguration of inverter. In detail, during open circuits faults, switching redundancies, provides an alternative path for the load current and contribute to output voltage. Thus, CHB being the simplest classical MLI configuration with good redundancies, this paper considered CHB configuration and estimated its performance for OC faults.

Organization of this paper is as follows: In section II, operation of CHB in normal and fault conditions is presented using phasor diagrams. Section-III presents the investigative discussion on methodology and limitations of practical fault tolerant approaches i.e., by-passing and Increasing burden methods. Section -IV presents implementation and performance by-passing method and increasing burden method on a three-phase-nine level CHB. Further, following conclusion and references are presented.

2. Behaviour of CHB-MLI under OC switch fault(s)

Assuming a stiff voltage Vdc across the dc-link capacitors, the three-phase circuit configuration of nine-level CHB is shown in figure 1. With, no fault acting CHB produces a balanced set of phase and line-voltages.



Figure 1. Three-phase 11-level CHB MLI.

Figure 2 shows the phasor representation of the phase-voltage obtained in healthy operation of CHB, where V_a , V_b and V_c corresponds to phase-voltages, and V_{ab} , V_{bc} , and V_{ca} corresponds to line-voltages. With k varying from 1 to 5, V_{a1} , V_{a2} ,... V_{ak} corresponds to the ac voltage contributed by each H-bridge of phase-a. Similarly, for phase-b and c. The expected balanced phase-voltages are given in (1) [8-9]



Figure 2. Phasor representation Balanced operation.

Assuming $v_{a1} = v_{a2} = v_{an} = m_a V_{dc} \sin \omega t$ and m_a is amplitude modulation index. Similarly, for phase-b and c, $v_b = \sum_{k=1}^n v_{bk}$ and $v_c = \sum_{k=1}^n v_{ck}$. Therefore,

$$\left. \begin{array}{l} v_a = nm_a V_{dc} \sin \omega t \\ v_b = nm_a V_{dc} \sin (\omega t - 120^\circ) \\ v_c = nm_a V_{dc} \sin (\omega t - 240^\circ) \end{array} \right\}$$
(1)

Fault on any H-bridge will create un balance operation and produces degraded phase and line performance. To fault on a switch may force the inverter to miss a positive level or negative level in output voltage. For example, if an OC fault appears on S11a, then that respective fault bridge can no longer produce +Vdc, which limits peak magnitude of phase-voltage to +Vdc. This effect is similar for the if the fault appears on top switch of first leg or bottom switch of second leg in any H-bridge. In case of vice-versa, negative level will be missed. In such as case, dc-off set is produced in phase-voltages, in addition to unbalance in line-voltages.

To avoid this and create a symmetrical effect on positive and negative levels, the faulted used is passed i.e., forced to contribute zero voltage to output voltage. Thus, if an OC fault appears on S11a, then S41a and S21a are turned ON and its corresponding output is forced to zero. However, to in case of OC fault on multiple switches of a H-bridge, an external switch is used to by-pass the faulty unit. This method of restricting voltage contribution of fault unit creates unbalance in phase-voltage and line-voltages, which further leads to flow of enormous circulating currents. Thus, assuming the contribution of faulted unit as zero, the effect of OC fault on phase-voltage magnitude and levels is given in Table 1, where 'n' number of cascaded bridges, considered case n=5.

No. of faulty units	Missing levels in phase voltage
0	None
1	$\pm n V_{dc}$
2	$\pm nV_{dc}and \pm (n-1)V_{dc}$
k	\pm (n) V _{dc} , \pm (n-1) V _{dc} , \pm (n-k)V _{dc}

 Table 1. Effect of OC fault on phase voltage levels.

Assuming one faulty unit in phase-a, two units in phase-b and three-units in phase-c, the phasor representation of produced unbalance is shown in figure 3.



Figure 3. Unbalance for single faulty on phase-c.

In general, with x faulty units in phase-a, y faulty in phase-c and z faulty in phase-c of an inverter with '*n*'-operating units, the output unbalanced phase voltages will be as given in (2)

$$\begin{array}{l} v_{a} = (n-x)[m_{a}V_{dc}\sin\omega t] \\ v_{b} = (n-y)[m_{a}V_{dc}\sin(\omega t - 120^{\circ})] \\ v_{c} = (n-z)[m_{a}V_{dc}\sin(\omega t - 240^{\circ})] \end{array}$$

where k = 1, 2, (n-x) for phase-*a*; k = 1, 2, (n-y) for phase-*b* and k = 1, 2, ..., (n-z) for phase-*c*.

3. Fault tolerance: Practical approaches

Involvement of any hardware components complicates the topology and raises the overall cost. Hence, various PWM schemes with-out involving any auxiliary equipment to obtain FTO are reported. PWM schemes such as space vector modulation (SVM) and carrier-based schemes are reported. Among PWM based schemes, Though SVM is an attractive to achieve FTO as it operates by creating switching redundancies, it is complex in implementation at higher levels [8-12].

On the other side, irrespective to the hardware solutions or PWM schemes, fault tolerant schemes (FTS), which generates a new set of modulating signals to reconfigure the inverter to obtain FTO are reported. These schemes can be applicable to the inverter with modular redundant topological structures such as CHB. Among these schemes, (a) by-passing method, (b) increasing the burden on healthy units/cells and (c) Neutral shifting (NS) FTS are the popular schemes reported to tolerate OC switch faults in CHB MLI. This paper presents the discussion on By-passing and increasing burden methods.

3.1. By-passing method[12-13]

One of the simplest approaches to restore the balanced operation is to ensure the number of operating units on all the phases are equal. To restore the balanced operation, this method by-passes few healthy units on one or more phases, such that the number of operating units on all the phases are same. Thus, this method of compensation forces the voltage contributed by few healthy units on one or more phases to zero, such that voltage contributed by all the phases is same. The number of healthy units to be by-passed depends on number of operating units on each phase. It is to be noted that the by-passing should not be carried out on the phase with maximum number of faulty units, as this phase contributing lowest voltage. For example, three units are operating in each phase in healthy condition, this fault tolerant method for one-unit fault in phase-*a* is illustrated in Figure 4. If a fault appears on one unit of phase-*a*, then the total voltage contributed by phase-*a*, *b* and *c* are $\pm 2V_{dc}$, $\pm 3V_{dc}$ and $\pm 3V_{dc}$. Thus, to restore the balanced operation, this method by-passes one unit on phase-*b* and phase-*c*, ensures the operating units on all phases are same with each phase producing a maximum voltage of $\pm 2V_{dc}$ as shown in figure 4. This method is easy to implement and can compensate simultaneous failure of multiple switches.



Figure 4. Illustrating balanced condition with by-passing method.

However, by-passing of the operating units, derates the inverter and reduces its efficiency. Thus, for achieving FTO without by-passing any healthy unit, "increasing burden" FTS is reported and is presented below.

3.2. Increasing burden[12-13]

This method obtains FTO by sharing the burden of faulty units of a phase across the healthy units of same phase, such that magnitude of the overall phase-voltage after compensation is equal to its pre-fault voltage. Sharing this fault burden, enforces additional burden on healthy units thus this method of fault compensation is called as increasing burden method. For example, consider a CHB with fault condition shown in Figure 3, where the unbalanced phase-voltages are given in (2). In such condition, to compensate the fault, this method shares the burden of x faulty units of phase-a across (n - x) healthy units of the same phase, such that total voltage contributed by these (n - x) healthy units is same as that of the total voltage contributed by n units in pre-fault condition. This increases a burden of $\frac{n}{(n-x)}$ in each operating unit of phase-a. Similarly, a burden of $\frac{n}{(n-y)}$ for phase-b and $\frac{n}{(n-z)}$ for phase-c is increased for each operating unit. Thus, this method of compensation produces balanced phase-voltages $(v_a', v_b' \text{ and } v_c')$ as given in (3) and shown in figure 5



Figure 5.Illustrating fault compensation with increasing burden method.

$$v_{a}' = (n-x) \left[\frac{n}{(n-x)} m_{a} V_{dc} \sin \omega t \right]$$

$$v_{b}' = (n-y) \left[\frac{n}{(n-y)} m_{a} V_{dc} \sin(\omega t - 120^{\circ}) \right]$$

$$v_{c}' = (n-z) \left[\frac{n}{(n-z)} m_{a} V_{dc} \sin(\omega t - 240^{\circ}) \right]$$
(3)

This scheme can compensate simultaneous failure of multiple switches and obtains balanced operation without by-passing any of the operating (healthy) unit. However, this method possesses the following limitations.

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Non-uniform power distribution among operating units: From Figure 5, the magnitude of voltage contributed by each unit in phase-a, is different from phase-b and c, respectively. This non-uniform burden among the operating units result non-uniform power distribution. This further reflects unbalance in dc link voltages, which is not desired in closed-loop applications.

Drives to overmodulation: If the number of faulty units increases, then the amplitude modulation index increases and drives the phase-voltage to overmodulation.

4. Simulation Results

Assuming each dc source of 100 V, switching frequency as 3000Hz and ma as 0.95, the recorded simulation results for single unit fault on phase-a of 11-level CHB are shown Figure 6. Further, its corresponding fault tolerant operation with by-passing method is shown in figure 7. Further, the FTO with increasing burden method for ma=0.95 and ma=0.85 are given in figure 8 and 9 respectively. The popular level shifted PWM is incorporated to extract the switching pulses. It is to be noted that switching pulses to the faulty H-bridge is seized and it is by-passed.



Figure 6. Unbalance for simple unit fault on phase-of 11-level CHB.

Figure 6, claims the produced unbalanced phase and line voltages due the presence of single faulty unit on the phase-a, where the phase and line voltage balance not only reflect in wave shape but also on RMS values.

4.1. Fault tolerance with By-passing method

The CHB reconfiguration for appeared single OC fault using by-passing method is projected in figure 7. Results are figure 7 are obtained by by-passing on healthy operating unit in each healthy phase-b & c. This ensures the number of operating units on all phases as same, and restricts the inverter to operate for 9-level rather than 11-level. This FTO derates the inverter as it reduces the magnitude of phase and line voltage.



Figure7. FTO of By-passing method for unit fault.

4.2. Fault tolerance with Increasing burden method

The reconfiguration of CHB supressing the appeared single open circuit switch fault on any H-bridge of phase-a, using increasing burden method is shown in figure 8 and 9.



Figure 8. FTO of Increasing burden scheme for single unit fault on 11-level CHB at ma=0.95.

Increasing burden imposes fault burden on the healthy operating units of the faulty phase and force them to produce the same magnitude phase-voltage as of in pre-fault condition. Thus, this drives the faulty phase i.e., phase-a to over-modulation and, operates the healthy phases phase-b and c unaffected. However, for the considered fault case forcing the faulty phase to over-modulation increases its operating ma to 1.33ma, where ma is pre-fault modulation index.

With ma=0.95, the overall post fault modulating index is 1.26. However, reconfiguration of inverter for ma>1.25 faces severe non-linearity and fails to achieve FTO. This is reflected in figure 8, where the line and phase unbalanced in terms of rms values can be noticed. This can be addressed by reducing the pre-fault modulation index to 0.85, which further reduces the non-linearity on the converter and achieve balance phase-voltage in terms of magnitude (rms) and, balanced line-voltage both in terms of waveshape and magnitude (rms).



Figure 9. FTO of Increasing burden scheme for single unit fault on 11-level CHB at ma=0.85.

5. Conclusion

This paper investigated popular and fundamental fault tolerant approaches of MLIs, considering cascaded H-bridge configuration. The demonstrated fault tolerant schemes by-passing method and increasing burden are easy to implement and don't require any hardware/auxiliary components. However, By-passing method reduces the converter efficiency due to by-passing healthy operating units. On the other hand, increasing burden drives the converter to over modulation and attains balanced line-line voltages. Thus, increasing burden methods forces the controller to mandatorily reduce the pre-fault modulation index for attain satisfactory FTO.

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