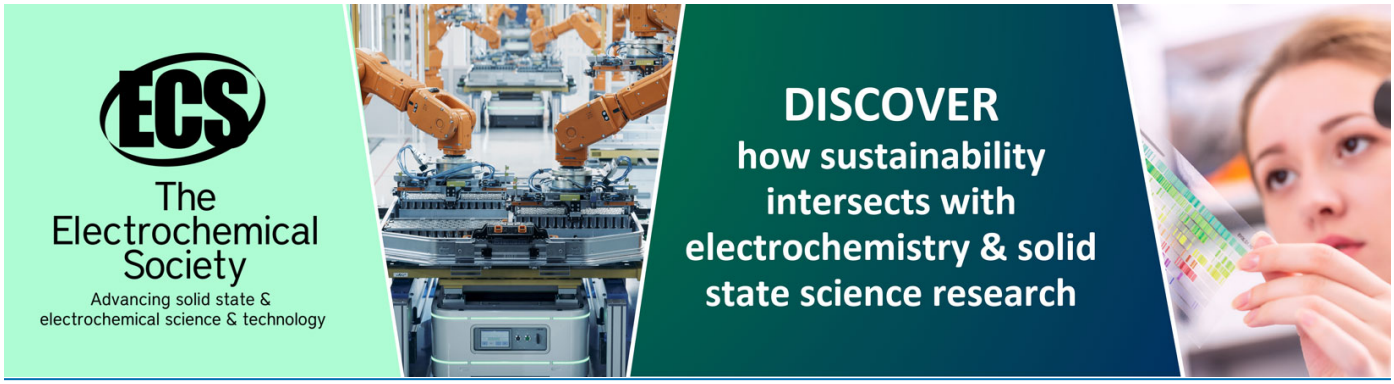
# SPIROC: design and performances of a dedicated very front-end electronics for an ILC Analog Hadronic CALorimeter (AHCAL) prototype with SiPM read-out





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# SPIROC: design and performances of a dedicated very front-end electronics for an ILC Analog Hadronic CALorimeter (AHCAL) prototype with SiPM read-out

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ABSTRACT: For the future e+ e- International Linear Collider (ILC) the ASIC SPIROC (Silicon Photomultiplier Integrated Read-Out Chip) was designed to read out the Analog Hadronic Calorimeter (AHCAL) equipped with Silicon Photomultiplier (SiPM). It is an evolution of the FLC_SiPM chip designed by the OMEGA group in 2005. SPIROC2 [1] was realized in AMS SiGe 0.35 $\mu$m technology [2] and developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of read-out channels. This ASIC is a very front-end read-out chip that integrates 36 self triggered channels with variable gain to achieve charge and time measurements. The charge measurement must be performed from 1 up to 2000 photo-electrons (p.e.) corresponding to 160 fC up to 320 pC for SiPM gain $10^6$. The time measurement is performed with a coarse 12-bit counter related to the bunch crossing clock (up to 5 MHz) and a fine time ramp based on this clock (down to 200 ns) to achieve a resolution of 1 ns. An analog memory array with a depth of 16 for each channel is used to store the time information and the charge measurement. The analog memory content (time and charge) is digitized thanks to an internal 12-bit Wilkinson ADC. The data is then stored in a 4kbytes RAM. A complex digital part is necessary to manage all these features and to transfer the data to the DAQ. SPIROC2 is the second generation of the SPIROC ASIC family designed in 2008 by the OMEGA group. A very similar version (SPIROC2c) was submitted in February 2012 to improve the noise performance and also to integrate a new TDC (Time to Digital Converter) structure. This paper describes SPIROC2 and SPIROC2c ASICs and illustrates the main characteristics thank to a series of measurements.

KEYWORDS: Front-end electronics for detector readout; Solid state detectors

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## Contents



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## 1 Introduction

The SPIROC2 chip is a System on Chip (SoC) that was designed in the framework of the CALICE collaboration and the European program EUDET to read-out the AHCAL calorimeter equipped with SiPM for ILC. The calorimeter prototype is designed by the German group of the DESY laboratory. Figure 1 [3] displays the Electromagnetic (ECAL) and Hadronic CALorimeter (HCAL), developed within the CALICE collaboration. The aim is to have a dense calorimeter with a high granularity (10 million channels). The thin detection gaps are made of active sensors with embedded readout electronics. Therefore any space for infrastructure has to be minimized. One of the major requirements is consequently to minimize power to avoid active cooling in the detection gap. The envisaged detector architecture is sketched in figure 1 (left picture). The barrel of the AHCAL has a cylindrical structure and will be placed outside the electromagnetic calorimeter, while it is surrounded by the magnet. The cylindrical structure is divided into 16 segments with 48 detector layers each. The figure 1 (right picture) shows one sector of a barrel. One active layer consists of three parallel slabs. Each slab is again subdivided in six HCAL basic units (HBU). These HCAL base units (HBU) are made of 144 scintillator tiles, 3 mm thick with embedded SiPMs read out by four SPIROC ASICs (figure 2).

As the electronic is embedded inside the detection layer (figure 2), its power consumption must be as low as 25 $\mu$W per channel to avoid active cooling in the detection gap.

SPIROC2 is one of the second generation of readout ASICs designed in 2008 by the OMEGA group to equip technological prototypes. SPIROC2 reads out SiPM detectors. It is therefore used in numerous applications such as medical imaging, astrophysics, volcanology and nuclear physics.

The main features of the ASIC are:

- auto trigger mode to reduce the data volume, with a threshold of 1/3 of p.e. (50 fC for SiPM gain $10^6$);
- Charge measurements up to 2000 p.e. (320 fC for SiPM gain $10^6$);

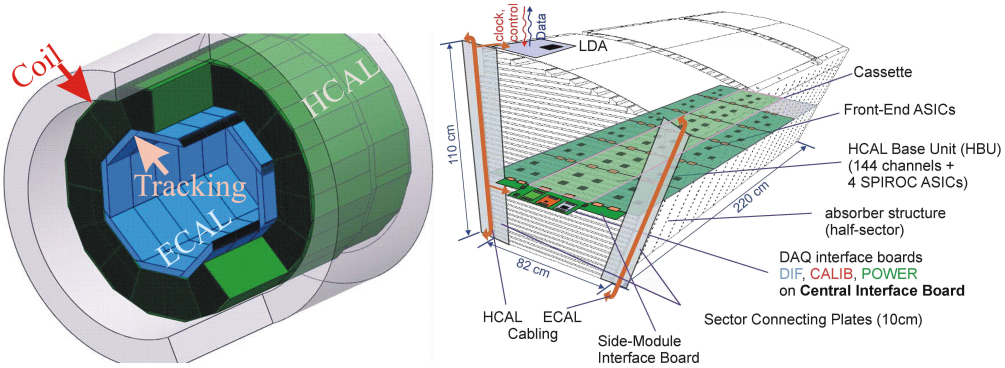


**Figure 1**. Left: ILC calorimeter developed by the CALICE collaboration divided in an Electromagnetic (ECAL) and Hadronic CALorimeter (HCAL). Right: a 1/16 half-barrel of the Analog HCAL (AHCAL).

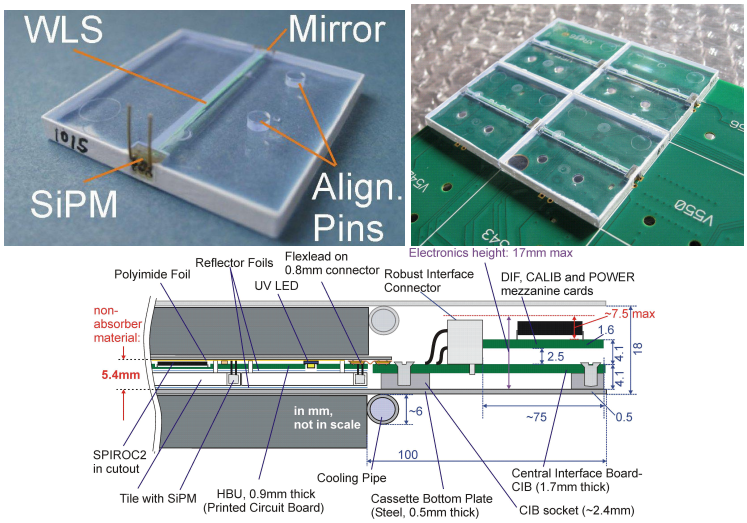


**Figure 2**. [4] Left: a scintillator tile equipped by SiPM. Right: a zoom of the slab implemented by SPIROC ASIC and the active sensor. Bottom: a scheme of the detection layer.

- Time measurements with a resolution of 1ns;
- Power-pulsing to reduce the power dissipation by a factor 100 and to achieve 25 $\mu$W per channel.

A very similar version (SPIROC2c) was submitted in February 2012 to improve the noise performance and also to integrate a new TDC (Time to Digital Converter) structure.

## 2 SPIROC2c architecture

The SPIROC2c ASIC architecture is shown in figure 3. It has the same mean features of the SPIROC2 and a similar architecture.

The analog core is composed of 36 channels. Each channel embeds an input DAC to tune SiPM high voltage on 5V. Two input preamplifiers (PA HG and LG in figure 3) are needed to handle the requested large dynamic range. They are followed by a trigger line made of a fast shaper (FSH in fig-



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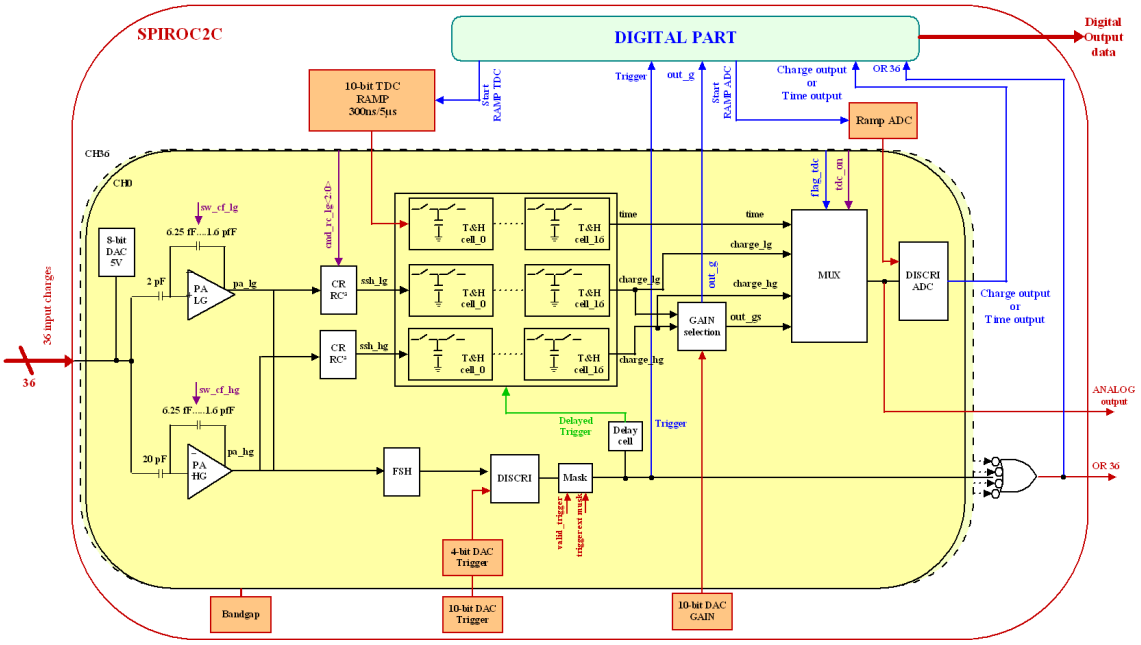


**Figure 3**. General schematic of SPIROC2c SIC. In yellow the one channel schematic, in orange the 36 channel common bloc and in green the common digital part with the main digital signals.

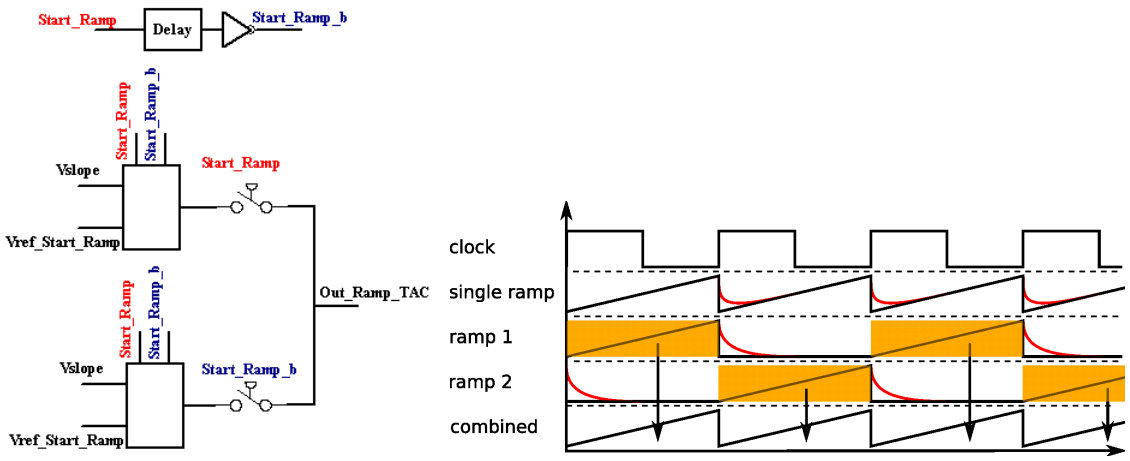


**Figure 4**. Block diagram and general schematic of the two TDC ramps of SPIROC2.

ure 3) and a discriminator (Discri in figure 3). The charge measurement line is made of two variable slow shapers (CRRC$^2$ in figure 3) and two 16-deep Switched Capacitor Arrays (T&H in figure 3).

The time is characterized by two measurements: a coarse time stamp performed by a 12-bit counter at a maximum frequency of 5MHz and a fine time obtained thanks to a TDC (Time to Digital Converter). The TDC signal is stored in the analog memory (SCA), in parallel with the charge. A 12-bit Wilkinson ADC is used to digitize the analog charge and time values at the end of the acquisition period.

The digital part is complex as it must handle the SCA write and read pointers, the ADC conversion, the data storage in a RAM and the readout process.



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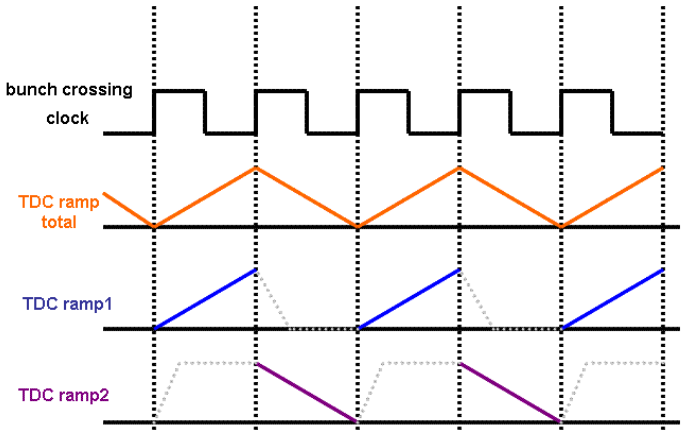


**Figure 5**. General schematic of the two TDC ramps of SPIROC2c.

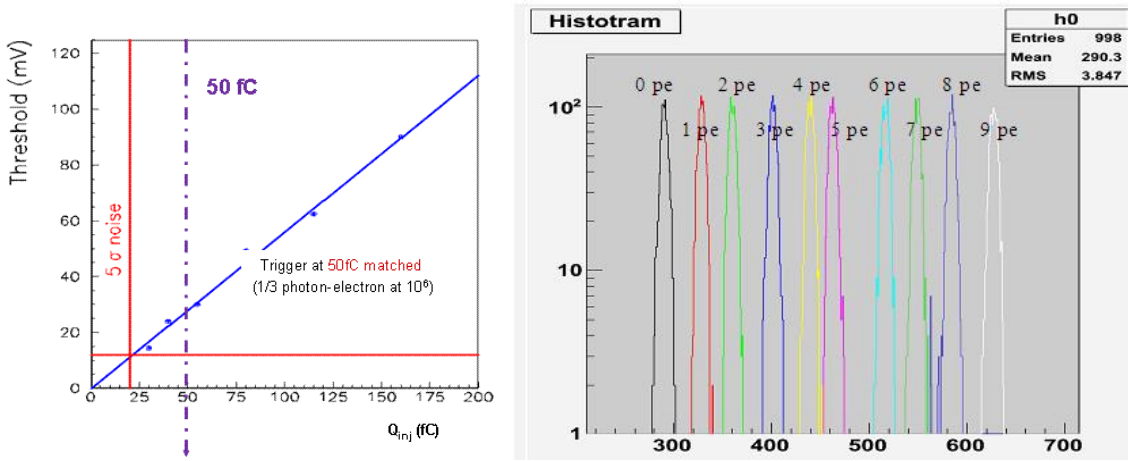


**Figure 6**. Left: trigger efficiency measurements, the threshold in mV is plotted versus the injected charge. The 5$\sigma$ noise and the 1 pe (50 fC) are stressed. Rigth: charge measurements for various injected charges. The accuracy value is plotted versus the charge in ADC count.

### 2.1 Input stage

A new voltage preamplifier structure has been designed in SPIROC2c to decrease its sensitivity to the power supply noise and therefore to improve the signal over noise ratio. The high gain (Gain=10) and low gain preamplifiers (Gain=1) have an input NMOS transistor (instead of the PMOS in SPIROC2) to reduce the coherent noise. Moreover each preamplifier has a variable feedback capacitor in order to adjust the high gain and low gain independently which was not possible in the SPIROC2 version. This tuning is very convenient to compensate the non-uniformity of the 36 channels.

### 2.2 TDC

In SPIROC2, the TDC is designed as a Time to Amplitude Converter (TAC).

The fine time measurement is performed by the SCA which samples a ramp (related to the bunch crossing clock), common for all channels, at the same time of the charge. An ADC converts this voltage value in a digital one.



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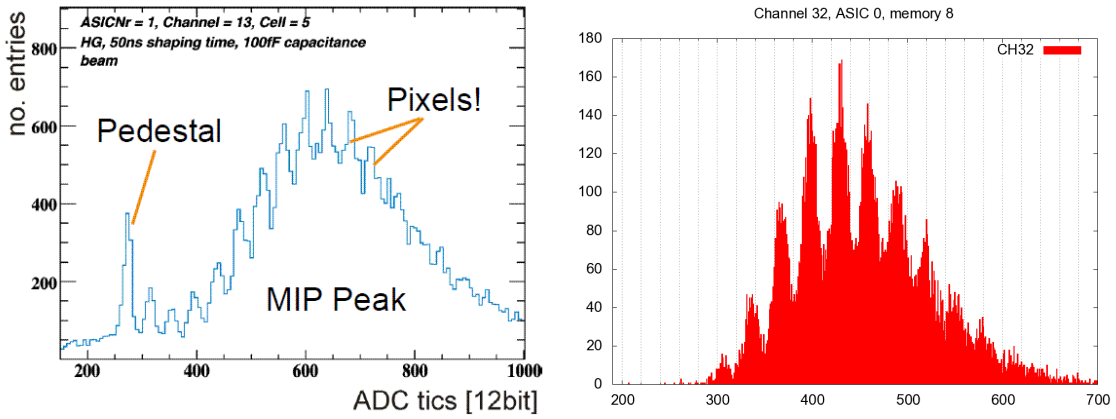


**Figure 7**. MIP (Minimum Ionizing Particle) distributions are plotted. Left: measurements at Desy laboratory with a 6 GeV electron test beam. Right: spectrum obtained in Prague laboratory with a LED calibration system.

The ramp is formed by a reference current generator and an integrator. The reference current flows into the amplifier input and is integrated in the feedback capacitor. The current, which flows in feedback, charges and discharges the capacitance Cf when the switch is turned off and on respectively, so the output of the amplifier gets a ramp voltage wave. The signal, named "start ramp", sent by the digital part and synchronized with the clock (clock of the timestamp), manages the switch. The signal rising edge starts the ramp and the falling one stop the ramp.

The final ramp is the result of two of these ramps which are selected thanks to the start ramp signal that commutates alternatively two switches (figure 4).

The ramp has been tested in Desy laboratory [5] considering a clock of 5 MHz showing a good resolution of 125–150 ps, a good ramp length of 220 ns (a bit more than expected) but with a dead time of around 100 ns, nearly 50% of the ramp length.

SPIROC2c ASIC implements a new structure of the ramp. The new structure has the same principle of operation of the old one but the second ramp has a negative slope. This structure can reduce the dead time of the old version (figure 5). This is a preliminary solution waiting for a new structure, more complex, that implicates a huge change in the ASIC and will be implemented in the third generation of the SPIROC ASIC.

## 3 Measurements

The ASIC was sent for fabrication in February 2012 and a batch of 5 packaged ASICs and 20 dies were received in June 2012. The die has a surface of 32 mm2 (4.2 mm $\times$ 7.2 mm) and is packaged in CQFP240 case.

SPIROC2c is pin-pin compatible with SPIROC2 allowing to perform the measurements using the same testboard. A dedicated Labview program allows to send the ASIC configuration parameters and to receive the output bits via an USB cable connected to the test board. A signal generator is used to create the input charge injected in the ASIC. As possible, the signal injected is similar



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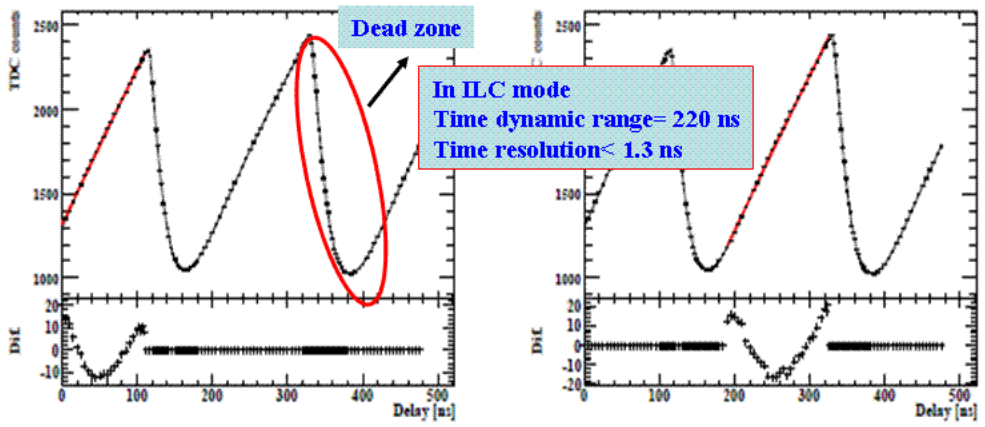


**Figure 8**. TDC ramp reconstruction tested in Desy laboratory. The dead time is emphasized in red.

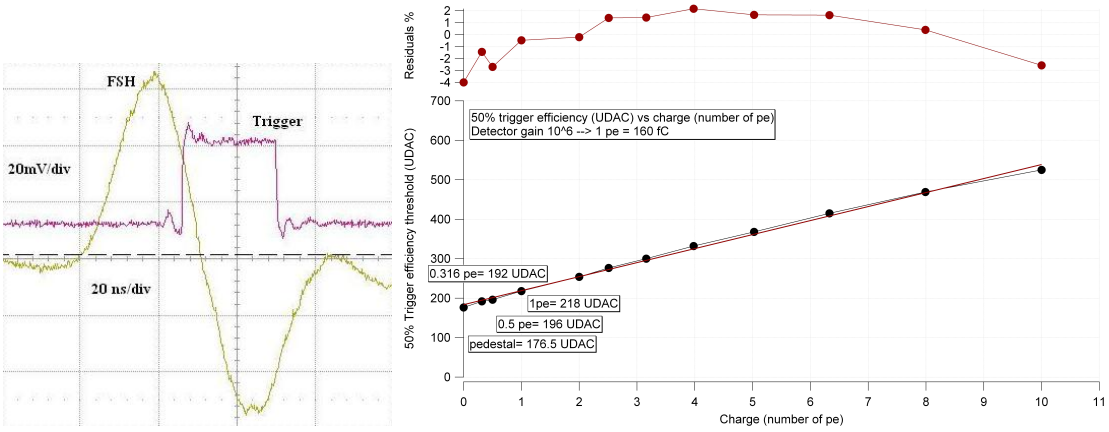


**Figure 9**. Left: fast shaper signal for 1 pe input signal and trigger signal. Right: 50% of trigger efficiency in DAC units (UDAC) (LSB= 1.8 mV) vs the injected charge in number of pe.

to the SiPM signal. The input signal is a voltage step injected in a capacitor of 100 pF to give a charge of 160 fC for one p.e. supposing a SiPM gain of $10^6$.

The SPIROC2 ASIC [1] has been tested showing the ASIC capability to detect an input signal of 1/3 of p.e. (figure 6 left plot) and to perform charge measurement (figure 6 right plot) (figure 7).

The time performances indicate that the ASIC can give a fine time measurements with resolutions of 1 ns but with a large dead time of 100 ns (figure 8).

The preliminary tests of the SPIROC2c indicate a good signal to noise ratio (SNR) of 30 for the trigger channel and for an input signal of 1 p.e. (figure 9). Therefore the ASIC can detect 1/3 of p.e. which is confirmed by the trigger efficiency measurements displayed on figure 9. The linearity is correct (with residuals from 4% to 2% referring to the measured values) down to 27 fC, which corresponds to 5 $\sigma$ noise with $\sigma$ at 5.3 fC. This confirms that the threshold can be set at 1/3 of p.e. (50 fC).



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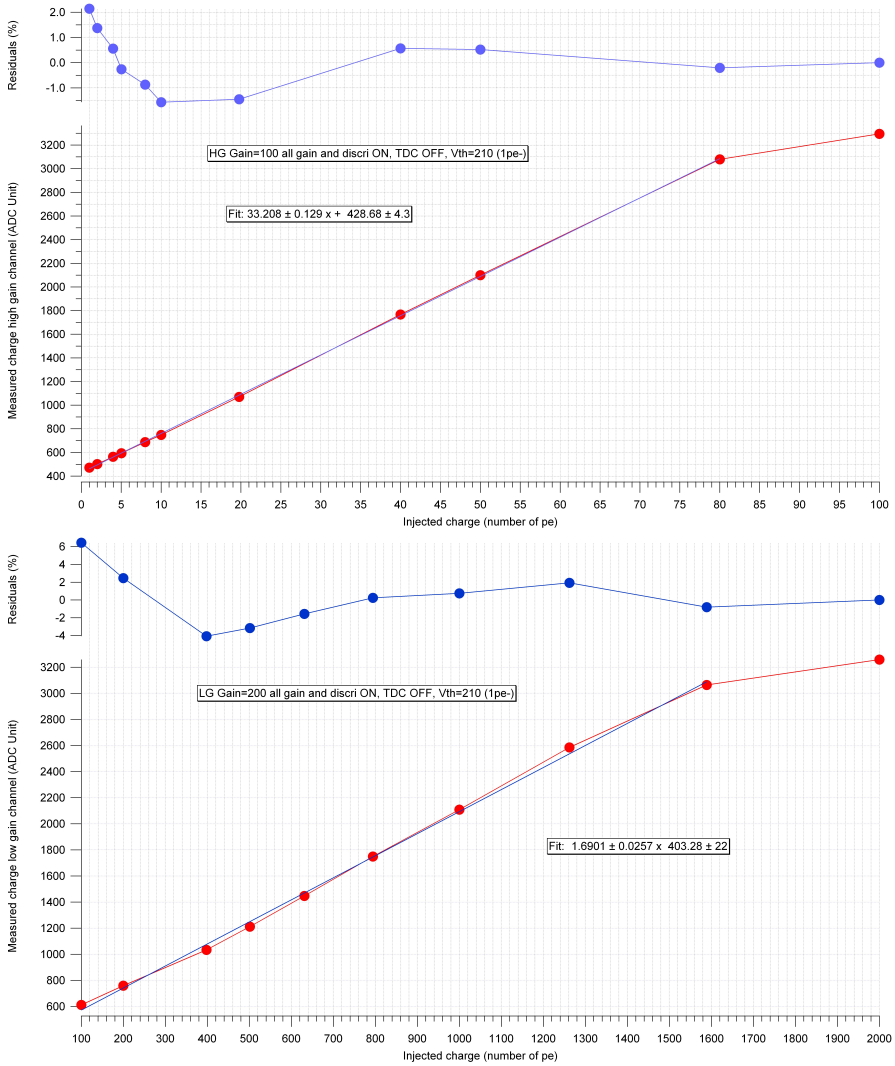


**Figure 10**. Measured charge in ADC units vs the injected charge. High gain channel on the top up to 100 pe and for low gain channel on the bottom up to 2000 pe.

The linearity of the low gain slow shaper (Gain=1) and the high gain slow shaper (Gain=10) has been measured in the auto-trigger mode with a threshold set to 1 p.e. and using the Switched Capacitor Arrays and the 12-bit ADC (LSB= 250 $\mu$V) (figure 10). The Integral Non Linearity is better than 6 % up to 1600 p.e.

The TDC ramp has been observed with the oscilloscope. Preliminary measurements of the TDC ramp have been performed showing that the dead time has been reduced (figure 11). More accurate tests will be performed on the ramp to characterize this TDC. Especially the strange behavior observed in the top of the ramp on figure 11 will be solved thanks to external resistors placed on the test board. These resistors change the Vref_start_ramp and V_slope (figure 4) that manage the slope and the reference level of the ramp.



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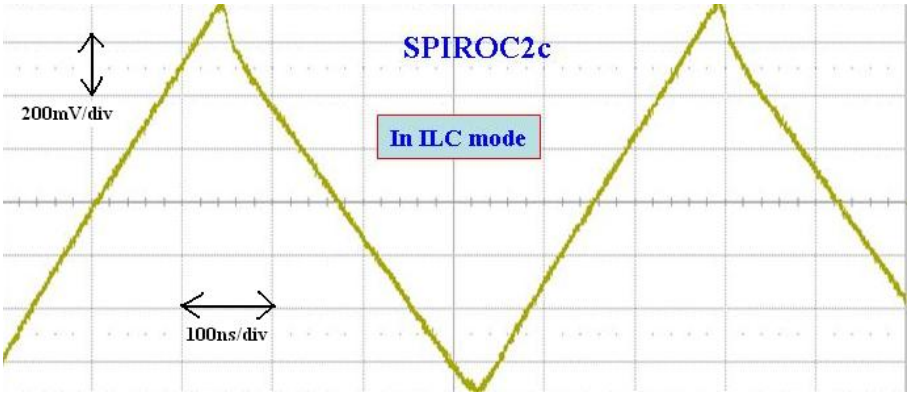


**Figure 11**. TDC ramp picture on the oscilloscope. The positive and negative slope ramps are observed. A strange behavior is observed in the top of the ramp but it can be solved thanks an external resistor placed on the test board.

## 4 Conclusions

The SPIROC2 chip is a System on Chip (SoC) that was designed in the framework of the CALICE collaboration and the European program EUDET to read-out the AHCAL calorimeter equipped with SiPM for ILC. The calorimeter prototype is designed by the German group of the DESY laboratory. SPIROC2 is one of the second generation of readout ASICs designed in 2007 by the OMEGA group to equip technological prototypes. This prototype has showed good overall behaviour in terms of auto trigger ASIC, charge measurements and digitization of the data. A very similar version (SPIROC2c) was submitted in February 2012 to improve the noise performance and also to integrate a new TDC (Time to Digital Converter) structure.

1000 chips of the SPIROC2 were produced in March 2010 to make a demonstrator in Desy laboratories and test beam measurements have been done in May 2012. A third generation with a new architecture based on independent channels will be studied and designed in the next year.

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