

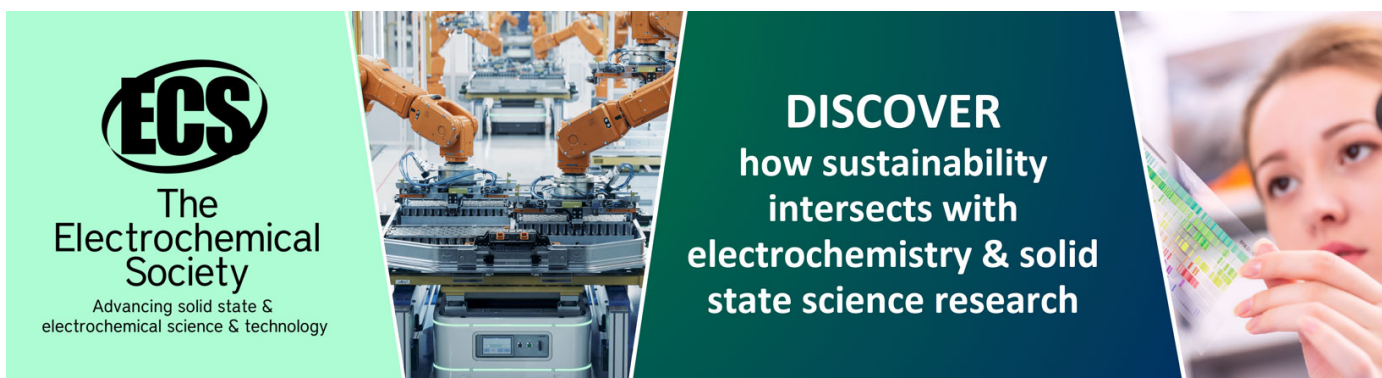
Erratum: optimizing latency in Xilinx FPGA implementations of the GBT

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Erratum: optimizing latency in Xilinx FPGA implementations of the GBT

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Erratum. The figure below replaces figure 3 on page 3, which contains two times the transmitter studies.

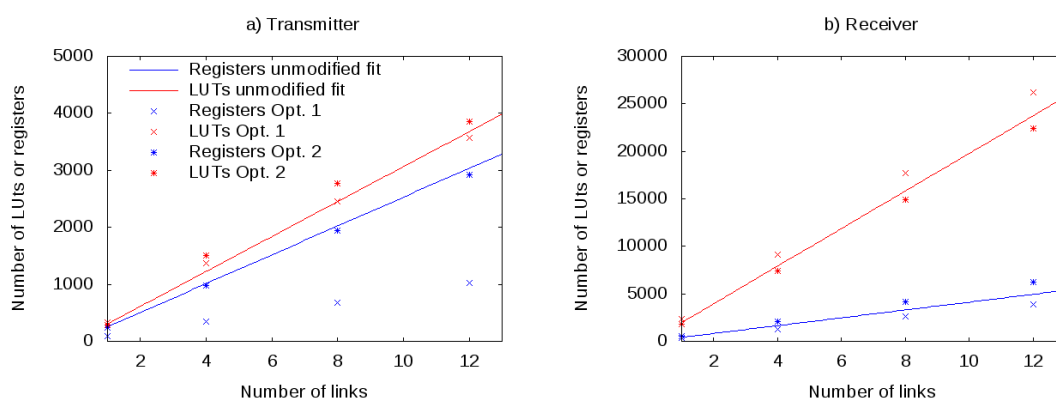


Figure 1. Utilization studies for transmitter (a) and receiver (b).

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