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Radiation tolerance of a column parallel CMOS sensor with high resistivity epitaxial layer

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ABSTRACT: CMOS Monolithic Active Pixel Sensors (MAPS) demonstrate excellent performances in the field of charged particle tracking. A single point resolution of $1 - 2 \mu\text{m}$ and a detection efficiency close to 100% were routinely observed with various MAPS designs featuring up to 10^6 pixels on active areas as large as 4 cm^2 [1]. Those features make MAPS an interesting technology for vertex detectors in particle and heavy ion physics. In order to adapt the sensors to the high particle fluxes expected in this application, we designed a sensor with fast column parallel readout and partially depleted active volume. The latter feature was expected to increase the tolerance of the sensors to non-ionizing radiation by one order of magnitude with respect to the standard technology. This paper discusses the novel sensor and presents the results on its radiation tolerance.

KEYWORDS: Si microstrip and pad detectors; Radiation-hard detectors; Particle tracking detectors (Solid-state detectors); Radiation damage to detector materials (solid state)

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Contents

1	Introduction	1
2	CMOS-sensors with massive parallel readout and on-chip data sparsification	1
3	MIMOSA-26AHR, a radiation tolerant sensor with massive parallel readout	4
3.1	Tracking performances of MIMOSA-26AHR	5
3.2	Radiation tolerance of MIMOSA-26AHR	7
3.3	Beam test results of MIMOSA-26AHR	10
4	Summary and conclusion	10

1 Introduction

The ability of CMOS Monolithic Active Pixel Sensors (MAPS) to provide charged particle tracking has been demonstrated with several MIMOSA¹ prototypes. Tests performed with 120 GeV/c pion beams at CERN proved their excellent detection performance (single point resolution of 1 – 2 μm , detection efficiency > 99.9% [1]).

MAPS have been proposed as sensor technology for the vertex detectors suited to the International Linear Collider (ILC) [2], the STAR Heavy Flavor Tracker [3] and the Compressed Baryonic Matter (CBM) experiment [4]. In those vertex detectors, the sensors are expected to be exposed to radiation doses ranging from several 10^{11} $n_{\text{eq}}/\text{cm}^2$ and few 100 kRad (ILC) to up to a few 10^{13} $n_{\text{eq}}/\text{cm}^2$ and ~ 10 MRad (CBM). Moreover, in order to keep the occupancy of the detectors reasonably low, a frame readout time in the order of 10 μs is required. The question whether the performance of MAPS for charged particle tracking can match those requirements is addressed by a joint research program of the IPHC/Strasbourg, the University of Frankfurt and GSI/Darmstadt.

2 CMOS-sensors with massive parallel readout and on-chip data sparsification

The sensing element of MAPS is formed by a sandwich of three differently P-doped silicon layers, which are the highly doped substrate, the moderately doped epitaxial layer and a highly doped P-well layer found in standard CMOS processes (see figure 1). The 10 – 20 μm thick, non-depleted epitaxial layer forms the active volume of the pixel. Free electrons excited in this volume diffuse inside the layer. The electrons cannot leave it as the doping gradients found at the interfaces of the layers generate repulsive build-in-voltages. They are collected by $P_{\text{EpiLayer}}/N_{\text{Well}}$ -diodes and loaded into the parasitic capacitor of the pixel (see box in figure 1). The related voltage drop in this capacity is buffered with a source follower and measured by an external ADC. In the conventional

¹Standing for Minimum Ionizing MOS Active pixel sensor.

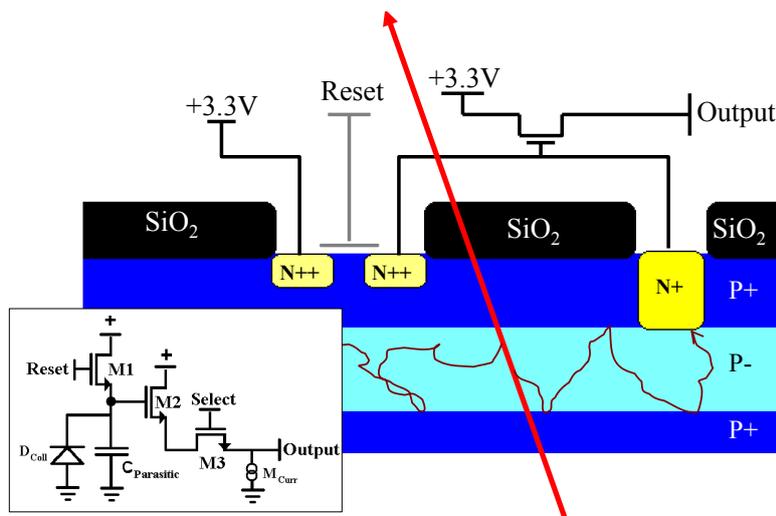


Figure 1. Fundamental layout of a CMOS-sensor. The trajectory of an impinging minimum ionizing particle (red arrow) and the diffusion paths of two free electrons is shown. The schematics of the illustrated preamplifier is shown in the lower left box.

3T-pixel shown in the figure, the signal charge as well as the accumulated charge generated by the leakage current of the collection diode is removed by closing a reset switch after each readout cycle. Correlated Double Sampling (CDS) is used to eliminate the kTC-noise introduced by this reset-procedure and to compute the signal charge.

3T-pixels match the requirements of a modern vertex detector with respect to detection efficiency, spatial resolution and light material budget. However, their radiation tolerance and readout speed remain to be improved. To speed up the readout, the 3T-pixel was replaced by novel architecture named *clamping pixel* allowing for a massive parallel readout concept. This approach accelerates the readout time (and time resolution) of the sensor by a factor equal to the number of (parallel processed) columns of the pixel array (e.g. 10^3). As transporting the related analog data from the chip to external discriminators would require an unrealistically high number of data lines, a zero suppression functionality was integrated into the sensor itself.

The design of this zero suppression circuitry is constrained as standard CMOS processes do not allow for integrating discriminators in the pixels. This follows from the fact that the PMOS-transistors needed for a discriminator require the use of additional N-Well implantations. Those would act as parasitic collection diodes and thus deteriorate the charge collection efficiency of the sensor. To overcome this obstacle, the signals of all pixels in a column are transported to a single discriminator, which is located at the end of the column. Since the discriminators deliver a common threshold for all pixels in a column, pixel-to-pixel dispersions give rise to a so-called fixed pattern noise. In conventional CMOS-sensors, this noise, which is adding to the intrinsic noise of the pixels, is eliminated during offline-processing. To provide an on-chip zero suppression, the related filters (namely the CDS and the leakage current compensation) were integrated into the analog electronics of the pixels [5, 6].

A simplified schematics of the clamping pixel of MIMOSA-26, which performs this analog data processing, is shown in figure 2. Central element of the pixel is a preamplifier, which amplifies

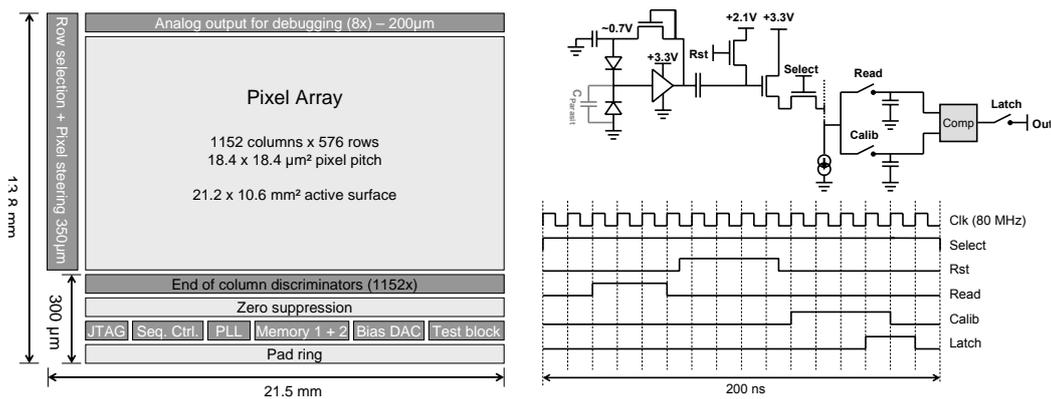


Figure 2. Block diagram of MIMOSA-26 (left). Simplified diagram and readout sequence of MIMOSA-26 (right).

the voltage applied to the parasitic capacity of the reverse biased collection diode. Moreover, it provides the bias voltage of the pixel via its feed-back loop. This allows for compensating the leakage current of the collection diode and for matching its reverse bias actively to the working point of the amplifier. A low pass filter in the feed-back loop ensures that the clearing time of the pixel is reasonably longer than its readout time.

The output of this preamplifier is AC-coupled to a clamping node. The potential of the latter is fixed prior to each readout cycle. This eliminates fluctuations of the dark signal due to the dispersion of the relative resistivity of the collection diode and the biasing circuit. Moreover, variations in the dark level of the preamplifier cancel out. Once the potential of the clamping node is set, the pixels integrate charge, which modifies the potential of the node. The latter is sensed by means of a source follower and sent to the discrimination block aside the pixel matrix.

The functionality of the CDS procedure can be understood from the pixel readout cycle displayed on the lower right panel of figure 2. The cycle starts with reading the potential of the pixel *after* the integration time and charging it into one of the storage capacitors located at the end of the column by closing the “read”-switch. Next, the clamping node is reset and the “calib”-switch is closed in order to store the respective potential as reference voltage into the second capacitor. Given the AC-coupling of the preamplifier to the clamping node, the voltage stored in the “read”-capacitor represents the sum of the signal after CDS-processing and the reset potential of the clamping node. To eliminate latter contribution, the voltage stored in the “calib”-capacitor is subtracted from the one stored in the ‘read’-capacitor in a second step. Provided the reset potential is arbitrary but well reproducible, the output of this procedure is a pedestal corrected CDS-signal, which is “computed” during the readout of the individual pixel. This signal is compared with a threshold, which is common for all pixels. To provide zero suppression, the location of an individual active pixel (or sets of up to four contiguous fired pixels in a row) is encoded in a data word, which is later sent to the outside world via a digital data connection.

The first prototype integrating the full readout chain mentioned above is MIMOSA-26 [6] (see figure 2), which was manufactured in early 2009. The sensor hosts 0.7 million pixels being organized in 1152 columns and 576 rows. The signal of the pixels of one column is multiplexed to

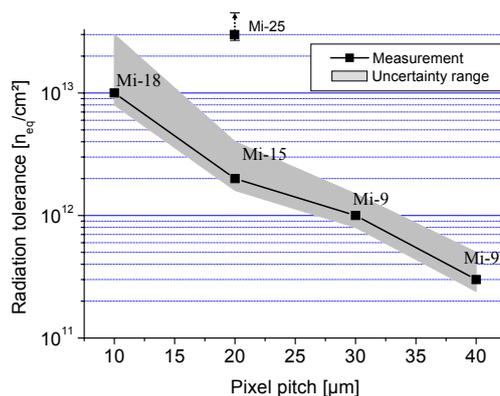


Figure 3. The measured tolerance of MAPS prototypes made with an $0.35 \mu\text{m}$ process to non-ionizing radiation as function of the pixel pitch.

a common readout bus, which is terminated by a discrimination and data sparsification block. The data obtained is sent out of the chip via two differential, digital lines with 80 Mbps each.

The pixel pitch of MIMOSA-26 is $18.4 \mu\text{m}$, which translates into a sensor surface of $\sim 2 \text{ cm}^2$. At nominal clock frequency (80 MHz), the sensor is readout within $115 \mu\text{s}$. This corresponds to a speed up of two orders of magnitude with respect to conventional CMOS-imagers.² The noise at room temperature was measured to be $12 - 13 \text{ e}^- \text{ ENC}$ and the power dissipation is $\sim 0.5 \text{ W}$. Its binary discrimination and data sparsification logic may sense up to nine sets of firing pixels per row.³

3 MIMOSA-26AHR, a radiation tolerant sensor with massive parallel readout

In the past, CMOS-sensors were found to be relatively vulnerable to non-ionizing radiation [7]. This is because the sensors collect the signal charge via the relatively slow thermal diffusion. As the bulk damage caused by non-ionizing radiation reduces the lifetime of free electrons in silicon, it increases the probability that the signal charge is lost because of recombination. This may be compensated by an accelerated charge collection, which may be reached by reducing the pixel pitch and, accordingly, the diffusion path of the electrons (see figure 3). However, this solution is not satisfactory as the smaller pixel pitch requires a higher number of pixels per surface unit, which translates into a higher power consumption and/or a slower readout of the sensor.

The alternative and most natural way to accelerate the charge collection is to deplete the sensors. This approach has been hampered by the high doping concentration found in the epitaxial layers of standard CMOS-process since the doping level limits the depletion depth within reach of the low voltages in those processes ($\leq 5 \text{ V}$) to a fraction of a micrometer. However, this obstacle vanished recently as a new industrial trend made CMOS-processes with a dedicated high

²Note that while a well optimized analog readout line of a conventional CMOS-sensor may handle up to 5×10^7 pixels/s, the more complex readout cycle of the pixels of MIMOSA-26 restricts the performance of the individual end of column readout cells to $\sim 5 \times 10^6$ pixels/s (corresponding to 5.8×10^9 pixels/s in total). The time resolution scales therefore not fully with the number of columns.

³Note that due to charge sharing, a hit tends to generate typically 3-5 fired pixels distributed over 2 or 3 rows.

Epi-layer	S/N (^{106}Ru)
Std-14 μm	20
HR-10 μm	35
HR-15 μm	41
HR-20 μm	36

Table 1. Performances of MIMOSA-26 depending on the type of the epitaxial layer. The uncertainties of the measurements are $\sim 5\%$.

resistivity epitaxial layer commercially available. These novel processes were first explored with the so-called MIMOSA-25 prototype [8], which was manufactured in a $0.6 \mu\text{m}$ high resistivity process. This process features an epitaxial layer with a resistivity of $\sim 1 \text{ k}\Omega \cdot \text{cm}$ but only three metal layers. Due to the latter limitation, the design of the test chips had to be restricted to conventional 3T-pixels with serial analog readout and off-chip hit discrimination. Nevertheless, the results were very promising and a tolerance to $\gtrsim 3 \times 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2$ could be demonstrated. As shown in figure 3, this corresponds to an improvement of more than one order of magnitude with respect to similar designs based on conventional CMOS-processes.

The next step consisted in combining a fast MIMOSA-26 architecture with a high resistivity epitaxial layer. This became possible as the $0.35 \mu\text{m}$ process, in which MIMOSA-26 had been fabricated, became available with a $400 \Omega \cdot \text{cm}$ epitaxial layer. MIMOSA-26 was refabricated on three different wafers featuring epitaxial layer thicknesses of 10, 15 and 20 μm respectively. The performances of the novel sensors, called MIMOSA-26AHR, was compared with the ones of MIMOSA-26 manufactured with conventional, low resistivity, epitaxial layers.

3.1 Tracking performances of MIMOSA-26AHR

The performances of MIMOSA-26AHR were evaluated by measuring the noise and the dark rate of several copies of the chip. Moreover, we studied the charge collection efficiency (CCE) of the sensor with an ^{55}Fe -source and measured its signal-to-noise ratio (S/N) for nearly minimum ionizing particles emitted by a ^{106}Ru -source. This data was complemented by systematic studies of the detection efficiency and the spatial resolution of the sensor, which were carried out with $\sim 120 \text{ GeV}/c$ pions delivered the CERN-SPS.

The results of the measurements performed with the ^{106}Ru -source (see table in figure 1) demonstrate that using high resistivity epitaxial layers improves the performances of the sensors substantially. The results are illustrated with the measured S/N of the sensor, where the signal is represented by the most probable value of its observed Landau distribution. The highest S/N value is found for the sensor with 15 μm thick epitaxial layer (HR-15). The thinner HR-10 sensor and the thicker HR-20 sensor exhibit a smaller S/N but their performance remains above the one of the standard sensor. To understand the maximum observed for the HR-15 sensor, one should be aware that the CCE shrinks with increasing thickness of the active volume. This reflects the stretch of the average diffusion paths of the signal electrons, which increases the probability that charge carriers are lost by recombination. One expects therefore an optimum S/N for an epitaxial layer, which is thin enough to keep a good CCE but sufficiently thick to allow a minimum ionizing particle to generate a sizable signal charge.

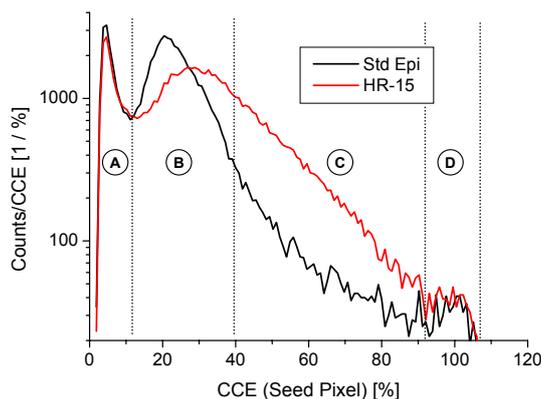


Figure 4. Charge collection spectrum for MIMOSA-26 with standard (Std-Epi) and high resistivity (HR-15) epitaxial layer (see text).

The measurements with the ^{55}Fe -source allowed obtaining a better understanding of the CCE of the sensors. They were performed as following: The chips were illuminated with the 5.9 keV photons of an ^{55}Fe -source and the response of the pixels was measured by sampling the output signal of the 8 analog readout lines of MIMOSA-26 with a 12-bit ADC. Due to the limited speed of those analog outputs, which are for testing and debugging purposes only, the integration time of the sensor was increased to $460\ \mu\text{s}$ during this measurement. All columns of the chip were read out by mapping consecutively groups of 8 columns to the outputs. The data obtained was scanned for hit clusters in an off-line analysis and the signal amplitude of all (by definition 5×5) pixels of the clusters was recorded. By filling a histogram with the signal magnitude of the most significant, central, pixel of the cluster, one obtains a so-called charge collection spectrum (see figure 4), which provides information on the CCE of the pixel. The number of counts corresponding to a certain CCE-value in this histogram can be interpreted as a measure of the fraction of the active volume of the pixel showing this CCE.

The active volume of a standard CMOS pixel can be divided in three sub-volumes. A first and typically very small volume is the depleted area of the pixel, which exhibits a CCE of 100%. Hits recorded in this volume form a small peak located in the zone “D” of the histogram, which is also used for calibrating the CCE-axis. In non-depleted sensors, this volume is separated by a relatively small transition region (related to the relatively poorly populated zone “C” of the histogram) from a sizable volume with reduced CCE (related to zone “B” of the histogram). The latter volume is associated with the non-depleted part of the epitaxial layer, from which the signal charge is collected by means of thermal diffusion. The low CCE part of the “underground” in the histogram and the hits in zone “A” are usually associated to silicon volumes located outside but in the vicinity of the epitaxial layer. Those are partially sensitive to X-rays if their location allows a sizable fraction of the generated signal electrons to diffuse into the epitaxial layer.

By comparing the charge collection spectra of MIMOSA-26 chips with standard and HR-15 epitaxial layer, one observes a substantial shape difference. The difference, though in qualitative agreement with the expectations, departs from them in magnitude when considering the number of counts recorded in zone D of the spectrum. As the lower doping of the epitaxial layer should expand

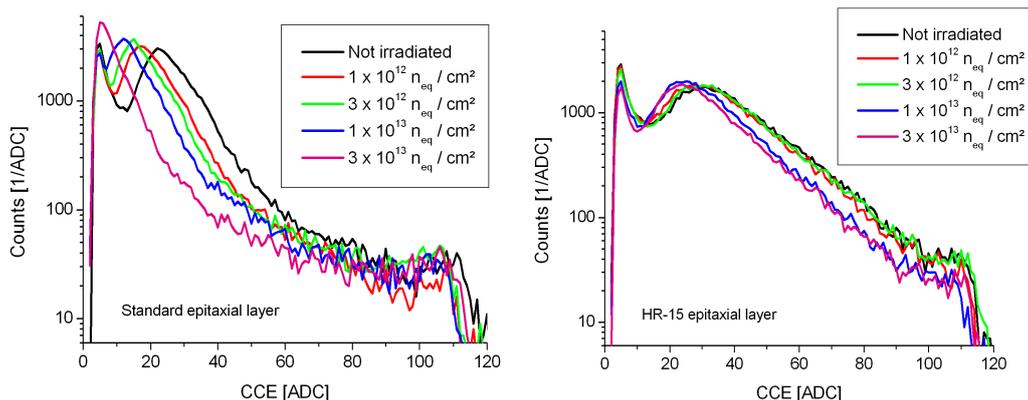


Figure 5. Charge collection spectra of irradiated MIMOSA-26 with standard (left) and HR-15 sensor (right).

the depleted volume of the collection diodes by a factor of up to five, we expected a proportional raise of the number of counts in this zone. Moreover, the expanded depleted volume of the diodes should show a bigger cross-section for collecting diffusing electrons and hence improve the CCE in the epitaxial layer. This should translate into a shift of the peak in zone B toward higher values. Indeed, this shift is observed and complemented by a substantial increase of the number of counts in zone C. However, the observed increase of the number of counts in zone D remains below a few 10%.

Those results are rather unintuitive. They confirm the sizable improvement of the sensor's CCE, which were already seen in the above mentioned measurements with the ^{106}Ru -source. On the other hand, they exclude the predicted origin of this effect, which is the sizable expansion of the depleted volume of the diodes. This raises the questions, why the depleted volume of the diodes did not change and why the CCE was nevertheless improved.

A speculative explanation model considers that the processing of the nearby P-Well implantations accidentally increased the doping level at the vicinity of the collection diode. If so, the rather small depletion voltage of MIMOSA-26 (0.7 V) could be insufficient to deplete this barrier and the volume of the diode would be mostly independent from the doping of the epitaxial layer. The observed increase of the CCE in the epitaxial layer might be caused by electrical fields, which are generated by second order effects such as doping gradients or the presence of the leakage currents of the collection diodes in the “high” resistivity material. Despite a strong charge sharing suggests that the thermal movement of the charge carriers remains dominant, the fields might cause a small drift component in the average movement of the charge carriers. If being oriented toward the collection diode, the latter might enhance the charge collection process quite significantly.

3.2 Radiation tolerance of MIMOSA-26AHR

The good results on the CCE of MIMOSA-26AHR suggest that the novel sensor design provides the ambitious, accelerated, signal charge collection. It was therefore supposed that the HR-sensors would show a substantially improved tolerance to non-ionizing radiation. In order to test this hypothesis, chips with standard and HR-15 epitaxial layer were irradiated with up to $3 \times 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2$

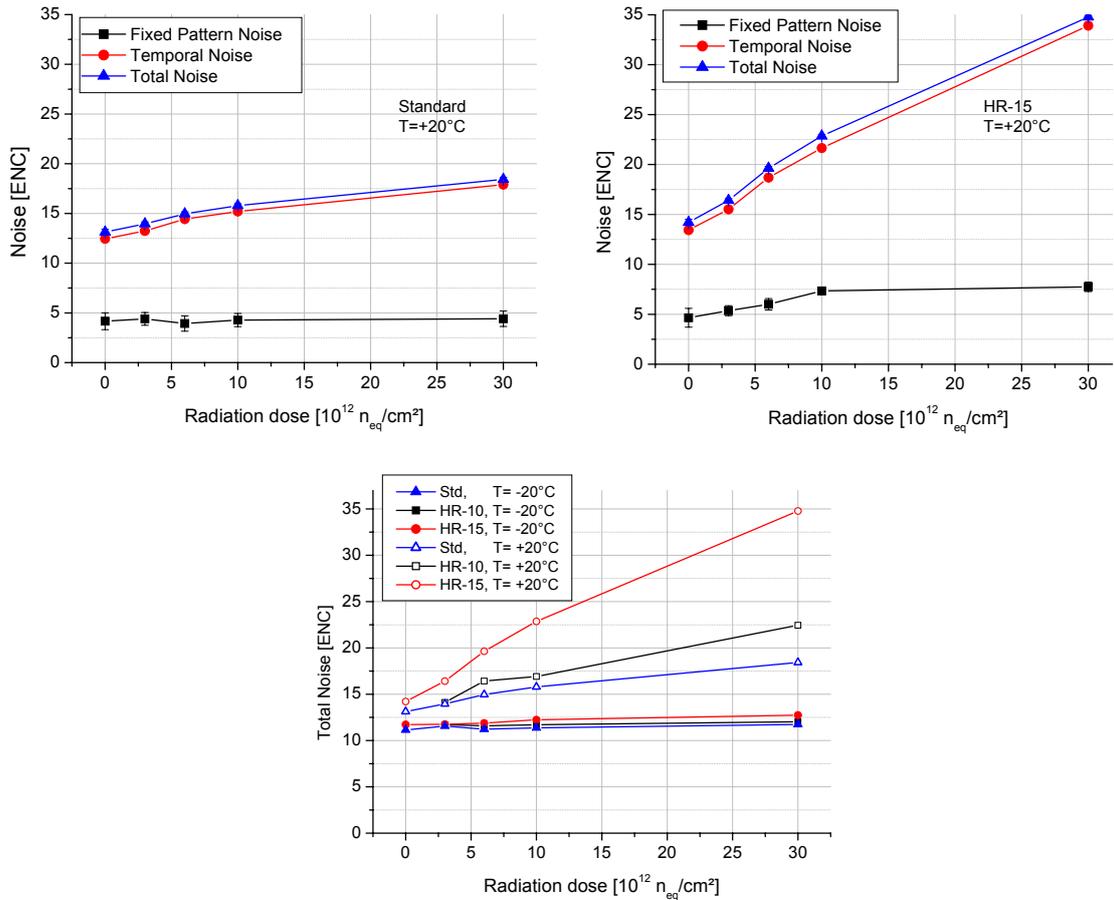


Figure 6. Selected results of the noise measurements with MIMOSA-26 for an integration time of 460 μs . The fixed pattern noise, temporal noise and total noise of the standard and the HR-15 sensors are shown as function of the radiation dose in the upper panels for $T = 20^\circ\text{C}$. The lower right panel displays the total noise of the sensors as function of dose and temperature. If not explicitly shown, the error bars are smaller than the symbols. Note that operating the irradiated sensors at their nominal 115 μs integration time will reduce their temporal noise.

unmoderated fission neutrons at the MEDAPP [9] facility of the FRM II reactor in Garching (Germany). During irradiation, the sensors were not powered in order to minimize the effect of a background of γ -rays, which is estimated to be $\lesssim 100 \text{ kRad}/(10^{13} \text{ n}_{\text{eq}}/\text{cm}^2)$. The irradiated sensors were tested with an ^{55}Fe -source in order to quantify the drop in CCE caused by the non-ionizing radiation damage.

As expected, this drop is quite substantial for the standard sensor (see figure 5 - left). According to our experiences with elder chip designs (see figure 3), we expect the sensor's detection efficiency for minimum ionizing particles to drop below 95% already after a fluence of a few $10^{12} \text{ n}_{\text{eq}}/\text{cm}^2$. The CCE of the HR-15 sensor exhibits a radiation tolerance substantially higher than the one of the standard sensor. This is illustrated in the right panel of figure 5, which shows that the CCE of this sensor is only slightly reduced even after the highest dose applied. This confirms that the goal of accelerating the charge collection in the sensor has indeed been achieved.

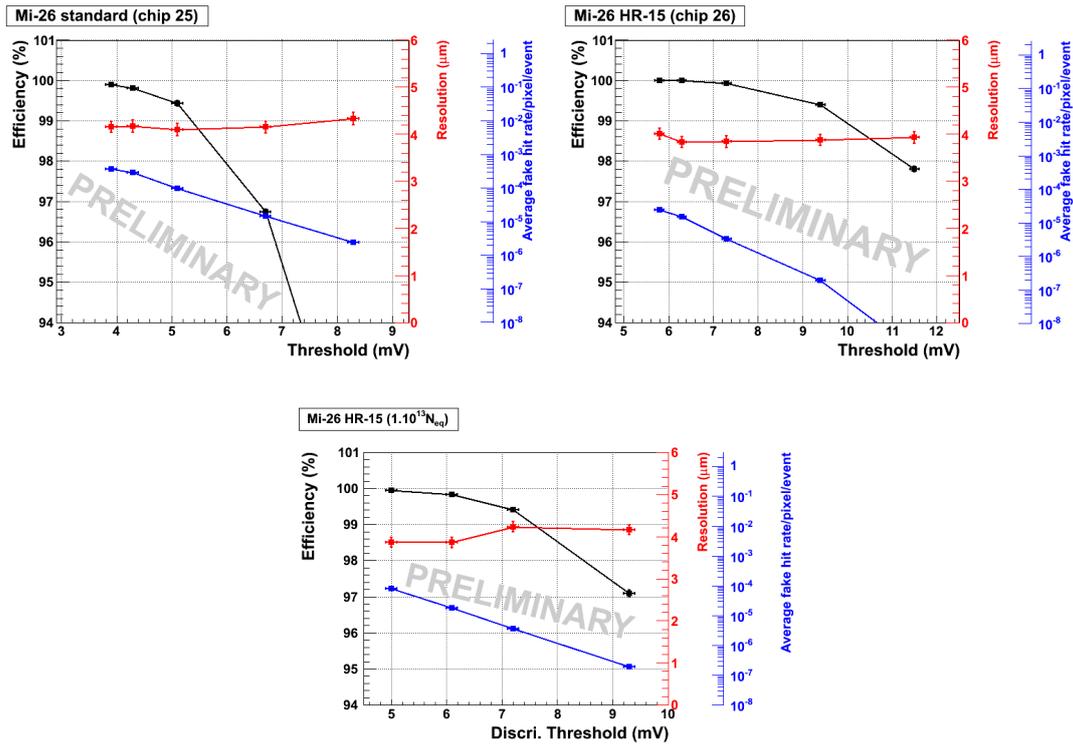


Figure 7. Preliminary beam test results for MIMOSA-26 with standard epi (upper left panel), HR-15 epi (upper right panel) and HR-15 epi irradiated with 10^{13} n_{eq}/cm^2 (lower right panel). It is assumed that the measured spatial resolution of the sensors will approach $3.5 \mu m$ during the final analysis.

Radiation damage is known to increase the leakage currents and the related shot noise of silicon detectors. While the intrinsic leakage current compensation of the pixel of MIMOSA-26 does not allow for a direct measurement of the leakage current, the noise of the detector could be accessed via the analog detector output. To do so, we measured the dark signal and its fluctuations for all individual pixels. The width of the distribution of the *average* dark signal of the individual pixels is associated with a fixed pattern noise as the on-chip discriminators cannot compensate this fluctuation. The fluctuation of the signal of the individual pixel *around its average dark signal* is considered as the pixel temporal noise. In figure 6, the mean value of the temporal noise of all pixels of a sensor is compared with the fixed pattern noise. The total noise is computed as the squared sum of both values, which ignores the small additional noise contribution of the on-chip discriminators of MIMOSA-26. Note that the measurements compare different chips, which adds a systematic uncertainty due to the production tolerances on the analog output circuitry. It seems that this uncertainty causes the observed scattering of the measured fixed pattern noise, which is however dominated by the temporal noise of the pixels.

One observes that the noise of the HR-sensors is slightly higher than the one of the standard sensor. This difference is small for the non-irradiated sensors and for sensors cooled to $-20^\circ C$. Little dependence of the noise on the radiation dose is seen for this operating temperature. For sensors operating at $+20^\circ C$, the noise increases with increasing radiation dose. This holds in particular

for the HR-15 sensor, which might be due to some shot noise caused by a especially high leakage current. This current could exceed the one of the other sensors as the HR-15 pixel has a larger sensitive volume than the HR-10 pixel and a better CCE for thermally generated electrons than the standard sensor. Still, the noise remains acceptable for radiation doses $\lesssim 10^{13}$ n_{eq}/cm², and would have been alleviated if the sensors had been operated with their nominal integration time of 115 μ s.

3.3 Beam test results of MIMOSA-26AHR

MIMOSA-26 was tested with a ~ 120 GeV/c pion beam of the CERN-SPS. The tests were carried out with the TAPI-beam telescope, which combines four MIMOSA-26 sensors with standard epitaxial layer and provides an extrapolated track resolution of ~ 2 μ m. The sensors under test were cooled to a temperature of $\sim 15^\circ$ C (non-irradiated sensors) and $\sim 0^\circ$ C (irradiated sensors) in order to reduce shot noise. All sensors were operated with the digital outputs at their nominal readout time of 115 μ s. The discriminator thresholds were varied in order to identify the best compromise between high detection efficiency and low fake hit rate. The preliminary results of the measurements are shown in figure 7, which shows the measured single point resolution, the detection efficiency and the fake hit rate of the sensors. One observes that according to the preliminary analysis and independently of the radiation dose, all sensors show a spatial resolution of ~ 4 μ m, which is expected to become ~ 3.5 μ m once the analysis is finalized.

The standard sensor provides a detection efficiency of 99.5% in combination with a fake hit rate of 10^{-4} at a threshold of ~ 5 mV. The novel HR-15 sensor provides substantially better S/N performances, which allow for substantially improved separation between real signals and fake hits. This margin can be used for tolerating radiation damage and/or for tolerating the additional noise cause by higher operation temperatures. Moreover, the use of higher discrimination threshold reduces the size of the clusters, which is of interest for applications with high occupancy. For a HR-15 sensor being irradiated with 10^{13} n_{eq}/cm², an efficiency above 99.9% is found in combination with a fake hit rate of 10^{-4} . This supports the statement that even after being exposed to this radiation dose, the HR-15 sensor shows better performances than the non-irradiated standard sensor.

4 Summary and conclusion

Within this work, we developed and tested a CMOS sensor with fast column parallel readout, on-chip data sparsification and digital readout. The sensor was manufactured in a 0.35 μ m process on both standard and high resistivity (400 $\Omega \cdot$ cm) epitaxial layer wafers. We observed that the use of high resistivity epitaxial layer provides substantial benefits in terms of CCE. While this feature would in principle indicate an increase of the depleted part of the sensitive volume, no direct evidence was found to fully support this hypothesis. It is speculated that the improved CCE originates in fact from beneficial changes of second order effects like doping gradients or small currents in the high resistivity silicon, which might generate small, but significant, drift fields in the undepleted part of the epitaxial layer.

Due to the higher CCE, the HR-sensor shows a twice higher S/N than the standard sensor (S/N ≈ 40 instead of ≈ 20 , tested with beta rays of a ¹⁰⁶Ru-source). Moreover, unlike known from standard sensors, the CCE of the HR-sensor remains mostly stable after bulk damage consecutive to a fluence $> 10^{13}$ n_{eq}/cm². During a beam test performed at 0°C with 120 GeV/c pions at

the CERN-SPS, the HR-15 sensor irradiated with 10^{13} n_{eq}/cm² demonstrated an efficiency above 99.9% in combination with a fake hit rate of 10^{-4} , which exceeds performances of a non-irradiated standard sensor. With this result, it has been demonstrated that one may fabricate CMOS sensors with a fast and column parallel readout adapted to fluences $> 10^{13}$ n_{eq}/cm².

Acknowledgments

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