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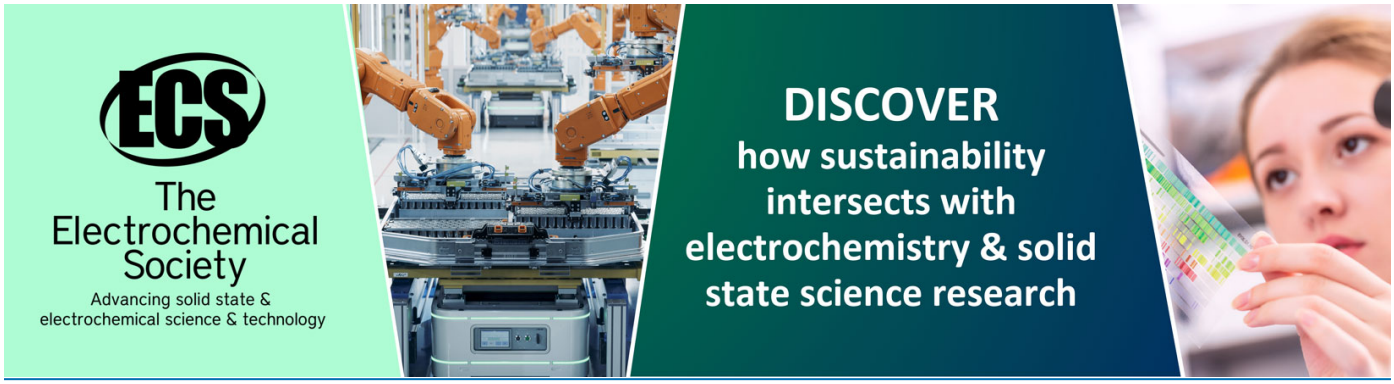

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SAMPA Chip: the New 32 Channels ASIC for the ALICE TPC and MCH Upgrades

J. Adolfsson,[a] **A. Ayala Pabon,**[b] **M. Bregant,**[c,1] **C. Britton,**[d] **G. Brulin,**[e] **D. Carvalho,**[b] **V. Chambert,**[e] **D. Chinellato,**[f] **B. Espagnon,**[e] **H.D. Hernandez Herrera,**[b] **T. Ljubicic,**[g] **S.M. Mahmood,**[h] **U. Mjörnmark,**[a] **D. Moraes,**[i] **M.G. Munhoz,**[c] **G. Noël,**[e] **A. Oskarsson,**[a] **L. Osterman,**[a] **A. Pilyar,**[j] **K. Read,**[d] **A. Ruette,**[f] **P. Russo,**[e] **B.C.S. Sanches,**[b] **L. Severo,**[b] **D. Silvermyr,**[a] **C. Suire,**[e] **G.J. Tambave,**[k] **K.M.M. Tun-Lanoë,**[e] **W. van Noije,**[b] **A. Velure,**[k] **S. Vereschagin,**[j] **E. Wanlin,**[e] **T.O. Weber**[l] **and S. Zaporozhets**[j]

[a] *Department of Physics, Division of Particle Physics, Lund University, Box118, SE-22100 Lund, Sweden*
[b] *Escola Politécnica da USP, São Paulo, Brazil*
[c] *Instituto de Física, USP, rua de Matão 1371, São Paulo, Brazil*
[d] *Oak Ridge National Laboratory, Oak Ridge, TN 37831, United States*
[e] *Institut de Physique Nucléaire d'Orsay (IPNO), Université Paris-Sud, CNRS-IN2P3, Orsay, France, 15 rue Georges Clemenceau, 91406 Orsay (France)*
[f] *Instituto de Física Gleb Wataghin, UNICAMP, R. Sérgio Buarque de Holanda, 777, Campinas, Brazil*
[g] *Brookhaven National Laboratory, Upton, NY 11973, United States*
[h] *University of Oslo, P.O. Box 1048, Blindern, NO-0316 Oslo, Norway*
[i] *Instituto Tecnológico de Aeronáutica, ITA, Sào José dos Campos, Brazil*
[j] *Joint Institute for Nuclear Research, Joliot-Curie 6, Dubna, Moscow region, Russia*
[k] *University of Bergen, P.O. Box 7800, NO-5020 Bergen, Norway*
[l] *Departamento de Computação, UFSC Campus de Araranguá , Rua Pedro João Pereira, 150, Araranguá, SC, Brazil*

E-mail: bregant@if.usp.br

[1] Corresponding author.

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Abstract: This paper presents the test results of the second prototype of SAMPA, the ASIC designed for the upgrade of read-out front end electronics of the ALICE Time Projection Chamber (TPC) and Muon Chamber (MCH). SAMPA is made in a 130 nm CMOS technology with 1.25 V nominal voltage supply and provides 32 channels, with selectable input polarity, and three possible combinations of shaping time and sensitivity. Each channel consists of a Charge Sensitive Amplifier, a semi-Gaussian shaper and a 10-bit ADC; a Digital Signal Processor provides digital filtering and compression capability. In the second prototype run both full chip and single test blocks were fabricated, allowing block characterization and full system behaviour studies. Experimental results are here presented showing agreement with requirements for both the blocks and the full chip.

Keywords: CMOS readout of gaseous detectors; Front-end electronics for detector readout; Analogue electronic circuits

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1 Introduction

ALICE (A Large Ion Collider Experiment) is one of the four big experiments at the LHC accelerator. The experiment's main goal is to study the strongly interacting matter and the quark-gluon plasma produced at the high energy density and temperature that relativistic heavy ion collisions make available. Presently the ALICE detector complex is handling well the high particle multiplicity conditions of a central Pb-Pb collision, but its acquisition rate (all detectors) is limited to few hundred Hertz by a design that traded off acquisition rate for the capability to maintain good tracking and identification capabilities, down to particle momentum as low as few hundred MeV, even for high particle density. Starting from 2021, after the LHC second long shutdown, a higher luminosity, and consequently higher event rate, will be provided by the accelerator. It is in the interest of ALICE physics to profit from this higher luminosity, therefore ALICE detector layout was revised and an upgrade plan was set. One of the most important point of the upgrade plan is related to the TPC, where the present tracking performance should be maintained, but the read-out capability should be improved by two orders of magnitude, allowing operation at 50 kHz event rate in Pb-Pb runs. To achieve that, the actual Multiwire Proportional Chamber (MWPC) readout plane will be replaced by a Gas Electron Multiplier (GEM) plane; the front-end electronics need to be replaced, too. A new ASIC, named SAMPA ([1]), was developed to serve both the TPC and the Muon Chambers [2]. The new chip is required to provide 32 channels, each integrating a pre-amplifier and an ADC, as well as to have digital processing capabilities to supply baseline compensation and signal filtering to reduce the data size. While the new TPC read-out plane is based on GEM detectors, the MCH will still use MWPC; the two detectors have different requirements, and the table 1 shows the main specifications for the two cases.

Table 1. Original specifications of the front-end ASIC (SAMPA).

Specification	**TPC**	**MCH**
Voltage supply	1.25 V	1.25 V
Polarity	Negative	Positive
Detector capacitance (Cd)	18.5 pF	40 pF–80 pF
Peaking time (ts)	160 ns	300 ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 600 e@ts = 160 ns*	< 950 e@Cd = 40 pF* < 1600 e@Cd = 80 pF*
Linear Range	100 fC or 67 fC	500 fC
Sensitivity	20 mV/fC or 30 mV/fC	4 mV/fC
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts = 160 ns	< 0.2%@ts = 300 ns
ADC effective input range	2 Vpp	2 Vpp
ADC resolution	10-bit	10-bit
Sampling Frequency	10 (20) Msamples/s	10 Msamples/s
INL (ADC)	< 0.65 LSB	< 0.65 LSB
DNL (ADC)	< 0.6 LSB	< 0.6 LSB
ENOB (ADC)**	> 9.2-bit	> 9.2-bit
Power consumption (per channel) CSA + Shaper + ADC	< 15 mW	< 15 mW
Channels per chip	32	32

*R_{esd} = 70 Ω
** @ 0.5 MHz, 10 Msamples/s

2 The SAMPA chip

The SAMPA chip provides 32 channels, as illustrated in figure 1, each is composed of an analogue front-end part followed by an ADC; a common digital processor completes the chip. SAMPA is designed and fabricated in 130 nm TSMC CMOS technology and it operates at a nominal supply voltage of 1.25 V.

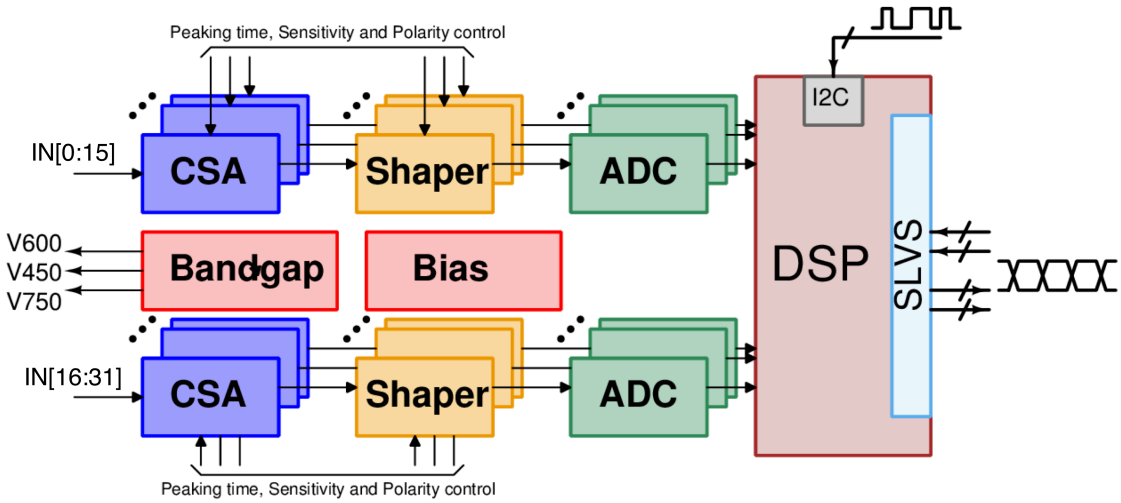

Figure 1. Sampa block diagram.

2.1 Analogue front-end

A Charge Sensitive Amplifier (CSA), followed by two shapers and a non-inverting stage compose the SAMPA front-end (see [1] and [2] for more details, and [4] for a full description). The CSA is capable to accept and to amplify either positive or negative charge pulses. The first shaper provides the first two poles and one zero of the shaping chain, while the second shaper, fully differential, implements a second order bridged-T filter. A non-inverting stage (NIS) is placed between the second shaper output and the ADC input to adapt the DC voltage level and to allow, in such a way, to use the full dynamic range of the ADC. In order to improve the noise figure the CSA implements a modified cascode topology (full details in [3] and [4]), providing a relatively flat minimum in the region of the expected detector capacitance. In addition, both CSA and the first shaper are connected to a power domain that is isolated from the power domain used for the second shaper and the NIS. Then, the ADC is connected to a third, independent power domain. That is aimed at reducing the switching noise coupling from the ADC to CSA. The front-end circuits require three reference voltages (450, 600 and 750 mV), which are internally generated by a band-gap.

2.2 The digitization stage

Each of the 32 SAMPA channels chain includes its own 10-bit capacitive successive-approximation (SAR) ADC. The converter is optimized to operate at 10 MSps, but it is capable to be operated up to 20 MSps. The ADC is using a split capacitor 3:7 array topology and implements a low energy switching technique (as from [5]). An external, stable, reference voltage of 1.1 V is required to operate the ADC, and it defines the range and the conversion factor of the system.

2.3 Digital and communication part

After leaving the ADC, the data can follow two alternative paths: be processed by the DSP or be sent out in the direct ADC mode.

In the direct ADC mode the chip sends out the data directly, unprocessed, via ten 320 Mbps eLinks. Two schemes were implemented: 1) the 32 channels values are sent out as 10 parallel bits word in 32 consecutive 320 MHz clocks; 2) the first 5 e-links send, split in two words of 5 parallel bits, the data of the first half (ch 0–15) of the chip, while the e-links 5–9 send out data of the second half (ch 16–31) of the chip. This second option is needed when an odd number of SAMPA chips is connected to an even number of higher level chips, as it is the case of the TPC front-end, where 5 SAMPAs are connected to 2 GBTx. Since in the direct ADC mode the data is not packaged with a header, the eleventh eLink is used to guarantee the synchronism of the data.

In order to process the data a set of 4 independently selectable (and configurable) filters are made available:

- Baseline Correction 1 (BC1), an infinite impulse response (IIR) filter to cope with slow baseline variations;
- Digital Shaper (DS), aimed at tail cancellation;
- Baseline Correction 2 (BC2), moving average filter aimed at tracking and removing fast variations in the baseline;

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- Baseline Correction 3 (BC3), alternative filter, based on limited slope baseline tracking, to complement and/or substitute the functions of BC1 and BC2 with a more robust approach.

The digital section includes also blocks to implement zero suppression, data compression (Huffman coding), pre-sampling (in case of triggered mode) and data formatting. In case of very low data rate, as the case of MCH, there is the possibility to daisy chain SAMPA chips, so that a single eLink is used to send out data of many chips (presently MCH front-end is planning to concatenate two SAMPAs). A clock manager provides and sincronizes clock signals for the full chip. The slow control (configuration) of the SAMPA is performed via a standard I2C interface integrated on the chip.

The digital part is very complex, and its input is not (fully) accessible for testing, therefore any attempt of functional test will provide a very little fault coverage of the DSP. To provide a better fault coverage and to be able to verify whether the digital part was fabricated correctly and without error, the Design for Test (DFT) technique was applied. The chip can be configured in test-mode, then test vectors, which were developed to provide a fault coverage higher than 96%, are fed and read back via the eLinks, the output is compared with the expected value.

3 Experimental results

The big area ($9.6 \times 9\,\mathrm{mm}^2$) of the SAMPA chip makes Multi-Project run as expensive as a dedicated engineering run. Therefore it was decided to go for the second option, a Multi-Layer-Mask process was chosen, producing 12 wafers of 8 inches size, each wafer containing approximately 180 unitary cells. Each unitary cell contains a full SAMPA prototype, and three-test chips. The first test-chip (chip_1) contains the test block of SLVS drivers and others sub-blocks; the second test-chip (chip_2) contains a complete replica (32 channels) of the analogue front-end implemented on SAMPA; the third test-chip (chip_3) contains an ADC block standalone. Other development project circuits complete the filling of the available area. The chip_1 was used to verify SLVS drivers; eye diagram was found well open even at transmission frequency twice the nominal 320 Mbps; fall and rise time are stable and in the order of few hundred picoseconds in all conditions and configurations.

3.1 Characterizing the analogue Front-End

The chip_2 die was directly mounted and wire-bonded on a test board. The 1.25 V needed to power the chip was provided directly from an external power supply, while the three reference voltages used for the buffer (450 mV, 600 mV and 750 mV) were generated internally by the circuit band-gap. Input charge stimulus was created by applying a voltage step across a known capacitor (usually 1 pF) connected in series with the input. A differential probe was used to collect the output by an oscilloscope. Visual inspection of the shape of the pulse never showed anomalous behaviours, besides a small undershoot, in some samples, in the baseline restoration for the high gain (20 mV/fC and 30 mV/fC) configurations. Measured peaking time was found well on target, being around 165 ns for the 160 configurations, and 305 ns for the 300 configuration. To measure sensitivity and linearity a complete scan of the dynamic range was performed, taking care to collect more injected charge points at the beginning and at the end of the range, to better evaluate non-linearities for low and high injected charge. For each injected value about one thousand waveforms, in average mode, were collected. The response of the circuit was defined as the peak value (as computed by the

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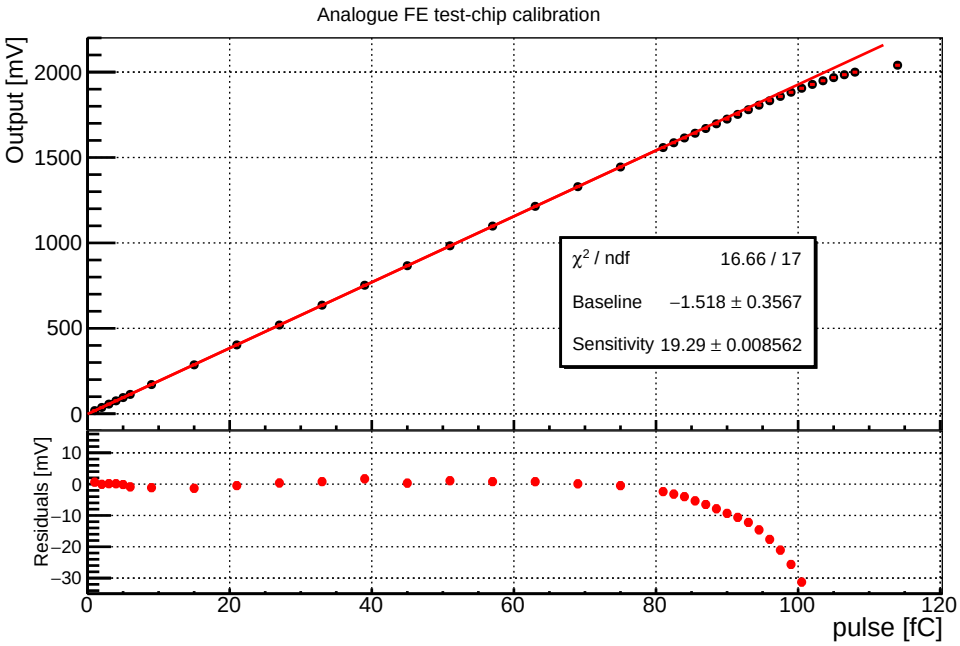

Figure 2. Analogue front-end test-chip: a calibration curve for the configuration 20 mV/fC.

oscilloscope) minus the baseline, defined as the average value of the output in the case no charge is injected. The response of the front-end is completely linear, with residuals below 2 mV (non-linearity < 0.1% of the full range) up to about 80% of the range, and remains linear (non-linearity < 0.5% of the full range) up to about 90% of the range. Figure 2 presents an example of response curve measured in a front-end test-chip.

The noise was evaluated computing the rms value in absence of input signal over a time of 50 μs, averaging over about 1000 waveforms. The oscilloscope and the differential probe add a noise contribution that is of the same magnitude as the chip noise. This contribution was estimated taking data with the probe connected, but keeping the chip powered off; the value obtained was then removed quadratically from the measurement performed with the chip powered. The Equivalent Noise Charge (ENC) was then computed using nominal gain. The variation of the noise with the capacitance in parallel with the inputs was measured using a set of pre-calibrated capacitors. During the measurement all the channels were loaded with approximately the same capacitor values. Figure 3 shows an example of noise vs capacitance curve, presenting the ENC for different channels of one of the tested front-end samples.

The chip was tested mainly powered at nominal voltage, 1.25 V, but several tests were performed also at the lowest (1.19 V) and at the highest (1.31 V) limit. Operating at lower voltage does not show any alteration in the chip behaviour, besides reducing the dynamic range. When operated at the higher voltage the chip behaves well and no issues were spotted so far.

3.2 Characterizing the ADC

The chip_3, which contains a 10 bit SAR ADC circuit, was, too, mounted directly on a dedicated test-board. The ADC was operated at the nominal frequency of 10 MHz, provided by an external

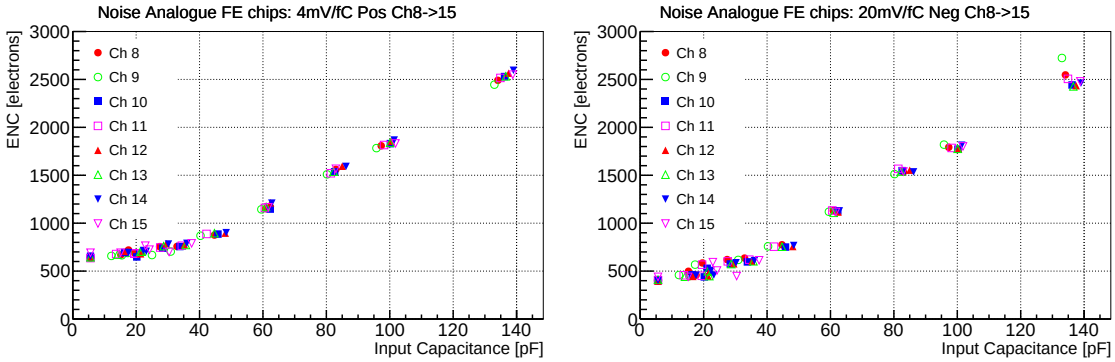

Figure 3. Noise, expressed in ENC, for 4 mV/fC (left) and 20mV/fC (right) configurations in various channels of one of the analogue front-end test-chip sample. ENC was calculated using nominal gain.

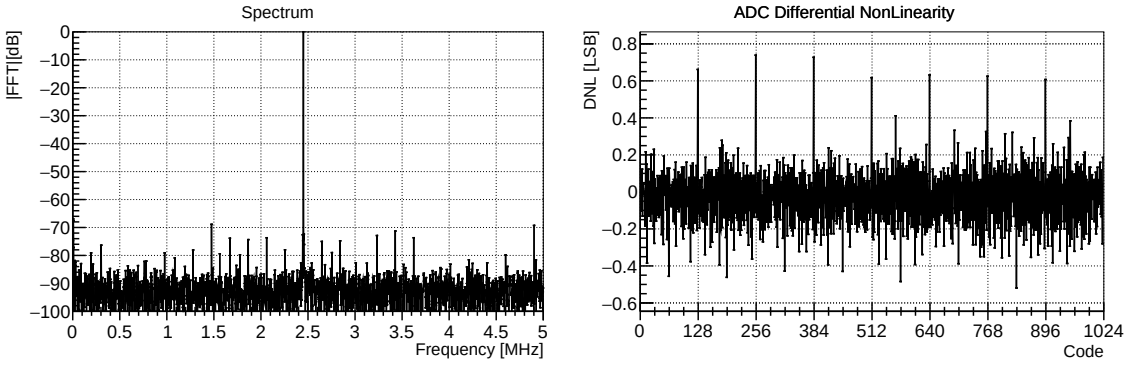

Figure 4. Measured performance of SAMPA prototype_2 ADC at 10 MSps: spectrum in presence of 2.45 MHz sine wave (left), Differential Non-Linearity (DNL) in the same conditions (right).

function generator. The 10 bits output was read out as a parallel word by a logic analyser. Three ADC test-chip samples were tested until the moment of submission of this paper. First the ADC were stimulated with different types of slow varying (1 kHz) signals, like ramp, sine wave, etc., looking for evident problems of non-linearity. Later a sine wave with frequency values ranging from 400 kHz to 4.7 MHz was used, and SINAD, SFDR and ENOB were computed. The equivalent number of bits, measured at 2.45 MHz, resulted below 9.2 (e.g. figure 4, left). Similar values were obtained for the measurements at the others stimulus frequencies. Tests also showed some pattern appearing in the DNL plot (figure 4, right) in correspondence of transition of bit 7 (code 128 and multiples). The most probable cause for both low ENOB and high DNL for some specific codes seems to be a too high parasitic capacitance, which affects the split capacitor array. This hypothesis is being verified in a forthcoming Multi-Project run, where a different layout, more robust against parasitics, is implemented for the capacitor array

3.3 Characterizing the full chip

The performance of the full chip was measured on a test board connected to a FPGA development kit board. The FPGA handles the communication with the chip, and allows to extract the stream of data coming from the SAMPA outputs. The test here reported were performed with the bare

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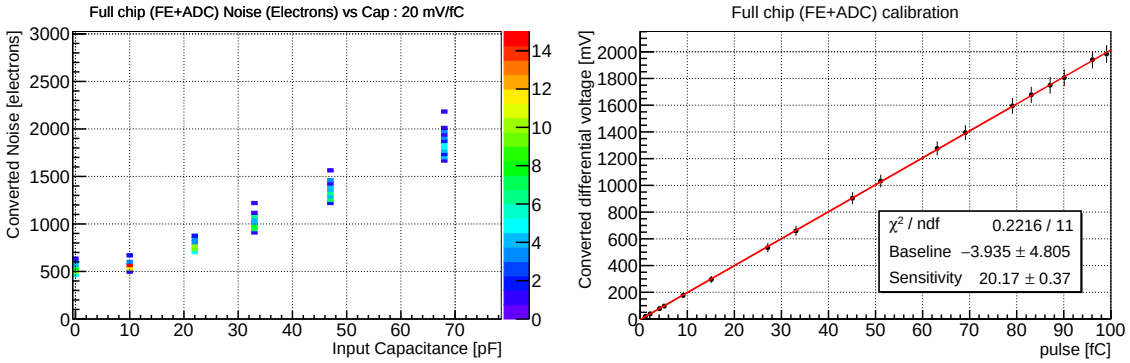

Figure 5. An example of full chip results, configuration 20 mV/fC. Left, noise, expressed in ENC (assuming nominal gain), colors represent number of channels in a noise bin. Right, a calibration curve. In both cases ADC values were converted using the nominal 2.15 mV/LSB factor.

die directly bonded on the board. The test strategy was the same as for the analogue front-end, measuring the noise as function of input capacitance and reconstructing the shaped pulse amplitudes when a charge pulse is injected in the input.

Data taking was performed in direct ADC mode, without activating any filtering in the DSP. The results (figure 5 shows an example) overlap well with the findings in the analogue front-end test-chips. The linearity is very good, and the noise, in the required detector capacitance range, is compatible with the measurements performed on the analogue test-chips, once the contribution of quantization noise is taken in account. The noise measurements were extended well above the values expected in the experiment, proving the stability of the system. For higher capacitance (above specifications range), the noise in the full chip is growing faster than in the front-end standalone, and with higher dispersion across channels. This behaviour is presently being investigated.

4 Conclusions

The SAMPA ASIC is designed to fulfil the needs for a new faster readout of the Time Projection Chamber and Muon Chamber of the ALICE experiment.

The second prototype run included both the first full size (32 channels), fully operating, SAMPA and test-chips to study and validate the single sub-blocks.

The test of the analogue Front-End test-chip (32 channels block of CSA followed by two shaper stages) proved this part is working fine and well inside the specification for both the TPC (20 and 30 mV/fC with 160 ns shaping, negative charge input) and MCH (4 mV/fC, 300 ns shaping, positive charge input) configurations.

The tests of the 10 bit SAR ADC test-chip showed an overall good linearity, but with a slightly low ENOB value and with some high DNL for some specific codes. The two issues appear to have same origin, related to parasitic capacitances in the DAC capacitor array, and are being addressed.

Tests performed in the full chip showed a good linearity and a low noise level, in line with specifications. In the required detector capacitance range, performance are comparable with the results of the analogue front-end standalone block, once read via a linear ADC. The integration of analogue and digital blocks in the same chips appears to add some extra noise, nevertheless the total

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noise remains low. This indicates the caution posed during the integration to isolate analogue and digital part of the chip allowed to tame the effects of a potentially destructive noise injected from the digital circuit into the sensitive amplifier. The SAMPA is capable to run in continuos mode, amplifying, digitizing and sending out the digitized values, all at the same time, without affecting the quality of the measurement.

The SAMPA chip is basically completely functional, therefore next step consists in just fixing the minor flaws that deteriorate the ADC performance.

Acknowledgments

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