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To cite this article: F Feinstein and E Delagnes 2007 *J. Phys.: Conf. Ser.* **60** 284

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# Concepts and trends for front-end chips in astroparticle experiments

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**Abstract.** We review recent application specific integrated circuits developed for high energy neutrino, gamma ray and cosmic ray detectors, which share constraints of the same kind. We compare various technical concepts used to fulfil similar requirements. We suggest some ways which could be followed in the near future to answer the needs of next generation experiments.

## 1. Introduction

Present astroparticle experiments such as ICECUBE and the future submarine neutrino telescopes, HESS and the future large gamma ray observatories, AUGER and other air shower arrays are modular, consisting of thousands of channels distributed over large surfaces or volumes. They require high dynamical range for a correct energy measurement. Rare events have to be extracted from a background which rate is several orders of magnitude higher. To minimize the resulting dead time, they use fast sensors such as photomultiplier tubes or hybrid photodiodes. Their design has also to ensure a reasonable cost and minimal repairs or losses.

All these conditions result in constraints which have led the various experimental groups to build a front-end electronics based on application specific integrated circuits (ASIC). These circuits are indeed a cost effective alternative to designs based on discrete components, with equal or better performances and a higher reliability.

## 2. Standard requirements for front-end electronics

All these detectors use Cherenkov or fluorescence light detection. The typical rise time of the resulting signal is of the order of 2 ns to 3 ns. A 300 MHz analogue bandwidth marginally widens the signal.

Trigger rates reach from several kHz for atmospheric Cherenkov telescopes, up to few 100 kHz for underwater neutrino telescopes. This requires a readout dead time from 200  $\mu$ s to 1  $\mu$ s.

As the amplitude calibration is obtained from single photo-electron measurement, the dynamical range must start at about 1/10 photo-electron, while the highest signals may reach up to 5000 photo-electrons, leading to a 1 to 50000 dynamical range. This is obtained using several gains for each channel. In this case the cross-talk must be limited to a few per mil.

The power consumption per channel is limited either by the extension of the arrays such as in AUGER and ICECUBE, the need to evacuate the heat from the HESS cameras, and in general the remoteness of the sites. Moreover, low power consumption usually goes together with high reliability.

Integrating more functions in the ASIC helps limiting the cost and the power consumption. Various parameters of the chip can be controlled digitally by the means of several integrated DACs. The signal digitization can be performed with internal ADCs.

Finally, the digital output can be minimized by integrating some logics to analyze the pulse shape and compress the data for simple shapes.

### 3. Dynamical range

The general approach to achieve the typical 16-bit dynamical range is to get it by parts by splitting the signal on two or three channels with different gains and overlapping ranges. A circuit developed for the front-end of AUGER northern site performs signal duplication with three gains : 0.15, 1 and 6.2 [1]. With a 10 bit fast ADC, the effective dynamical range is 16.6 bits with 60 MHz analogue bandwidth.

ICECUBE [2] and ANTARES [3] have chosen to read the anode and two attenuated channels of their photomultiplier tubes. In the HESS 2 camera, the anode signal is duplicated with two gains of 1 and 25. With almost 12 bits dynamical range per channel, the effective dynamical range reaches 16 bits.

### 4. Sampling and digitization techniques

Signal sampling at a frequency about 5 times higher than the analogue bandwidth is an alternative to standard integrated charge and time measurements. It allows an optimal signal to noise separation. Flash ADC technique is widely used for such purpose. However, it has some drawbacks such as its cost, power consumption, limited maximal frequency and dynamical range.

#### 4.1. Switched capacitor arrays used as transient recorders

The signal can be sampled by an array of switched capacitors which is started by an external trigger. The effective time between each sample is the time it takes to propagate the switch command from one cell to the next one. This technique provides GSample/s rate without any high speed clock. The signal samples are stored in the array, ready to be digitized at a much lower frequency. This has been implemented successfully in the Analog Transient Waveform Recorder (ATWR) and its successor the ATWD [4] which are used by the AMANDA and ICECUBE experiments.

#### 4.2. Switched capacitor arrays used as circular buffers

The switch capacitor array can also sample continuously the signal until stopped by an external trigger. Once the last cell is written, it overwrites the first one. The array memorizes the past information in the N-1 cells. This gives a delay which is the product of the sampling period and the array depth, typically 120 ns for a 128-cell array and 1 GHz sampling rate. It can be used to build the trigger that will stop the array, saving a delay line for the analogue signal. The sampling rate is often controlled by an external clock running at the sampling rate divided by the array depth, 8 MHz in our example.

The ANTARES experiment implemented first this technique in the Analogue Ring Sampler (ARS0 and ARS1) [5]. The ARS0 was also used in the four HESS 1 cameras [6]. The Domino Ring Sampler (DRS) [7], developed for the MEG experiment, uses a similar technique. The Large Analog Bandwidth Recorder and Digitizer with Ordered Readout (LABRADOR) [8], developed for the ANITA experiment, differs slightly in the fact that the switch command wraps back to the beginning of the array in a time interval covered by four specific cells. In most applications, the sampled signal occupies only a small fraction of the array, the rest of the depth is used as a delay.

In all the previously mentioned arrays, the cells are arranged in a linear architecture, often a source of fixed pattern noise. The analogue bandwidth is limited by the number of capacitors connected to the input buffers. The positioning of the read pointer along the line may cause some extra dead time. The MATAcq circuit [9] uses a matrix of 20 x 128 cells allowing a very uniform response over the whole memory. It is implemented on an commercialized VME board, providing a very compact and versatile fast acquisition system, working up to 2 Gsample/s, with a 300 MHz analogue bandwidth.

The new HESS 2 telescope will trigger at a much higher rate than HESS 1, incompatible with the ARS0 dead time. Moreover the analogue bandwidth of the ARS is limited to 80 MHz and forces to use a long integration window, increasing the night sky background focused by the large HESS 2 mirror. A new circuit, the Swift Analogue Memory (SAM) [10] has been designed. It is a 16 x 16 cell matrix, working up to 2 Gsample/s, with a 300 MHz analogue bandwidth. The readout time of 16 cells has decreased from 275  $\mu$ s for the ARS to 1.5  $\mu$ s for the SAM.

#### 4.3. Cell readout and digitization

The simplest digitization technique, used for DRS and SAM, consists in using an external fast ADC to read the memory serially. Each SAM cell is digitized in 90 ns by a 12 bit-ADC. A cheaper but slower solution used in the ARS1 is to integrate the ADC, leading to 1.5  $\mu$ s readout and conversion per cell.

The ATWD and the LABRADOR integrate common ramp Wilkinson ADCs which digitize all the cells in parallel. The dead time is governed by the ramp speed, typically 40  $\mu$ s, and the digital readout, also about 40  $\mu$ s. The fast ADC is the most efficient solution if only part of the memory is read out.

### 5. A system on a chip

The ARS1 circuit [11] used by ANTARES, integrates several original functions to minimize dead time, which make it a real system on a chip.

#### 5.1. Data compression

Most signals have a simple, standard shape. The ARS1 contains an analogue pulse shape discriminator to distinguish them from large, wide or multiple pulses. This allows to measure and transmit only the arrival time and the integrated charge of the standard pulses and transmit the sampled shape only for complex pulses, thus reducing dead time and data flow.

#### 5.2. Derandomization

The time distribution of random events follows a Poisson law and is the cause of dead time. The ATWR and the ATWD are used in pairs in a flip-flop mode. When one chip is in dead time, the second one takes over, thus squaring the dead time. The ARS1 uses the same mechanism. A 16-cell mixed analogue and digital FIFO, stores the charge, time and time stamp of standard pulses before digitization. The combination of the derandomization and data compression gives for standard pulses a drastic dead time reduction down to 0.2  $\mu$ s, as long as the event rate is lower than the digitization rate.

### 6. Present and future performances

In the following table, we compare the most meaningful characteristics of the chips discussed above.

Function \ Chip name	ATWD	ARS1	DRS	LABRADOR	MATACQ	SAM
Power (mW)	150	500	50	50	1000	300
Sampling range (GS/s)	0.00005-2	0.3-1.2	0.7-2.5	0.5-3.5	1.-2.	1.-2.
Analogue BW (MHz)	350	80	400	600	300	250
sampling freq. servo control	no	yes	yes	no	yes	yes
jitter at max. freq. (ps)	?	< 50	80	?	< 60	< 50
Number of cells	128	128	1024	260	20x128	16x16
Number of channels	4	4	10	9	1	2
Dead time ( $\mu$ s)	100	0.2 or 180	256	150	160	0.09 / cell
Total noise RMS (mV)	1	4	2	?	< 0.2	0.7
Maximum signal (V)	3	3	1	?	+/- 0.5	2
Dynamic range	2500	750	500	1000	5000	3000
Crosstalk (%)	?	5	?	?	-	< 0.3
Technology ( $\mu$ m)	1.2	0.8	0.25	0.25	0.8	0.35
ADC in chip	yes	yes	no	yes	no	no

Readout dead time is a key parameter. Derandomization, data compression, internal digitization and matrix structure are efficient options to reduce it. With more integrated technologies, the future of derandomization may be to group two or more chips on the same die, to simplify the passing of a token ring. Common ramp Wilkinson ADCs suffer from a rather slow conversion time. A new Wilkinson ADC initially developed to be integrated in the SAM has been successfully tested to perform 12 bit conversion in 1.2  $\mu$ s. After digitization, an extra dead time comes from data readout. An internal FIFO could smooth out the data flow and free the chip as soon as digitization is performed. These improvements could make possible acquisition rates up to a few 100 kHz with a negligible dead time.

Consecutively, need for data compression will grow. It could be performed by integrating some programmable logics to perform digital treatment which is presently done outside the chip, such as summing the samples, finding the time of the maximum or the width of the signal.

Memory depths can be increased to allow for global array trigger building. Versions of the SAM with 1024 cells and of the LABRADOR with 64 k-cells are foreseen.

## 7. Conclusions

In the last ten years, front-end samplers have improved drastically. Dead time has gone down from several 100  $\mu$ s to a few  $\mu$ s. Dynamical range has increased from 8 bits to 12 bits. The integration of ADCs has become the norm. Soon, with 0.35  $\mu$ m and 0.25  $\mu$ m technologies being widely used, more digital treatment will be integrated, offering powerful online signal processing and data compression. We have all reasons to believe that front-end chips will be a cornerstone of future astroparticle experiments.

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