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Abstract. Aiming at the problems of using optocouplers to achieve logic level matching in the current communication circuit, there are many components, high cost, and high requirements for component parameters. Based on the basic requirements of circuit logic level matching, this paper combines The research on the basic principle of triode switch, using the Schottky diode's unidirectional conduction and low conduction voltage drop characteristics, introduces a logic level matching circuit for inter-module communication with switch isolation function in communication circuits. Through the verification of relevant experiments such as functionality, stability and reliability, the circuit has a simple structure and stable performance, and is very suitable for use in communication circuits between modules of different voltage levels.

1. Introduction

With the rapid development of communication technology and microelectronics technology, electronic and electrical equipment has been widely used. For more complete functions and better experience of electronic and electrical equipment, the internal functional modules of each electronic and electrical equipment Communication and the communication function between multiple electrical and electronic devices are also very important. Since the controllers of electronic and electrical equipment and their respective functional modules may be single-chip microcomputers, DSPs, FPGAs, PLCs, etc., their respective operating voltages are inconsistent, resulting in inconsistent communication logic levels between them, and the required input current, output The driving current is also different. In order to ensure stable and reliable communication with each other, the matching of logic levels in the communication circuit is the first problem to be solved [1].

At present, the logic level matching of different voltage levels in communication circuits usually considers devices such as optocouplers. The circuits built by such devices can not only achieve logic level matching, but also have isolation functions, but the components required for circuits built by such devices There are many devices, the cost is high, and the parameters of the optocoupler are high in high-speed communication [2].

This paper introduces a logic level matching circuit in communication circuits. This circuit is mainly based on the switching principle of triodes, combined with the characteristics of unidirectional conduction and low conduction voltage drop of Schottky diodes, and realizes the matching of different logic levels in communication circuits. It can solve the problem of many devices and high cost of the current logic level matching circuit. At the same time, the switching function of the circuit can effectively ensure the independence of circuits of different voltage levels without interference and influence, and ensure the stability and reliability of the entire circuit.

2. Design of logic level matching circuit in communication circuit

2.1. Basic Requirements for Hardware Design of Logic Level Matching Circuits in Communication Circuits

- Level relationship: The output voltage of the driving device must be within the input voltage range required by the load device, and a certain noise tolerance (Vohmin-Vihmin≥0.4V, Vilmax-Volmax≥0.4V) must be guaranteed [3].
- Driving ability: The driving device must be able to meet the maximum demand of the load device for sinking and sourcing current [4].
- Delay characteristics: The delay caused by logic level conversion should be fully considered in the design to ensure that data transmission can meet the timing tolerance of load devices, especially high-speed signals.
- Rise/fall time characteristics: It should be ensured that Tplh and Tphl meet the requirements of the circuit timing relationship and the requirements of EMC.
- Requirements for voltage overshoot: The overshoot should not exceed the absolute maximum voltage allowed by the device, otherwise it may cause damage to the device.

2.2. Hardware Design of Logic Level Matching Circuit in Communication Circuit

First of all, according to the principle of level matching, the circuit needs to be isolated, and the high and low voltage terminals use different voltages, so the circuit considers using diodes and triodes to isolate.

Secondly, because the driving capabilities of different devices are inconsistent, we consider using pull-up resistors, so that according to Ohm's law, the current of the circuit is proportional to the voltage on the power supply communication line, and inversely proportional to the impedance on the line, that is

$$I = \frac{U}{R} \tag{1}$$

By adjusting the size of the resistance, the matching of different driving capabilities can be achieved.

Finally, considering the delay and interference, filter capacitors are used in the circuit design to ensure the stability and reliability of the circuit.

The logic level matching hardware circuit in the communication circuit is shown in Figure 1:

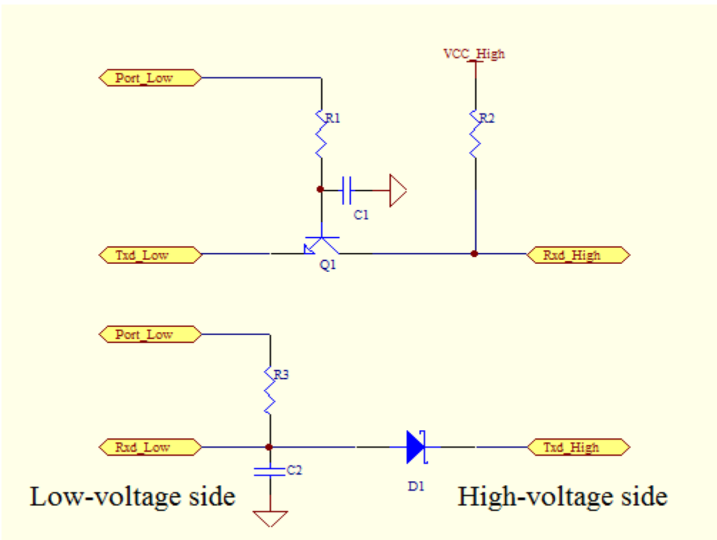

Figure 1. The logic level matching hardware circuit

Circuit related symbols and device descriptions:
- Port_Low is the low-voltage side control port.
- Txd_Low is the data transmission port on the low voltage side.
- Rxd_Low is the data receiving port on the low voltage side.
- VCC_High is the power supply of the high voltage side.
- Txd_High is the data transmission port on the high-voltage side.
- Rxd_High is the data receiving port on the high voltage side.

2.3. The function of the circuit is introduced

2.3.*1. The process of sending logic levels from the low voltage side to the high voltage side in the communication circuit*

When the low-voltage side needs to send a logic level to the high-voltage side, the low-voltage side control port Port_Low outputs a high level, and then

- When the low-voltage side sends a logic level "1" through the Txd_Low port, since there is no voltage difference between the B-level and E-level of the transistor Q1, the transistor Q1 is turned off [5], the current cannot flow through the transistor Q1, and the high-voltage side Rxd_High port level is pulled up by the resistor R2 is pulled to a logic high level, that is, the high-voltage terminal Rxd_High port receives a logic level "1".
- When the low-voltage side sends a logic level "0" through the Txd_Low port, since the voltage difference between the B-level and E-level of the transistor Q1 exceeds the conduction condition of the transistor Q1, the transistor Q1 is turned on, and the current flows through the pull-up resistor R2 on the high-voltage side. After passing through the transistor Q1, since the turn-on voltage of the C-level and E-level of the transistor Q1 is very low, usually about 0.2V, the high-voltage terminal Rxd_High port receives a level signal of about 0.2V, which is consistent with the logic low level less than 0.3VCC [6]. Level requirements, that is, the high-voltage terminal Rxd_High port receives a logic level "0".

When the low-voltage side compensation needs to send a logic level to the high-voltage side, the low-voltage side control port Port_Low outputs a low level, and the transistor Q1 is turned off, so that the current cannot flow through the transistor Q1, and the high-voltage side and the low-voltage side do not affect each other.

2.3.2. The logic level process of the low-voltage side receiving the high-voltage side sending in the communication circuit

When the low-voltage side needs to receive the logic level sent from the high-voltage side, it outputs a high level through the low-voltage side control port Port_Low, and then

- When the high-voltage side sends a logic level "1" through the Txd_High port, since the forward voltage of the diode D1 is less than the reverse voltage, the diode D1 is turned off, the current cannot flow through the diode D1, and the low-voltage side Rxd_Low port level is pulled by the pull-up resistor R3. to a logic high level, that is, the low-voltage end Rxd_Low port receives a logic level "1".
- When the high-voltage side sends a logic level "0" through the Txd_High port, since the forward voltage of the diode D1 is greater than the reverse voltage, and the diode D1's turn-on voltage condition is reached, the diode D1 is turned on, and the current flows through the low-voltage side pull-up resistor R3. Through diode D1, since the forward voltage drop of diode D1 is very low, usually about 0.2~0.3V, the Rxd_Low port of the low-voltage side receives a level signal of about 0.2~0.3V, according to the logic low level less than 0.3VCC Level requirements, that is, the low-voltage end Rxd_Low port receives a logic level "0".

When the low-voltage side does not need to receive the logic level sent from the high-voltage side, the low-voltage side control port Port_Low outputs a low level, so that the forward voltage of the diode D1 is not greater than the reverse voltage, so that the conduction voltage condition of the diode

D1 cannot be reached, that is, Turn off the diode D1, so that the current cannot flow through the diode D1, and the high-voltage side and the low-voltage side do not affect each other.

2.4. Analysis, testing and verification of circuits

When evaluating the communication circuit, the function of the circuit must be ensured first. Therefore, by using a single-chip microcomputer system with a working voltage of +3.3V as the low-voltage side [7], and a GPRS system with a working voltage of +3.9V as the high-voltage side, the connection between the high and low-voltage sides is performed. to communicate with each other, thereby verifying the functionality of the carrier communication circuit.

By testing with a Tektronix oscilloscope [8], when the +3.3V MCU system on the low-voltage side sends data, the +3.9V GPRS system on the high-voltage side is in the receiving state, the waveform sent by the low-voltage side of the +3.3V MCU system and the high-voltage side of the +3.9V GPRS system The receiving waveform is shown in Figure 2, where channel 1 (CH1) is the signal sent by the +3.3V single-chip microcomputer system on the low-voltage side, and channel 2 (CH2) is the +3.9V GPRS system receiving end signal on the high-voltage side.

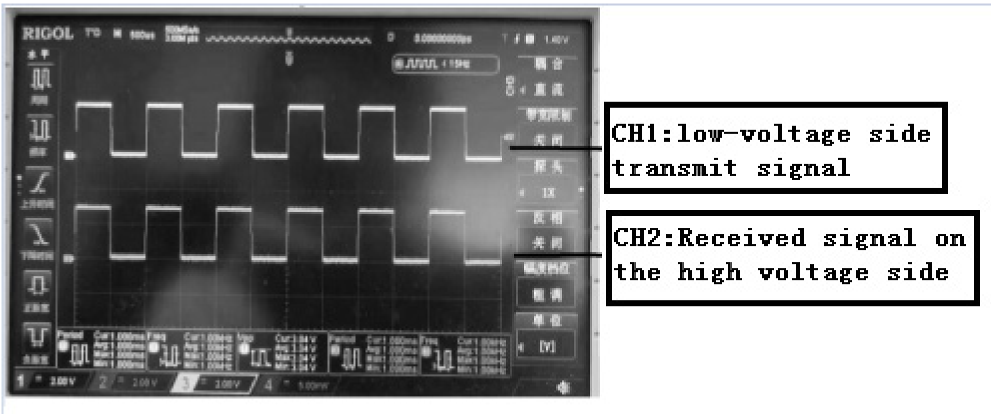

Figure 2. Low-voltage side sending and high-voltage side receiving waveforms

When the high-voltage side of the +3.9V GPRS system sends data, the +3.3V single-chip microcomputer system on the low-voltage side is in the receiving state, and the waveform sent by the high-voltage side of the +3.9V GPRS system and the low-voltage side of the +3.3V single-chip system are received. The waveform is shown in Figure 3: Channel 1 (CH1) is the receiving end signal of the +3.3V single-chip microcomputer system on the low-voltage side, and channel 2 (CH2) is the +3.9V GPRS system sending signal on the high-voltage side.

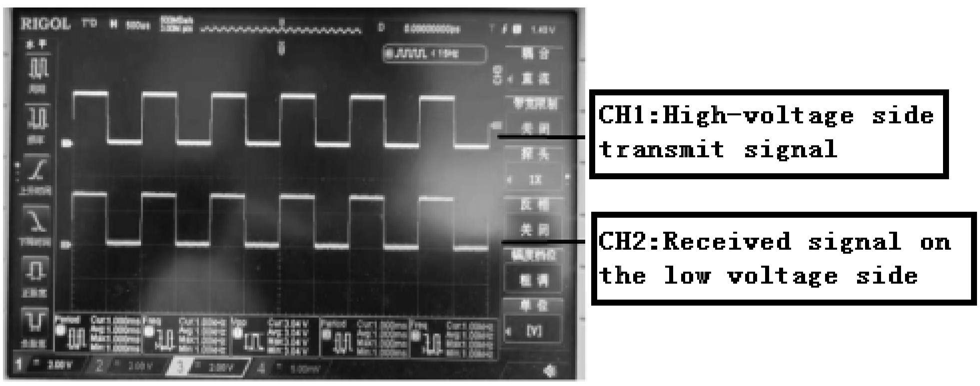

Figure 3. High-voltage side sending and low-voltage side receiving waveforms

From the data detected by the oscilloscope, it can be determined that when the low-voltage side of the +3.3V MCU system or the high-voltage side of the +3.9V GPRS system sends data, the other party can receive the relevant data in a timely and accurate manner, and then continue to return the data. The built high and low voltage level matching circuit is tested for transmission rate and stability. The feasibility and reliability of the design function of the level matching circuit are also verified by instruments such as oscilloscopes and the actual measurement results, and the communication circuits of different voltage levels are realized. function of logic level matching circuits.

3. Conclusion

With the rapid development of electronic technology, electronic products have been widely used, and the matching of logic levels in communication circuits between modules of different voltage levels is becoming more and more important. The logic level matching circuit of communication has simple structure, stable performance and low cost, and is very suitable for use in communication circuits between various voltage level modules in equipment and products in the industrial and commercial fields.

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"Golden Course" Construction of "University Physics Experiment" Course of Guangdong Provincial Department of Education, Document Number: Yuejiao Gao [2019] No. 6

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