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Design of 1T2M integration of storage and calculation based on threshold memristor

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Abstract. Memristor is a new type of electronic component with small size and non-volatile, and it is the most promising new electronic component to replace MOS tube. The computing and storage parts of the computing electronic machines we use today are separate. With the development of technology and new materials, the indicators of CPU and memory have undergone qualitative changes, but the data transmission of CPU and memory still needs to rely on the bus, which greatly reduces the performance of computing and storage. This paper studies the integration of storage and computing. The ultimate purpose of this experiment is to integrate computing and storage into one chip. This paper proposes a 1T2M memory-computing integrated circuit design based on threshold-type memristors. This circuit is a new circuit structure. This circuit consists of an NMOS transistor and two threshold-type memristors. This structure can realize “OR logic operation” and “storage”. The circuit structure is simple, the performance is better, the number of transistors is less, the integration level is higher, and the reading and writing speed is faster. The simulation verification is carried out by LTSpice.

1. Introduction

The concept of memristor [1] was first proposed by Cai Shaotang, and HP Labs announced the first memristor [2]. The resistance value of the memristor changes with the flow of electric charge [3], and has the characteristics of non-volatility, small size, low power consumption and easy compatibility with CMOS technology [4]. Many researchers have studied various aspects of memristors, making memristors achieve good results in many fields such as memory circuits [5], logic circuits [6], chaotic circuits [7], and neural networks [8]. With the development of artificial intelligence, a large amount of data needs to be stored and calculated. However, the traditional Von Neumann architecture is separated from the calculation and storage units, which greatly reduces the performance of the computer and causes a waste of resources. Now many scientific researchers are studying the integrated circuit of storage and calculation. This paper proposes a new integrated circuit structure of memory and calculation. Compared with other integrated circuits of memory and calculation, the circuit has simpler structure, better performance, fewer transistors, higher integration, and faster read and write speed.



2. Memristor Model

A large number of researchers have obtained memristors with different characteristics based on different materials and different technical means, and subsequently established various memristor models with different characteristics, such as threshold-type memristor models and general-purpose memristor models etc [9]. Among them, the threshold-type memristor model [10] is mainly used in this paper. When the applied voltage is greater than or equal to the positive threshold voltage, the memristor resistance becomes low resistance, and when the applied voltage is less than or equal to the negative threshold voltage, the memristor resistance becomes high resistance, and when the applied voltage is greater than the negative threshold voltage and less than the positive threshold voltage, the resistance value of the memristor remains unchanged. This model proposes a mathematical model as follows:

$$\frac{dx}{dt} = \begin{cases} \frac{1}{e^{x-a}} & v > 0.2 \\ 0 & -0.2 \leq v \leq 0.2 \\ \frac{-1}{e^{-x-a}} & v < -0.2 \end{cases}$$

$$R(x) = \begin{cases} R_{ON} & x \geq 0 \\ R_{OFF} & x < 0 \end{cases}$$

$$i(t) = \frac{1}{R(x)} v(t)$$

where x is the state variable of the system, a is a parameter representing the voltage across the memristor, i is the current flowing through the memristor, $R(x)$ is the memristor resistance value, and R_{on} and R_{off} are the low and high resistances. The voltage-current characteristic curve is shown in the figure 1.

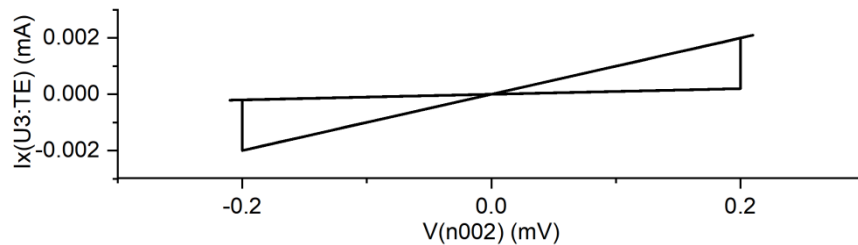


Figure 1. Voltage-current characteristic curve.

3. 1T2M storage and calculation integrated circuit

The circuit proposed in this paper is composed of two memristors and one NMOS transistor, in which the NMOS transistor is equivalent to an equivalent resistor, and the memristors are connected in parallel with each other to realize binary calculation and storage functions. A voltage greater than 0 represents a high level (logic 1), and a voltage less than or equal to 0 represents a low level (logic 0). Connect the gate of the NMOS tube to VDD to ensure that $V_{gs} > V_{th}$, so that the NMOS tube is turned on. At this time, the equivalent resistance of the NMOS tube is set to R_1 . The circuit diagram is shown in the figure 2.

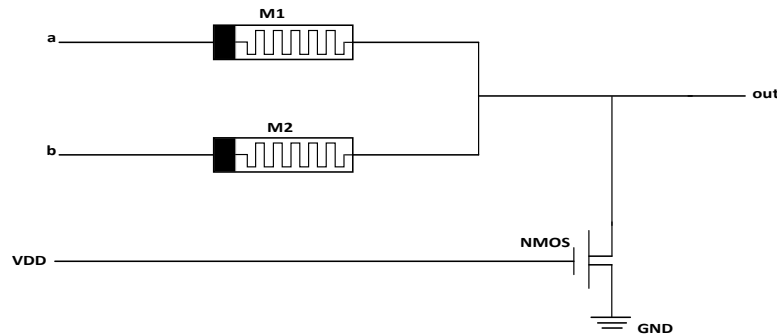


Figure 2. Integrated circuit diagram of 1T2M storage and calculation.

3.1. Calculation

The resistance values of each memristor in 1T2M are R_{on} and R_{off} , and the gate of the NMOS tube is connected to VDD to ensure that the NMOS tube is turned on at all times, which is equivalent to an equivalent resistance R_1 .

(1) When $a=V_H$ $b=V_H$

$$M1=R_{on}, M2=R_{on}$$

$$out = \frac{V_H}{\frac{R_{on}}{2} + R_1} R_1 > 0$$

$$out \approx V_H$$

(2) When $a=V_H$ $b=V_L=-V_H$

$$M1=R_{on}, M2=R_{off}$$

$$\frac{V_H - out}{R_{on}} = \frac{out + V_H}{R_{off}} + \frac{out}{R_1}$$

$$out = \frac{V_H (R_1 R_{off} - R_1 R_{on})}{R_{on} R_{off} + R_1 R_{on} + R_1 R_{off}} > 0$$

$$out \approx V_H$$

(3) When $a=V_L=-V_H$ $b=V_H$

$$M1=R_{off}, M2=R_{on}$$

$$\frac{V_H - out}{R_{on}} = \frac{out + V_H}{R_{off}} + \frac{out}{R_1}$$

$$out = \frac{V_H (R_1 R_{off} - R_1 R_{on})}{R_{on} R_{off} + R_1 R_{on} + R_1 R_{off}} > 0$$

$$out \approx V_H$$

(4) When $a=V_L=-V_H$ $b=V_L=-V_H$

$$M1=R_{off}, M2=R_{off}$$

$$out = \frac{-V_H}{\frac{R_{off}}{2} + R_1} R_1 \leq 0$$

$$out = V_L$$

Table 1. a and b implement the "OR logic" operation.

a	b	out
VL	VL	VL
VL	VH	VH
VH	VL	VH
VH	VH	VH

3.2. Read operation

When reading again, set the reading voltage $a = b = V_{READ}$ between the positive and negative

threshold voltage to ensure that the resistance of the memristor is not changed. If the total read current of the circuit is $I_{\text{READ}} = \frac{V_{\text{READ}}}{R_{\text{total}}} = \frac{V_{\text{READ}}}{\frac{M_1 M_2}{M_1 + M_2} + R_1}$, the read current information is as follows:

(1) When $M_1 = R_{\text{on}}, M_2 = R_{\text{on}}$,

$$I_{\text{READ}} = \frac{V_{\text{READ}}}{R_{\text{total}}} = \frac{V_{\text{READ}}}{\frac{R_{\text{on}}}{2} + R_1}$$

(2) When $M_1 = R_{\text{on}}, M_2 = R_{\text{off}}$,

$$I_{\text{READ}} = \frac{V_{\text{READ}}}{R_{\text{total}}} = \frac{V_{\text{READ}}}{\frac{R_{\text{on}} R_{\text{off}}}{R_{\text{on}} + R_{\text{off}}} + R_1}$$

(3) When $M_1 = R_{\text{off}}, M_2 = R_{\text{on}}$,

$$I_{\text{READ}} = \frac{V_{\text{READ}}}{R_{\text{total}}} = \frac{V_{\text{READ}}}{\frac{R_{\text{on}} R_{\text{off}}}{R_{\text{on}} + R_{\text{off}}} + R_1}$$

(4) When $M_1 = R_{\text{off}}, M_2 = R_{\text{off}}$,

$$I_{\text{READ}} = \frac{V_{\text{READ}}}{R_{\text{总}}} = \frac{V_{\text{READ}}}{\frac{R_{\text{off}}}{2} + R_1}$$

4. Simulation

In this section, LTSpice is used to simulate the circuit of the proposed storage-computing integration. The memristor used in this paper is a threshold-type memristor. When the voltage at both ends is greater than or equal to 0.2V, the resistance value of the memristor is R_{on} equal to 100Ω. When the voltage across the two ends is less than or equal to -0.2V, the resistance value of the memristor is R_{off} equal to 1000Ω. The turn-on voltage of the NMOS tube used in this article is 0.7V, and the equivalent resistance is 50Ω.

4.1. Calculation

(1) when $a = V_H, b = V_H$

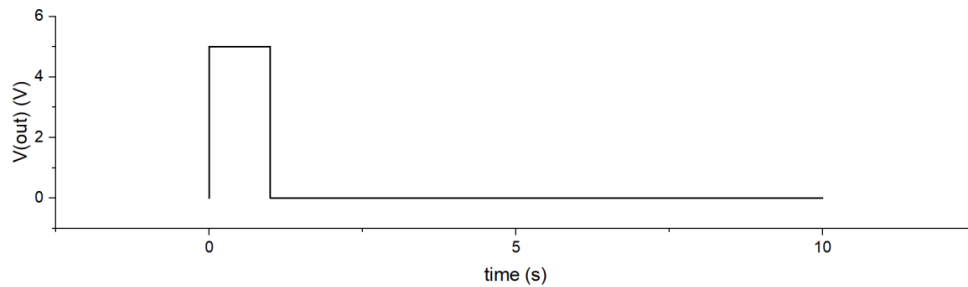


Figure 3. When a is high level and b is high level. The output voltage is high level.

(2) when $a = V_H, b = V_L = -V_H$

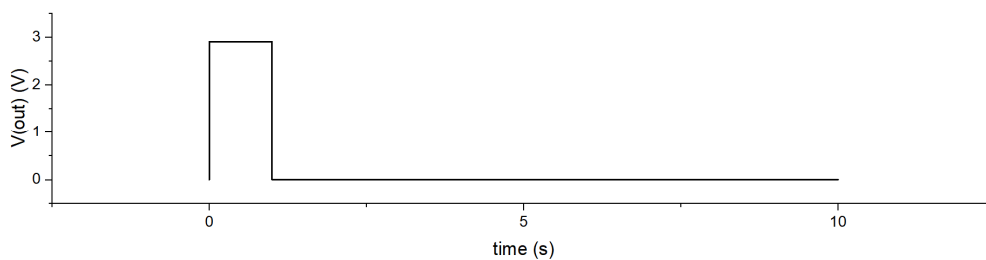


Figure 4. When a is high level and b is low level. The output voltage is high level.

(3) when $a=V_L=-V_H$ $b=V_H$

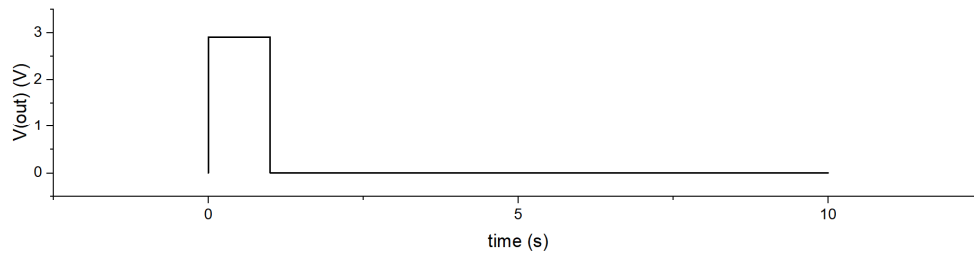


Figure 5. When a is low level and b is high level. The output voltage is high level.

(4) when $a=V_L=-V_H$ $b=V_L=-V_H$

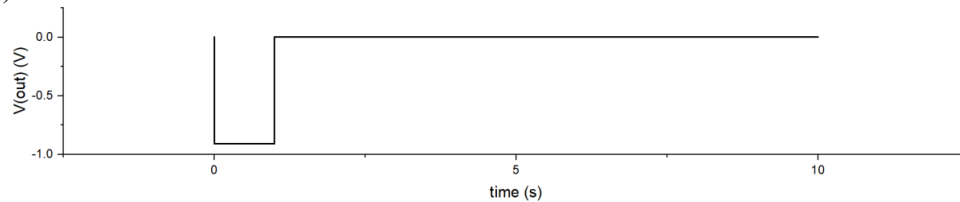


Figure 6. When a is low level and b is low level. The output voltage is low level.

4.2. Read operation

(1) when $M1=Ron, M2=Ron,$

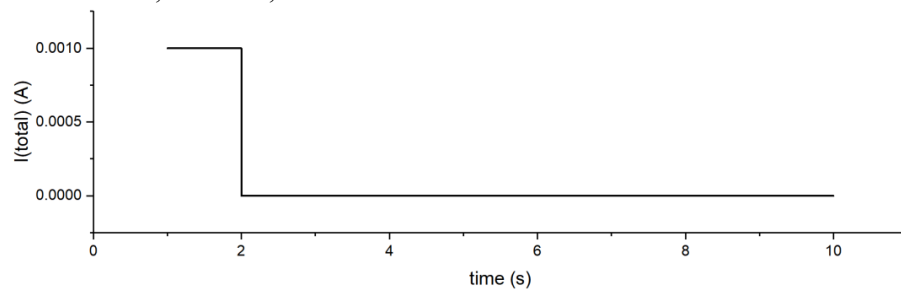


Figure 7. When M1 is Ron level and M2 is Ron. Value the I(total).

(2) when $M1=Ron, M2=Roff,$

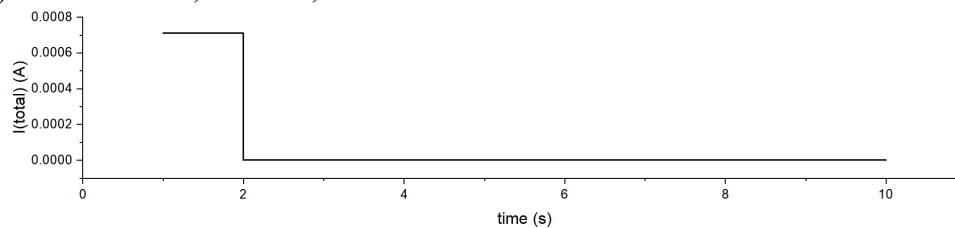


Figure 8. When M1 is Ron level and M2 is Roff. Value the I(total).

(3) when $M1=Roff, M2=Ron,$

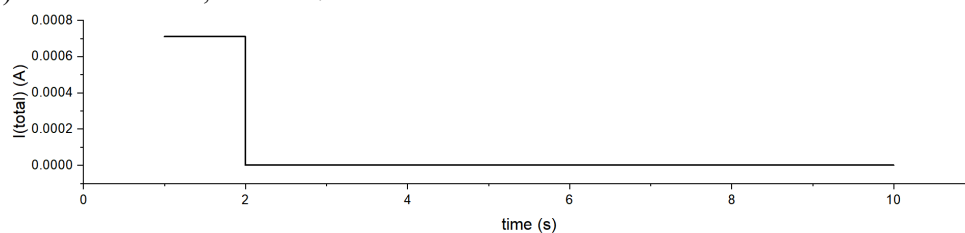


Figure 9. When M1 is Roff level and M2 is Ron. Value the I(total).

(4) when $M1=R_{off}$, $M2=R_{off}$,

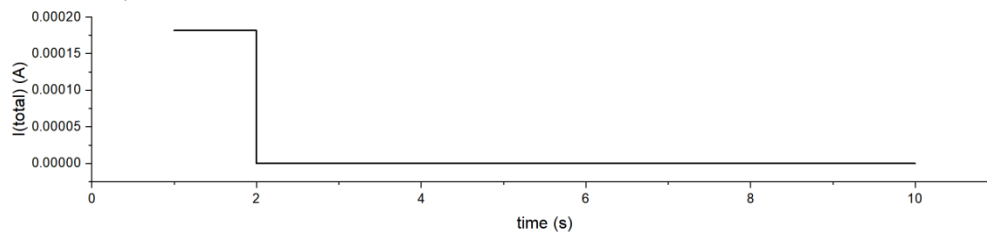


Figure 10. When $M1$ is R_{off} level and $M2$ is R_{off} . Value the $I(total)$.

5. Conclusion

This paper proposes an "integrated circuit of storage and computation based on threshold memristor 1T2M", which can perform OR operation and store data. It has been verified with LTSpice simulation software. It is hoped that further in-depth research on the integrated circuit of storage and calculation can be carried out in the future research.

Acknowledgments

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References

- [1] Chua, L. (1971) Memristor-the missing circuit element. *IEEE Transactions on Circuit Theory*, 18: 507–519.
- [2] Li, L. (2020) Graphene oxide: graphene quantum dot nanocomposite for better memristic switching behaviors. *Nanomaterials*, 10: 1448–1461.
- [3] Abraham, I. (2018) The case for rejecting the memristor as a fundamental circuit element. *Scientific Reports*, 8: 10972–10980.
- [4] Luo, L. (2020) Memristor based stateful logic gates for multi-functional logic circuit. *IET Circuits Devices & Systems*, 14: 811–818.
- [5] Kvatinsky, S. (2014) MAGIC-Memristor-Aided Logic. *IEEE Transactions on Circuits and Systems II-Express Briefs*, 61: 895–899.
- [6] Wang, G. (2020) Design of memristor based multiplier circuits. *Journal of Electronics & Information Technology*, 42: 827–834.
- [7] Wu, R. (2016) A new simple chaotic circuit based on memristor. *International Journal of Bifurcation and Chaos*, 26: 1650145.
- [8] Hong, Q. (2021) Memristive self-learning logic circuit with application to encoder and decoder. *Neural Computing and Applications*, 33: 4901–4913.
- [9] Kvatinsky, S. (2013) TEAM: ThrEshold Adaptive Memristor Model. *IEEE Transactions on Circuits and Systems I-Regular Papers*, 60: 211–221.
- [10] Wang, X. (2021) A behavioral spice model of a binarized memristor for digital logic implementation. *Circuits, Systems, and Signal Processing*, 40: 2682–2693.