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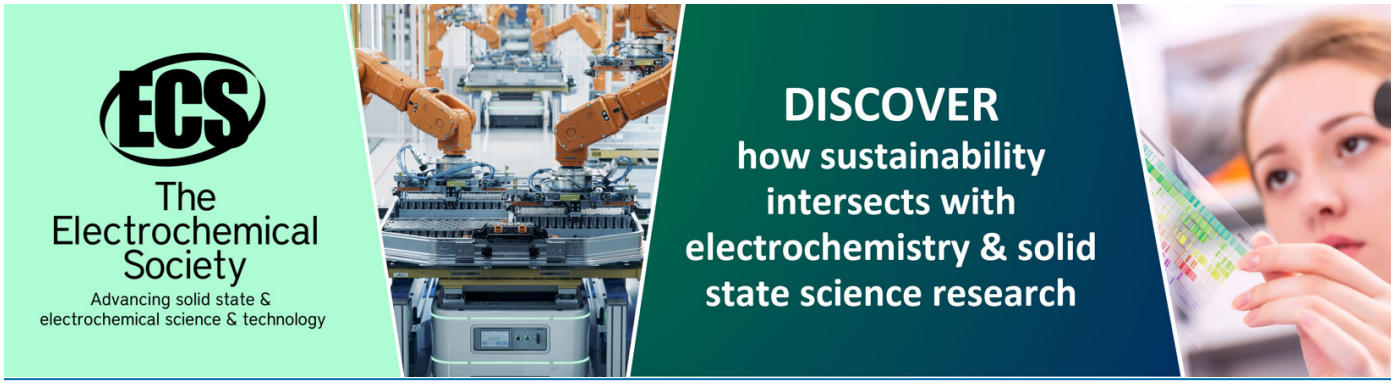

Design of low-power CIC decimation filter based on nibble serial arithmetic

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Abstract. Aiming at the problem of large area and high power consumption of traditional CIC (Cascade Integral Comb Filter) decimation filter, a folded multistage cascade CIC decimation filter is designed. The nibble-serial arithmetic and multiplexing technology are used to reduce the operation and storage logic unit, lower the cost and improve the utilization efficiency of system resources. The folded multistage cascade CIC decimation filter has a programmable structure of down sampling factor and can dynamically realize 1~16 times extraction. It is suitable for communication systems with multiple channel bandwidths. In addition, the designed truncation module can optimize the effective accuracy of the final stage output.

1. Introduction

The implementation of the decimation filter is crucial to the digital down-conversion circuit, which is widely used in the fields of mobile, satellite, broadcast communication and radar detection [1]. In 1980, Eugene B Hogenauer proposed Cascade Integrator Comb (CIC) [2], which includes an integrator working at a high sampling rate and a comb at a low sampling rate [3]. The traditional CIC filter is used to process the data stream directly, which not only occupies a large area, but also increases the dynamic power consumption [4]. Recent studies use a non-recursive model [5, 6, 7, 8]. Although the power consumption is reduced, the hardware complexity is high, and the extraction multiple is fixed, which is difficult to adapt to different requirements.

This paper presents a design scheme of recursive programmable multi-stage cascaded CIC decimation filter based on nibble serial algorithm. The use of nibble serial algorithm and multiplexing technology can effectively reduce costs and improve computing efficiency [9]. The recursive structure can realize the extraction of arbitrary multiples [10]. In order to fit different situations, a configurable design is added. Meanwhile, in the final output stage, the effective bit width is adjusted according to decimation multiple.

2. ASIC circuit design

2.1. system design

For the problem where the internal bit width of the traditional CIC decimation filter is too high, this design innovatively proposes the overall architecture based on the nibble serial algorithm as shown in Figure 1. Including the clock control module and the CIC decimation filter realization structure[11, 12]. The clock control module generates low frequency clock required by each module; the CIC decimation filter has 6 modules, namely: coding, integrator, decimator, comb filter, serial-to-parallel

conversion, and truncation module.

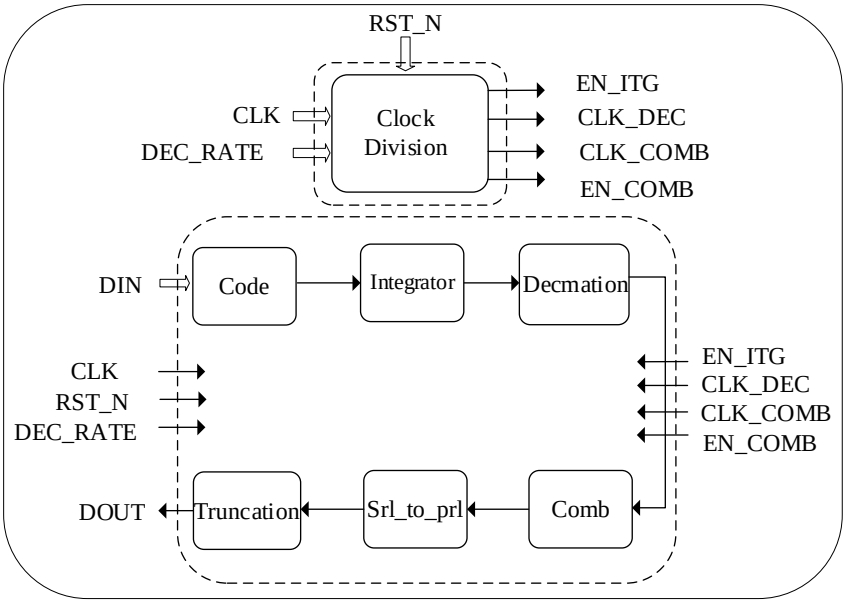


Figure 1. Overall structure block diagram

2.2. Coding module design

In order to ensure sufficient precision and prevent data overflow, the effective bit width is changed from 22 to 40 through bit expansion, and the expanded effective bit is filled with MSB of the input data. Based on the principle of nibble algorithm, the signal with extended bit width is sequentially divided into 4 pieces of data (same bit width from MSB to LSB), which are serially output from low to high.

2.3. Integrator and comb filter design

The integrator is mainly composed of an adder and a register [13]. Without affecting the input stream, start new accumulation after every 4 serial data accumulations are completed. Its state equation is :

$$y(n) = x(n) + y(n-4) \tag{1}$$

Figure 2 is the structural diagram of integrator. The input data of the integrator is encoded data, and the addition of significant bits produces the carry signal, which is stored in register. After a delay of one clock cycle, the carry signal is carried to high order. When the accumulation of 4 serial data is completed, it is equivalent to the completion of 40-bit data operation, so the carry signal generated by the last accumulation does not participate in the next accumulation operation.

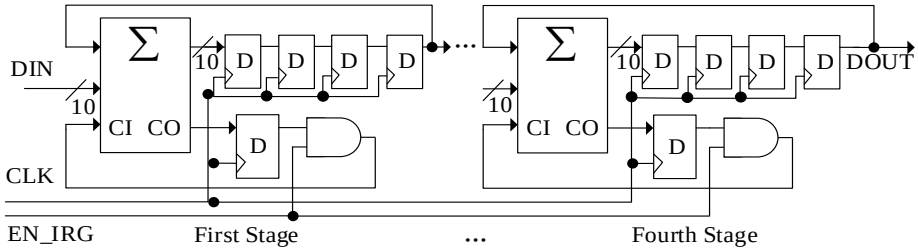


Figure 2. Schematic diagram of the structure of the integrator

Comb filter is also mainly composed of an adder and a register. The adder is cleared after every 4 serial data addition operations. Its state equation is :

$$y(n) = x(n) - x(n-4) \tag{2}$$

Figure 3 is the structural diagram of comb filter. The subtraction operation is transformed into addition operation by means of direct inversion of data, which simplifies the circuit structure of the operator.

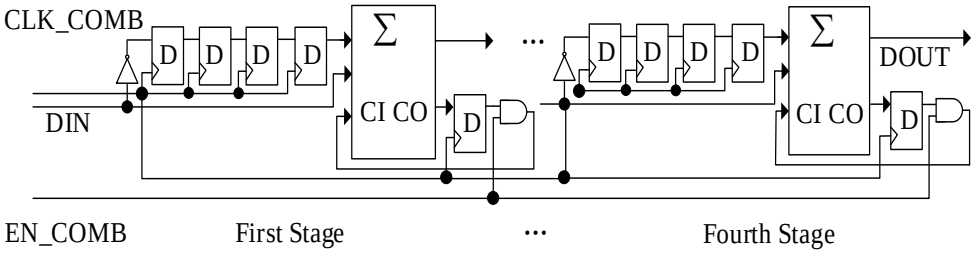


Figure 3. Schematic diagram of the structure of the comb filter

2.4. Extraction and truncation module design

The configured programmable decimation factor is transmitted to the clock control block and the truncation block, respectively. According to the frequency division control factor D and the principle of nibble serial algorithm, the clock control module generates the corresponding frequency division clock, then sends it to sub-modules of the CIC filter.

Based on the nibble serial algorithm, each bit of data is divided into 4, so the decimation module down-samples the input signal every 4*D clock cycles. Finally, the sampled 4-channel data is reorganized and converted into 1-channel data to output. The truncation module calculates the truncation bit width by substituting the input and output data word length - B_{in}, B_{out}, the decimation multiple - D, the delay factor - M, and the cascade number - N, into equation (3):

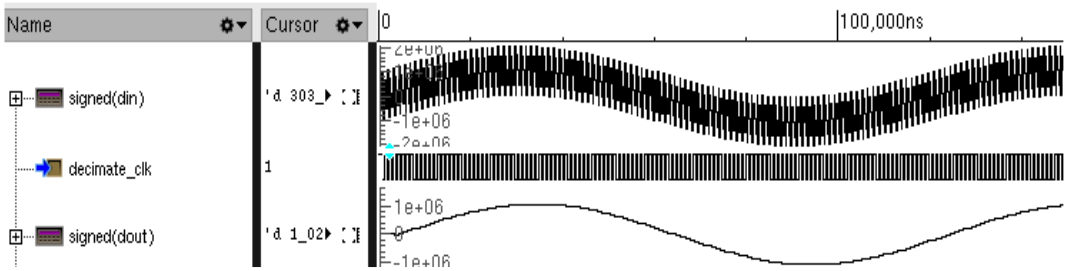
$$B_{LSB} = Nlog_2^{(DM)} + B_{\text{in}} - B_{out} \tag{3}$$

In order to achieve specific effective accuracy, the output is dynamically truncated by rounding [14, 15]. Retain the high significant bits required by the last stage that are the same as the output bit width and length, and round 0 to 1 for the discarded B_{LSB} low-order data.

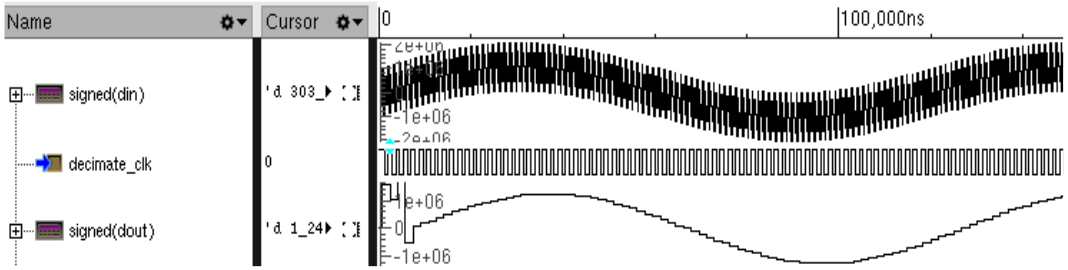
3. Results

3.1. Simulation verification

Adopt the top-down hierarchical design idea, the RTL level description of the whole module and the testbench for testing are designed by Verilog HDL language. Meanwhile, the NC_Verilog tool is used for simulation. Taking the decimation rate D equal to 3, 5, 9 and 15 as an example, the output simulation waveform is shown in Figure 4. It can be seen that the CIC filter designed in this paper can filter high-frequency noise and decimation.



(a)



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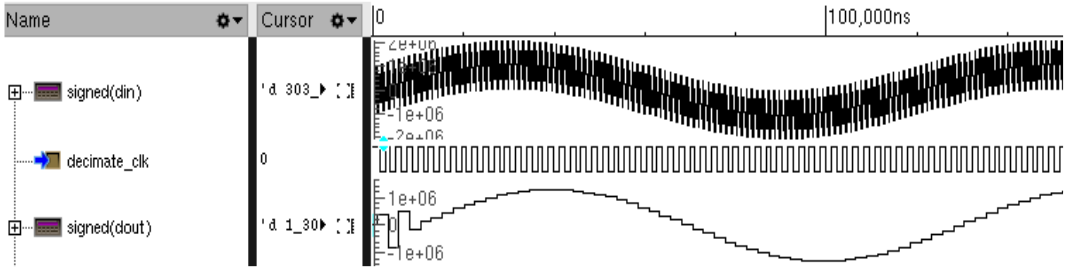
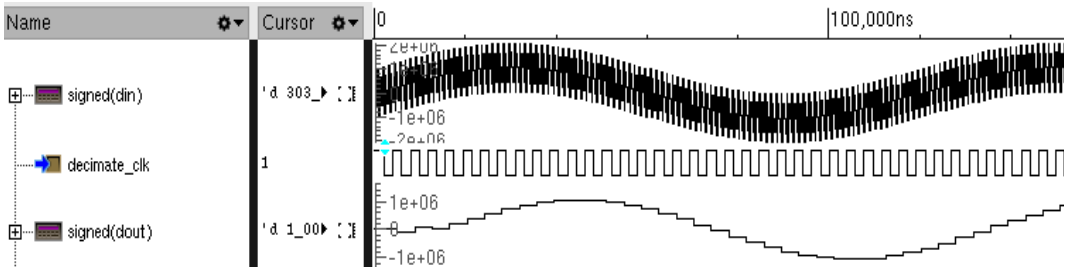


(c)



(d)

Figure 4. Output simulation waveform from different decimation rate
(a — 3, b — 5, c — 9, d — 15)

3.2. DC synthesis

Using Design Compiler (DC) of Synopsys to perform circuit synthesis based on 65 nm CMOS standard cell technology library. Then the corresponding gate-level netlist is obtained, as shown in Figure 5.

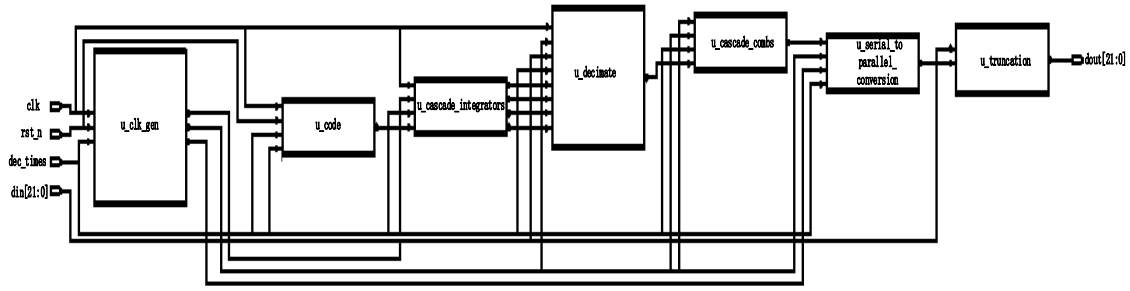


Figure 5. CIC filter DC synthesis netlist

Compared with the traditional CIC filter, the CIC filter designed in this paper reduces the area by 45.51% and the power consumption by 68.95%. In sum, power consumption and area have been greatly improved. The results are shown in Table 1.

Table 1. Comparison of performance parameters

index	This article	traditional
craft	65nm CMOS	65nm CMOS
Area / μm ^{2}	3529	6476
Dynamic power consumption / mW	0.9503	3.0604

The area is divided into combinational logic, buffer and non-combinational logic area; power consumption is divided into dynamic and static power consumption; dynamic power consumption is caused by short-circuit current and switched capacitors; static power consumption is mainly composed of leakage power consumption.

3.3. Layout and routing

The purpose of placement and routing is to convert the gate-level netlist (Gate Netlist) generated by the front-end design into the layout file through electronic design automation software (Innovus).

Utilize the gate-level netlist file (.v) and constraint file (.sdc) generated by DC synthesis to perform placement and routing, resulting the design layout shown in Figure 6, the layout size is 83 nm*89 nm.

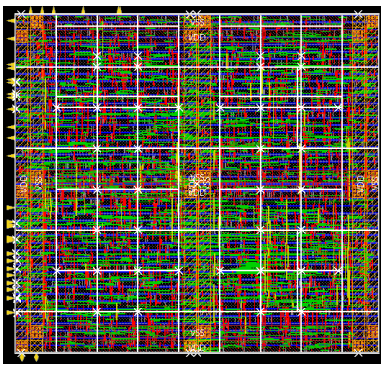


Figure 6. CIC decimation filter layout and wiring diagram

3.4. Gate Level Simulation

Gate-level simulation is to back-label the delay information of placement and routing to the design netlist for post-simulation. The delay file (.SDF) at this time is the most comprehensive, including gate-level delays and routing delays.

Figure 7 shows the gate-level simulation waveform with a decimation multiple of 2. The results show that the design can correctly implement the 2x down-sampling and filtering functions. In addition, the timing and signal integrity requirements are met.

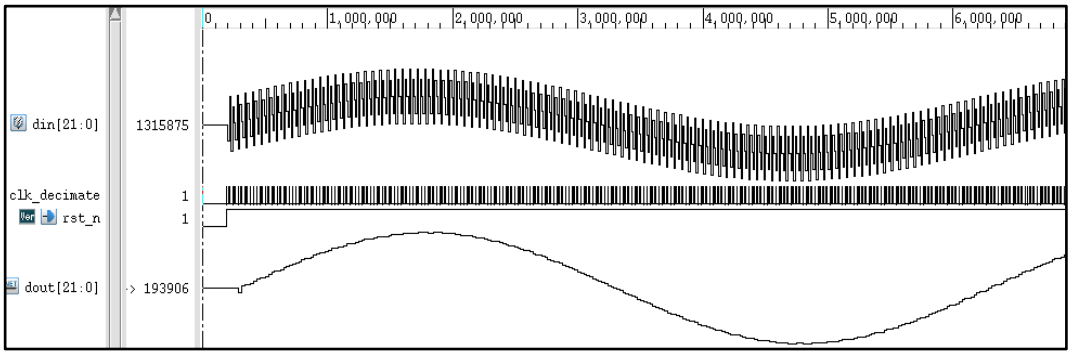


Figure 7. Gate simulation CIC decimation filter waveform

4. Conclusion

This paper discusses a design method of a programmable cascaded CIC decimation filter based on nibble serial algorithm. Hence, the input data is divided into 4 groups with a bit width of 10 bits from MSB to LSB, reducing the use of internal operation and storage logic units. The programming module can flexibly process multi-rate signals, and its decimation multiple is adjustable within the range of 1 to 16 times. Therefore, this design can be applied to communication systems with coexistence of multiple channel bandwidths.

In addition, the output of the final stage is dynamically truncated to achieve effective precision for a specific application. Based on the 65 nm CMOS standard cell library for DC synthesis, compared with the traditional CIC filter, this solution has significant advantages in reducing power consumption and area. Using Innouvs for automatic placement and routing, the layout size after placement and routing is 83 nm*89 nm. Adopting SDF and netlist files to complete the gate-level post-simulation, the correctness of the design is verified.

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Min Gao, master student, majoring in electronic science and technology, School of Internet of Things Engineering, Jiangnan University. The research direction is the design of large-scale integrated circuits.

Acknowledgments

The authors gratefully appreciate the assistance of the College of Io T Engineering, Jiangnan University. The design processing was performed in the China Electronics Technology Group Crop. This work was also grateful to Pro. Z.G. Yu and Dr. S.Q. Wan for their constructive discussion and technical support.

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