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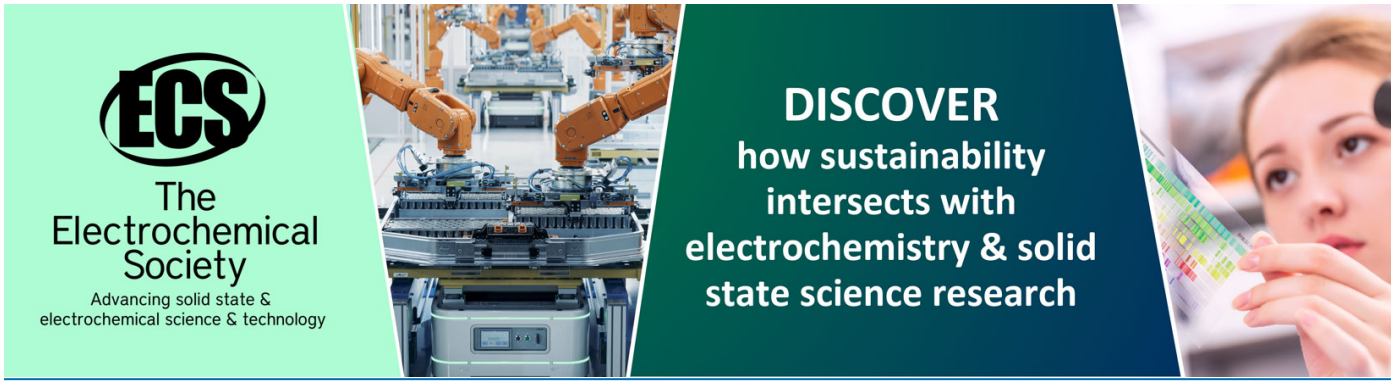

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A Compact 60GHz Power Amplifier in 65nm CMOS Technology

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Abstract. A compact 60GHz power amplifier chip in 65nm CMOS technology of three-stage common source structure is presented. The first two amplifiers offer sufficient gain to pre-amplify the small input power. The third stage amplifier uses two sets of differential pairs to achieve power synthesis. On-chip transformer coupling is adopted to realize inter-stage impedance matching as well as input and output matching. The compact structure of on-chip transformer can reduce the chip size and improve the integration degree. The measured small signal gain at 60GHz of 22.3dB, the saturation power of 20.2dBm, the output P_{-1dB} of 17.3dBm, the PAE of 14%, and the core area is 0.19mm^2. The power amplifier can be used in high-speed short-range wireless communication system to enhance communication data transmission capacity.

1. Introduction

With the rapid development of millimeter wave technology, the application of the internationally universal license-free 60GHz band in high-speed short distance communication links is capable of thousands of megabits of data transmission per second[1]. In wireless communication system, power amplifier plays a key role in communication distance and channel quality. Nowadays, the cut-off frequency of CMOS process devices has exceeded 200GHz, and process nodes are gradually reduced to ultra-deep sub-micron level[2]. Compared with group Ⅲ-Ⅴ compounds semiconductor technology, silicon-based CMOS technology has the unique advantages of high integration, low cost and easy integration with digital circuits. Millimeter-wave power amplifier based on silicon CMOS technology is faced with two problems: Firstly, in millimeter-wave band, various parasitic effects generated by transistors have many adverse effects on the gain and stability of the amplifier. Secondly, the low breakdown voltage brought about by smaller transistor sizes greatly limits the output power.

In this work, a high performance 60GHz power amplifier is designed based on 65nm CMOS technology and transformer matching method on chip. It has great application potential in high-speed short-range wireless communication, point-to-point wireless communication, high-precision radar detection and other fields.

2. Circuit topology

The circuit structure of the compact power amplifier designed in this paper is shown in Fig.1. The circuit topology of the three-stage common source amplifier cascade and the matching method of on-

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chip transformer are adopted to obtain sufficiently high gain and output power. The first two amplifiers were used as the driving stage, and the differential common source amplifiers were used to enhance the gain. The third-stage amplifier uses two groups of symmetrical differential pair transistor amplifiers to improve the output voltage swing through the power synthesis network of the four-input transformer structure, so as to improve the output power [3]. The input and output signals of the power amplifier are single-ended signals matched to the load of 50 ohm. The input impedance matching design increases the series differential inductor on the transformer to avoid the impedance mismatch problem. The standard on-chip transformer coupling structure is used between the first and second stage amplifiers. The output of the second stage amplifier and the input of the third stage amplifier are matched by four inputs on-chip transformers.

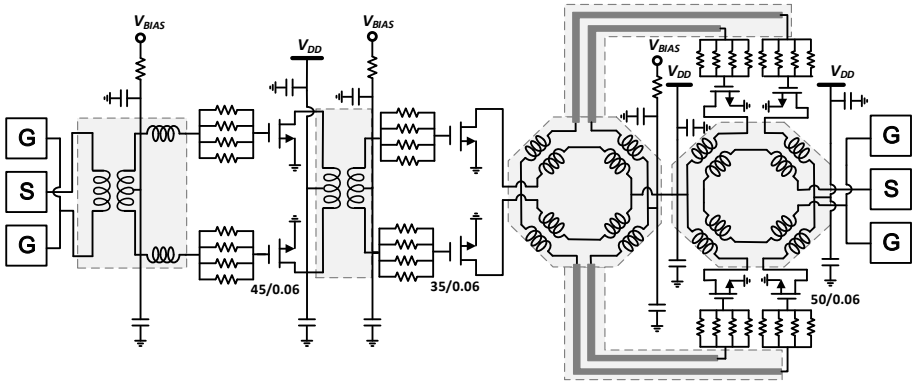


Fig.1 Schematic diagram of compact three stage power amplifier

2.1. Amplifier section

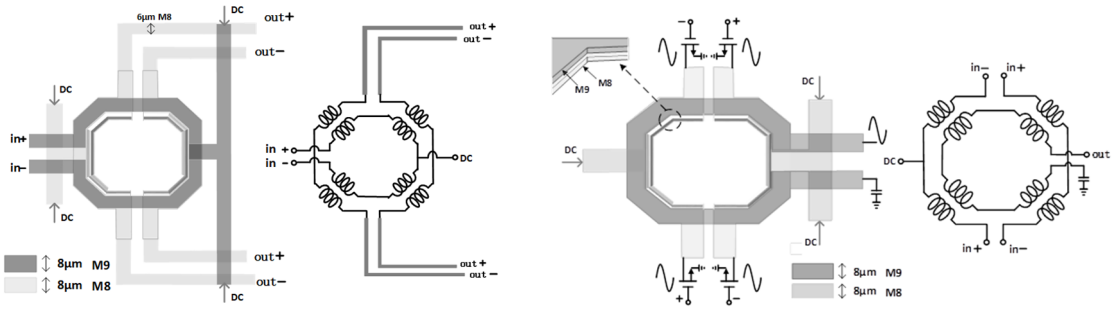
The active part of the power amplifier is constructed by the conventional amplifying circuit three stage topology cascade, which were all biased in class A. Based on the bias current density theory and load line theory combined with the formula, the transistor size of the power amplifier was deduced and calculated. Considering the transistor power gain and the loss and parasitic effect in the high frequency band, the transistor size and dc bias current are designed as follows: the transistor size of the first stage amplifier is set as 45/0.06μm, and the dc current is 20mA.The intermediate amplifier transistor size is set to 35/0.06μm, dc current 50mA. The third stage amplifier transistor size is set to 50/0.06μm, dc current 80mA.The transistor gate of each stage amplifier is in series, and the appropriate capacitance is added at each stage bias voltage and transformer tap to ensure the stability.

2.2. Transformer on-chip section

The 65nm CMOS process PDK used herein provides a total of 9-layer metal for a signal trace in which the top metal layer has the largest thickness and the lowest resistivity, and the insertion loss is relatively small [4]. The top two-layer metal is designed to have a tapped octagonal inductance, which is a state in which the space is vertically stacked. Using the primary coil, the vertical wide side coupling structure of the secondary coil can increase the coupling coefficient of inductance at a resonant frequency of 60 GHz. The central tap of the transformer primary coil and the secondary coil is a natural virtual ground, which is fed from this point to DC voltage, and the performance of the transformer is unaffected.

Power splitter uses a transformer matching network as shown in Fig.2(a). Two pairs of differential transmission lines are inserted between the power splitter and the output differential pair to compensate for the 1: 1 transformer impedance range. The output terminal impedance matching and power synthesis adopts the four-input transformer structure shown in Fig.2(b), the transformer secondary coil is grounded, and the power signal is completed by the differential-single-ended conversion, the synthesis of all the way signals. During the differential-single-ended conversion process, since the voltage swing of the matching network is effectively superimposed, the impedance

seen in each input port is a quarter of the load, compared to the standard 1: 1 transformer compared to voltage gain.



(a) (b)

Fig.2 On-chip transformer structure. (a) Power splitter, (b) Power combiner

3. Experimental results

The 60GHz power synthesizer chip is developed based on 65-nm CMOS technology. The on-chip transformer is used to make the circuit structure more compact and achieve sufficient power output while ensuring high gain and stability. The test conditions are power supply voltage 1.2V, each stage bias voltage 0.8V, input power is -25dbm.The measured S-parameters are shown in Fig.3. Under the condition of well-matched input/output, the power amplifier can achieve the working bandwidth of 8GHz in the range of 56GHz-64GHz, in which the small signal gain is better than 20dB and the reverse isolation is more than 40dB.

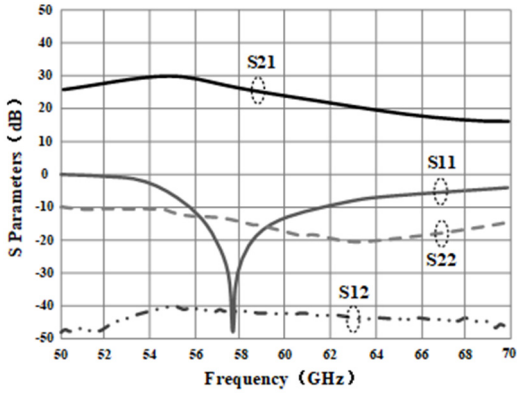
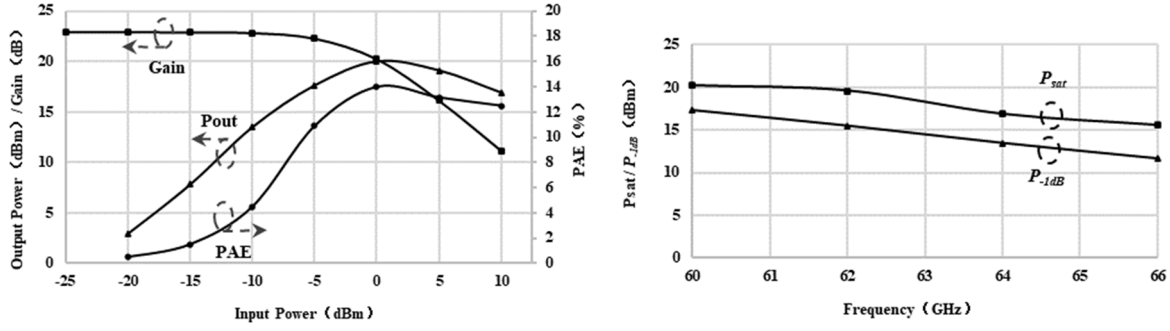


Fig.3 Measured S-parameters

As shown in Fig.4(a), the output power and gain test result at 60 GHz, wherein the PAE reaches 14% when the input power of 0 dBm. As shown in Fig.4(b), in the 60 GHz to 66 GHz frequency range, the P_{sat} of 20.2 dBm, and the P_{-1dB} of 17.3 dBm at 60 GHz.



(a) (b)

Fig.4 (a)Measured gain and out power (b) Measured saturation power and output P_{-1dB}

The die photo of the PA is shown in Fig.5, the core area of 0.64 mm × 0.3 mm without the PAD. The Comparison of state-of-art 60GHz CMOS PAs list in Table. 1.

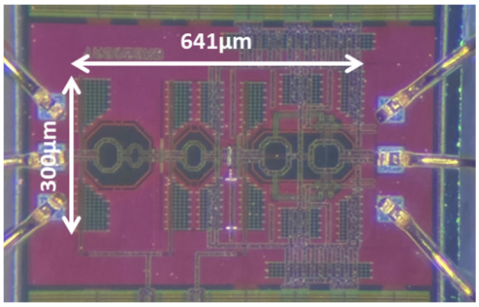


Fig.5 Die Photo of compact 60GHz power amplifier

Table.1 Comparison of state-of-art 60GHz CMOS PAs

Parameters	This work	[4]	[5]	[6]
CMOS/nm	65	65	65	65
Power Supply/V	1.2	1	1	1.2
Gain/dB	22.3	20.3	19.2	17.5
Psat/dBm	20.2	18.6	17.7	17.2
OP_{-1dB}/dBm	17.3	15	15.1	16.6
PAE/%	14	15.1	11.1	11.3
Core Area/mm^2	0.19	0.28	0.83	0.48

4. Conclusions

A high performance compact 60GHz power amplifier chip based on 65nm CMOS technology is designed. Three-stage common source amplifier cascade structure and on-chip transformer impedance matching networks are adopted to achieve sufficient power output while realising high gain and stability. The test results show that the power amplifier achieves a high gain of 19.5dB-27.5dB in the frequency range of 56GHz-64GHz, and the output saturation power is higher than 15dBm, which can meet the international universal application of 60GHz wireless communication system.

Acknowledgments

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