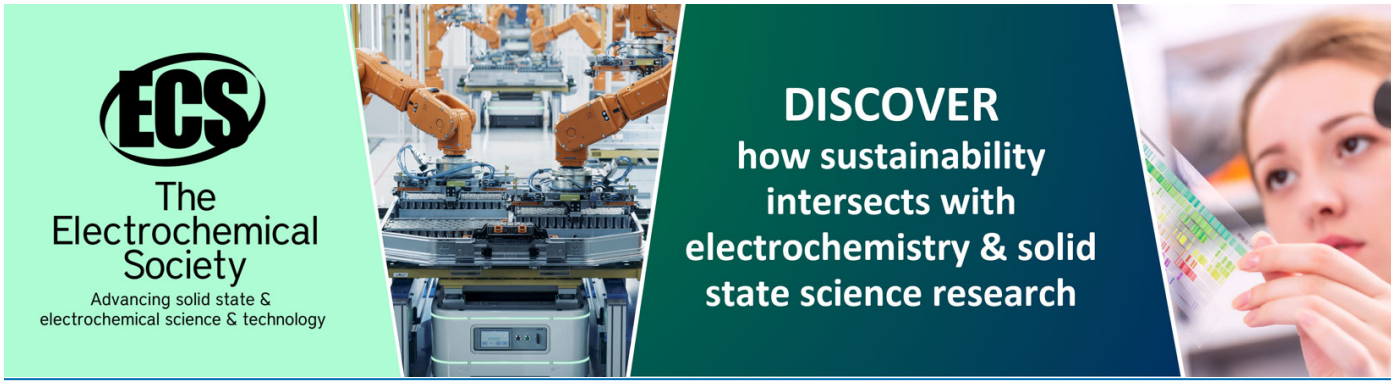
Innovative Techniques in Comparator Designs



Innovative Techniques in Comparator Designs

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Abstract. This paper presents four innovative designs of comparators proposed these years. A latch-type dynamic bias adds a tail capacitor to prevent fully discharging at the pre-amplifier output nodes to reduce energy consumption. The comparator is analysed and then compared with floating inverter amplifier (FIA) type. The pre-amplifier of the FIA type adopts an inverter-based input pair by a floating reservoir capacitor, greatly boosting gm/Id and improving the energy efficiency. The edge-pursuit comparator (EPC) provides a new perspective when designing comparators. According to the input difference, it will automatically adjust the comparison energy, avoiding wasting unnecessary energy spent on coarse comparison. Finally, for the edge-race comparator (ERC), it further improves the performance of saving energy and addressing the relatively long comparison time in the EPC.

1. Introduction

Comparators play a core role in bridging physical and digital worlds nowadays. As the development of highly integrated circuits such as biomedical implants and sensing devices in the daily life, the demand for low-power and lower noise analog-to-digital converter (ADC) is growing rapidly. Normally, 40% to 50% of energy consumed by ADCs can trace back to the power distributed to the comparators [1-3]. Meanwhile, low-voltage operation requires strict conditions on quantization noise. As a result, improving the energy efficiency becomes both critical and challenging to pursue high-performance digital integrated circuits.

Many reformative structures of comparators are proposed in the recent years. The innovations of the improved designs mainly focus on reducing energy consumption, lowering the decision delay, minimizing the inferred input noise, and optimizing the voltage gain. Based on the Elzakker's comparator, H. S. Bindra proposed the dynamic-bias latch-type comparator in 2018 [1, 4]. This new architecture greatly improved the energy efficiency by adding a tail capacitor to prevent fully discharging for the transistors. The noise performance of the dynamic-bias comparator was also ameliorated. In 2020, X. Tang proposed a comparator with the dynamic floating inverter amplifier (FIA) under 180-mm process [5]. It greatly reduced the influence of the process corner and the input common-mode voltage on the comparator performance. M. Shim brought an innovative structural design named edge-pursuit comparator (EPC) in 2017 [6]. By adjusting the comparison energy automatically with different input voltage, it greatly saved energy and optimizes the tunability with the input-referred noise. In 2020, H. Zhuang proposed the edge-race comparator (ERC) [7]. It compared the differential input voltage by generating two propagating edges in two inverter loops and measured the distance between them to determine the comparison result. This new architecture further reduced the energy consumption and resolves relatively long comparison time in previous designs.

This paper is organized as follow: in Section 2, compared with the conventional double tail latch type comparator, the advantages of the dynamic bias comparator proposed by H. S. Bindra are discussed [4]. Due to the existing trade-offs in dynamic bias comparator, further amended architecture presented by X. Tang will be indicted in Section 3 [5]. Section 4 provides a brand-new perspective with the edge-pursuit comparator proposed by M. Shim [6]. In Section 5, the performance of H. Zhuang's edge-race comparator will be analysed quantificationally [7]. Comparisons for all the four innovative designs are mentioned in Table I in Section 6. Finally in Section 7 concludes this paper.

2. Dynamic bias latch-type comparator

Based on the conventional double-tail latch-type comparator, M. Elzakker proposed a new as shown in figure 1 [1]. Only when the output common-mode voltage is lower than the threshold voltage of (M6/M7), the latch stage starts working. By this mechanism, pre-charge energy of the pre-amplifier stage is minimized, resulting in decrease in the energy consumption.

The proposed dynamic bias comparator not only further improves the energy efficiency but also optimizes the overhead issues compared to the previously proposed design "bi-directional dynamic comparator [2]. The dynamic bias comparator adds a tail capacitor M3b and a tail transistor M3a (as shown in figure 2) to control the discharge from nodes Di+ and Di-. When CLK=0, CTAIL is discharged to ground through M3b. When CLK=VDD, all reset transistors are turned OFF while M3a turns ON and capacitances on the drain nodes Di+ and Di- starts to discharge. This leads to the tail current charging the capacitor M3b and increase in the voltage VCAP, thus contributing to diminishing VGS of the differential part (M1/M2) and finally provides a dynamic bias for the differential pair.

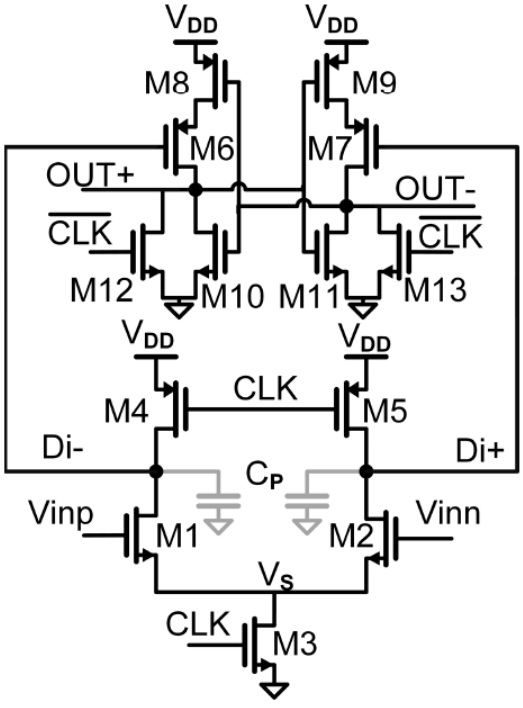

Figure 1. Circuit of Elzakker's comparator.

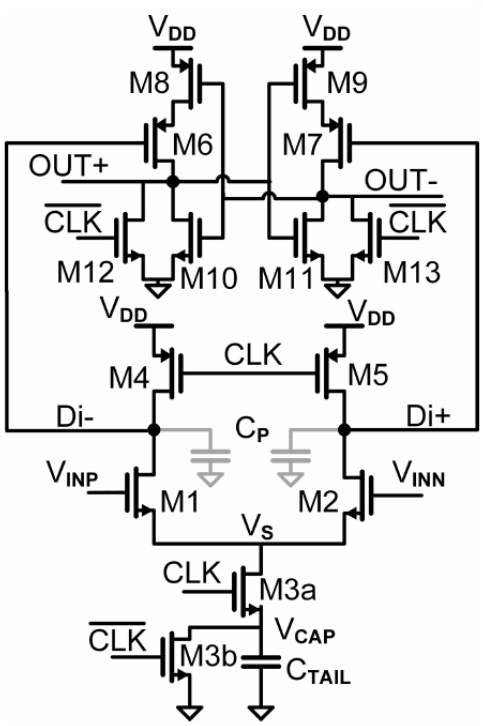

Figure 2. Circuit of the proposed dynamic bias comparator

The required energy for the preamplifier in the dynamic bias comparator to pre-charge the drain nodes is 2*Cp*VDD2-Cp*VDD*(VD1+VD2), which is lower than the conventional pre-charge energy for the 2*Cp*VDD2 in the case of Elzakker's comparator. Figure 3 indicates the lower power consumption of dynamic bias compared with Elzakker's latch.

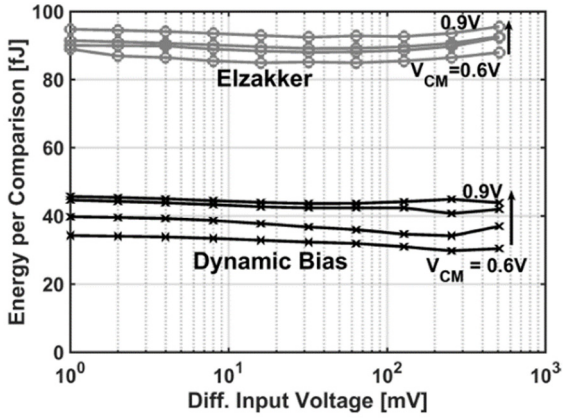

Figure 3. Energy consumption of dynamic bias and Elzakker's latch-type comparator across differential input voltage.

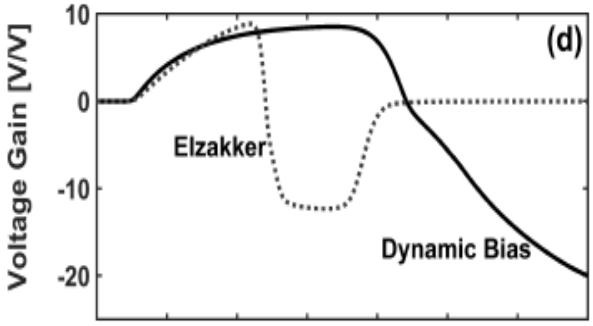

Figure 4. Simulated pre-amplifier differential voltage gain of the two comparators.

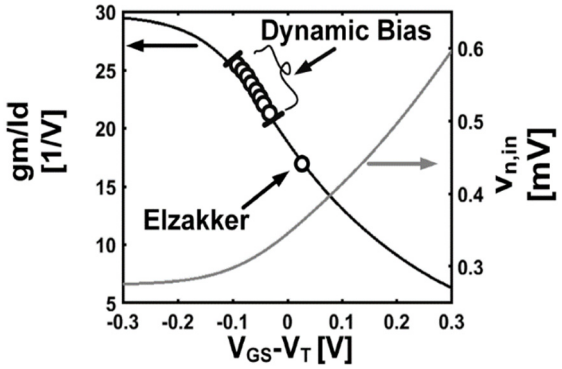

Figure 5. gm/Id and input noise voltage (calculated) versus Vov.

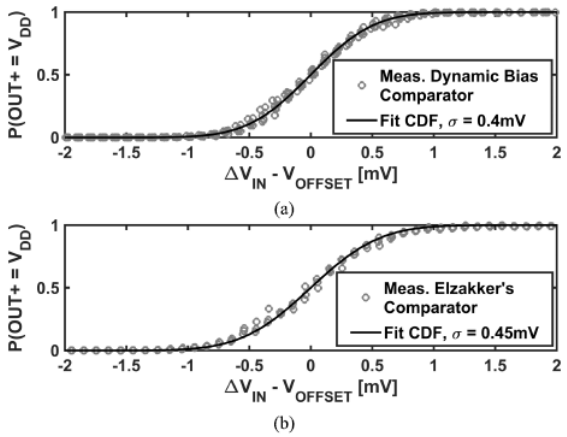

Figure 6. Measured cumulative probability density distribution and fit to Gaussian distribution for (a) dynamic bias comparator and (b) Elzakker's comparator.

As for the voltage gain of the dynamic bias comparator, the dynamic bias comparator performs more stable than Elzakker comparator, the result can be derived from figure 4. The detailed expression of voltage gain of dynamic bias can be written as

$$A_V(T_{\mathrm{INT}}) = \frac{C_{\mathrm{TAIL}}}{2n \cdot C_P} \frac{V_s(T_{\mathrm{INT}})}{\frac{kT}{q}} \tag{1}$$

Where $V_s(T_{\mathrm{INT}})$ is

$$V_s(T_{\mathrm{INT}}) = \frac{2 \cdot \Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}}) \cdot C_P}{C_{\mathrm{TAIL}}} \tag{2}$$

The maximum drop in $\Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}})$ is

$$\Delta V_{\mathrm{Di,CM},max} = \frac{C_{\mathrm{TAIL}}}{C_{\mathrm{TAIL}} + 2 \cdot C_P} V_{\mathrm{DD}} \tag{3}$$

From the expressions, it can be observed that the Di nodes do not fully discharge to ground even under the extreme conditions. Therefore, the conclusion that dynamic bias comparator is more energy efficient than Elzakker's comparator can also be proved.

In addition to the optimization in energy consumption, the proposed dynamic bias comparator also performs better than Elzakker's comparator in thermal noise contribution of the differential pair. The input-referred noise of the pre-amplifier in Elzakker's comparator in the strong inversion operation can be calculated for

$$E\left[v_{\mathrm{n,SI,in}}^2(T_{\mathrm{INT}})\right] = \frac{4kT\Upsilon}{C_P \cdot \Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}}) \cdot \left(\frac{g_m}{I_{\mathrm{CM}}}\right)_{\mathrm{SI},T_{\mathrm{INT}}}} \tag{4}$$

Where $\Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}})$ is

$$\Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}}) = \frac{I_{\mathrm{CM}} \cdot T_{\mathrm{INT}}}{C_P} \tag{5}$$

Meanwhile, under the weak inversion operation the noise of the dynamic bias pre-amplifier can be derived as

$$E\left[v_{\mathrm{n,WI,in}}^2(T_{\mathrm{INT}})\right] = \frac{2nkT}{C_P \cdot \Delta V_{\mathrm{Di,CM}}(T_{\mathrm{INT}}) \cdot \left(\frac{g_m}{I_{\mathrm{CM}}}\right)_{WI,T_{\mathrm{INT}}}} \tag{6}$$

Where Cp is the capacitor at the pre-amplifier's output nodes, gm is the transconductance of M1 and M2 and ICM is the current through M1 and M2.

From formula (4) and (6), it can be observed the input-referred noise is generally inversely proportional to gm. So larger gm or smaller VGS can ameliorate the performance of both comparators. Figure 5 shows the relationship between gm/Id with the overdrive voltage V_{OV} of the two comparators. When V_{OV} decreases, the input-referred noise also reduces. The increasing Vs ensures the gm/Id of dynamic bias comparator at the integration time is higher than that of Elzakker's comparator. In addition, it can also be observed that for the dynamic bias, the overdrive voltage lies in the weak inversion region where Vov is lower than 0V, so gm/Id for the dynamic bias comparator raises for about 25% compared to Elzakker's comparator. Moreover, figure 6 shows the rms input referred noise of the dynamic bias comparator is 0.4 mV and the Elzakker's comparator is 0.45mV when fitting the measurements to a Gaussian CDF

However, the performance of CLK-Q delay of the dynamic comparator is not that satisfactory. The results for both comparators are shown in figure 7, and it can be concluded that the dynamic bias comparator is more sensitive to the change of the input common-mode voltage than Elzakker's comparator. This problem is improved by the architecture discussed in Section 3.

3. Floating inverter pre-amplifier comparator

X. Tang proposed an energy-efficient dynamic comparator with a floating inverter amplifier (FIA)-based pre-amplifier, as shown in figure 8. It comes from the further modification of CMOS DB integration pre-amplifier shown in figure 9 by connecting two tail capacitors and replacing with C_{RES}. The presence of the FIA is because CMOS DB integration is infeasible in the extreme corner like SF, where nMOS is in the slow corner while pMOS is in the fast corner. FIA comparator fixes this problem and to ensure the input-output current for C_{RES} to be the same. Take the SF corner as an example, the comparison result is shown in figure 10.

The integration gain of the FIA can be expressed as

$$A_V(T_{\mathrm{INT}}) = \frac{2 \cdot C_{\mathrm{RES}} \cdot \Delta V_S(T_{\mathrm{INT}})}{n \cdot C_X \cdot U_T} \tag{7}$$

Where $\Delta V_S(T_{\mathrm{INT}})$ is the source voltage change at the integration time, also the input referred noise at the integration time can be calculated

$$\sigma^2_{in,\mathrm{FIA}}(T_{\mathrm{INT}}) = \frac{2nkT}{C_{\mathrm{RES}} \cdot \Delta V_S(T_{\mathrm{INT}})} \cdot \frac{I_D}{G_m} \tag{8}$$

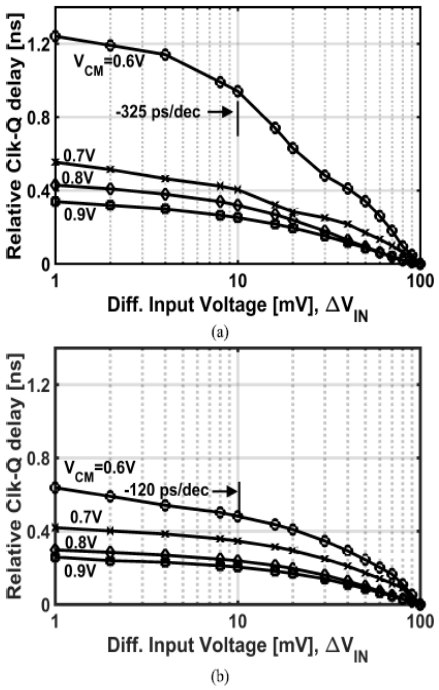

Figure 7. Relative CLK-Q delay measured for the (a) dynamic bias comparator and (b) Elzakker's comparator for various V_{CM}.

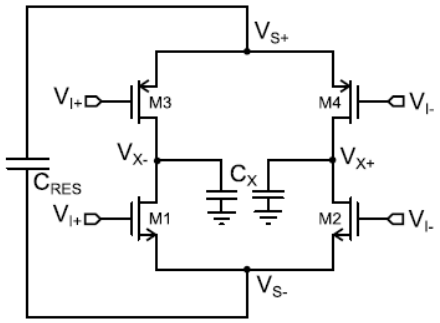

Figure 8. Proposed CMOS DB integration model.

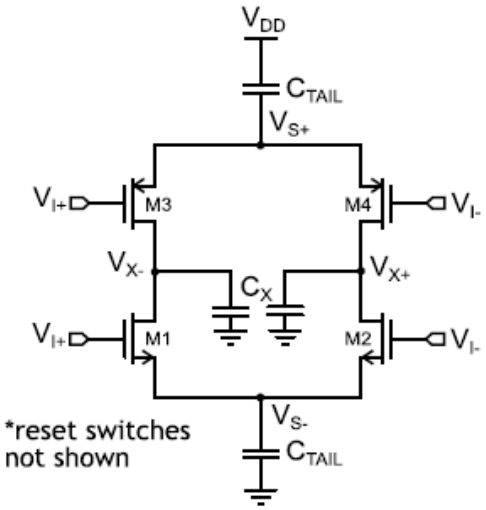

Figure 9. Proposed CMOS DB integration model.

The fundamental trade-off between energy consumption and thermal noise is described as the parameter FoM (figure of merit). It is defined as the product of energy consumption and the input-referred noise power. The energy efficiency improvement of FIA can be calculated as

$$\frac{FoM_{SA}}{FoM_{FIA}} = \frac{V_{\mathrm{DD}}}{V_{\mathrm{THN}}} \cdot \frac{(G_m/I_D)_{\mathrm{FIA}}}{(g_m/I_D)_{\mathrm{SA}}} \tag{9}$$

The equation indicates two main advantages of the proposed FIA. First, the coefficient (VDD/VTHN) comes from the circumvent of fully discharging the integration capacitor. Besides, ratio of gm/Id for the two kinds of pre-amplifiers is about 2.5, thus predicts the higher energy-efficiency and lower input-referred noise in the FIA structure. Figure 11 and figure 12 are the simulation results and proves the previous conclusion.

As described before, the design mainly solves the relatively long CLK-Q delay time from the nMOS DB integration pre-amplifier. Figure 13 shows the simulation of CLK-Q delay with 1-mV differential input and energy efficiency of the proposed comparators with different choices of CRES values. Figure 13(a) indicates that when the choice of CRES lies between 1pF to 3.5pF, the absolute value of the rate of change in simulated CLK-Q delay is large and it becomes mild when coming to 3.5pF to 5pF region. Figure 13(b) shows when the CRES value is chosen between 2pF to 3.5pF the simulated FoM is enough to suppress the latch stage noise for avoiding the degradation of comparator precision. Besides large CRES will lead to the reduction in the dynamic bias effect and diminish gm/Id. By reason of the foregoing, X. Tang chooses 2-pF CRES to reach the balance between energy efficiency, comparison speed and area consumption.

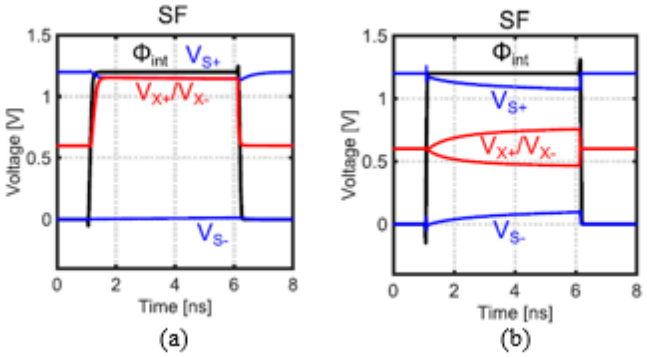

Figure 10. Behavior Simulation at SF corner for (a) pre-amplifier and (b) FIA.

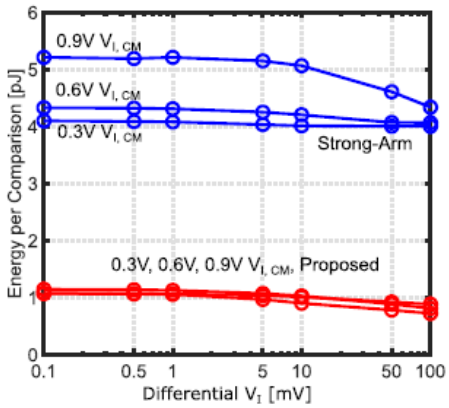

Figure 11. Measured energy consumption versus input voltage for the SA latch and proposed comparator.

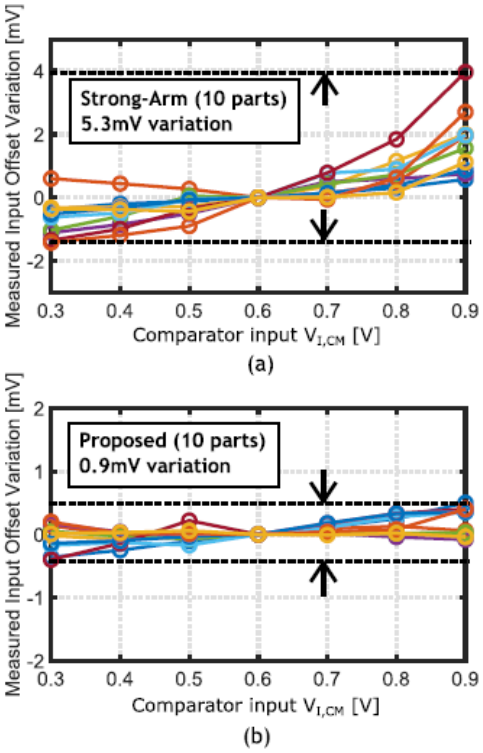

Figure 12. Measured ten-part input-referred offset versus input CM voltage for (a) SA latch and (b) proposed comparator.

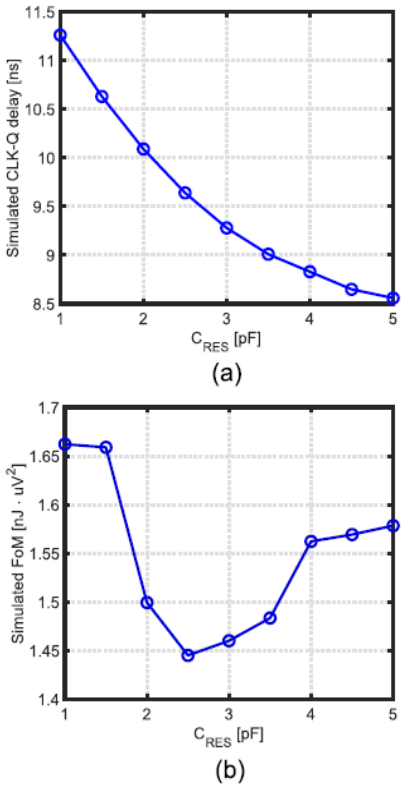

Figure 13. Simulated (a) CLK-Q delay with 1-mV differential input and (b) energy efficiency of the proposed comparator.

After choosing the applicable CRES, figure 14 presents that the simulated CLK-Q delay of the proposed comparator is much more stable than the previous strong-arm design. Also, when using higher input common-mode voltage, CLK-Q delay is even lower.

Figure 15 describes the measured cumulative probability density distribution and fit to Gaussian distribution for both proposed comparator and SA latch. The result reveals that FIA reduces the noise variation by four times due to its input common-mode-insensitive operation compared with the traditional architecture. The comparison of strong-arm and proposed type is shown in figure 16. It indicates that with the same common-mode input voltage, the input noise of the proposed type is about

25% lower when $V_{I,CM}$ is 0.3-0.6V. Apart from that, with the input voltage increasing, the FIA type comparator shows more stable performance for the changes in the measured input noise is much lower than that of the strong-arm type.

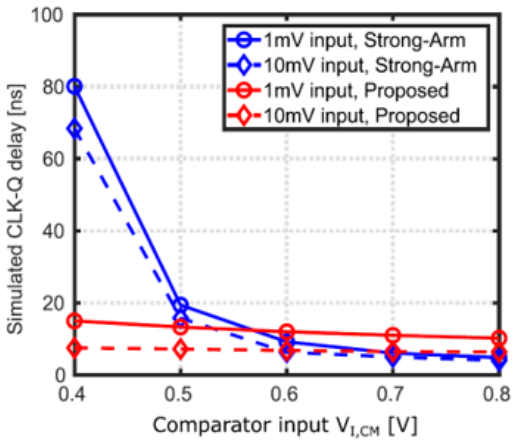

Figure 14. Simulated CLK-Q delay versus input common-mode voltage.

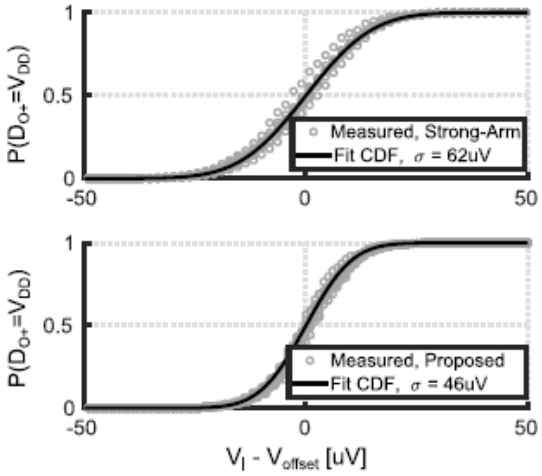

Figure 15. Measured cumulative probability density distribution and fit to Gaussian distribution for proposed comparator and SA latch with 1.2-V supply and 0.6-V input common-mode voltage.

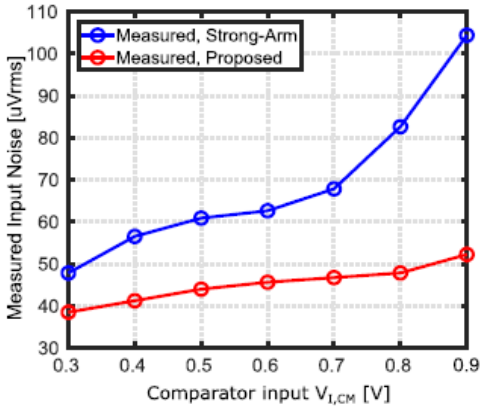

Figure 16. Measured input-referred noise versus input common-mode voltage for the SA latch and proposed comparator.

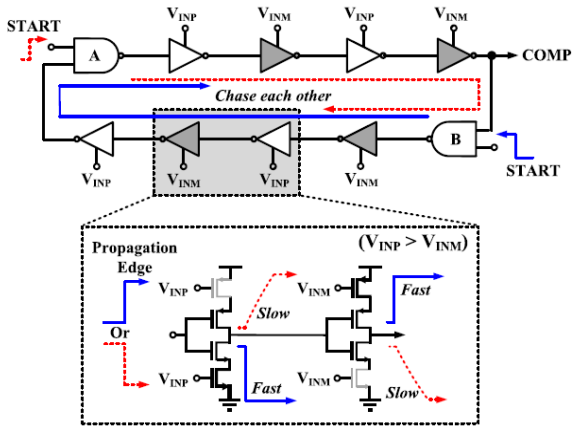

Figure 17. Structure of the EPC.

4. Edge-pursuit comparator

By changing the comparison energy automatically according to the input difference to save energy, M. Shim proposed an innovative comparator named edge-pursuit comparator (EPC) in 2017 [6]. This new structure is composed of two NAND gates and several inverter delay cells as shown in figure 17. When the comparator initiates with the signal START goes high at both NAND gates, two propagating edges will be injected into the oscillator and then travel around the comparator. By increasing V_{INP}, one edge will propagate faster (and vice versa for V_{INM}), resulting in the oscillation collapses and indicating the slower edge is overtaken. Therefore, the logic level is set to either V_{DD} or GND. For large voltage differences, the oscillation collapses quickly, reducing the energy consumption for coarse comparisons. By this methodology, the comparator not only optimizes the energy dissipation but also realizes high accuracy.

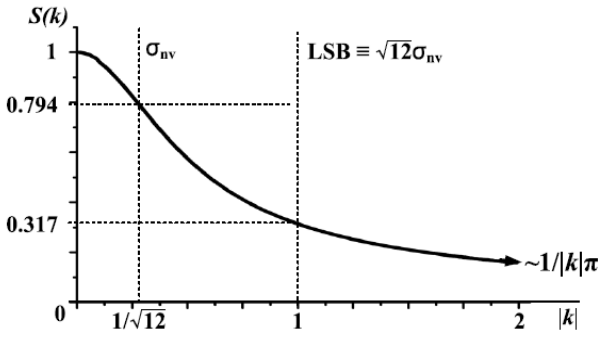

Figure 18. EPC's scaling factor S(k).

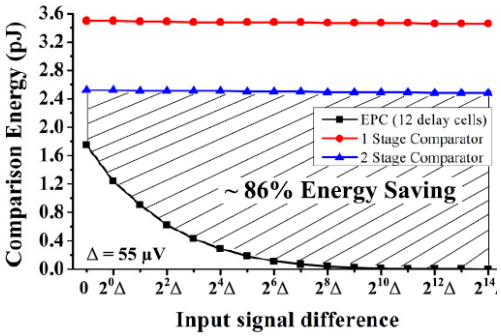

Figure 19. Comparison of simulated comparator performance among EPC and conventional comparators for energy.

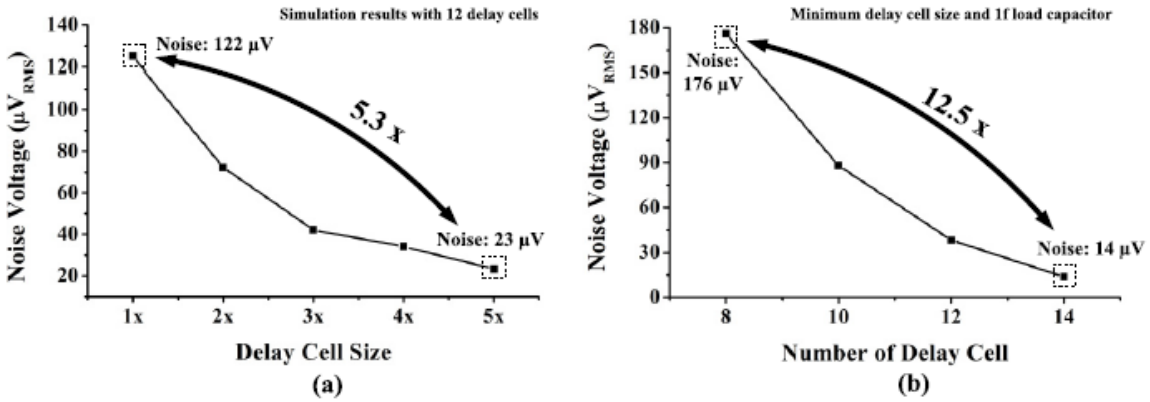

Figure 20. Simulated input-referred noise versus (a) delay cell size and (b) number of delay cells.

By analysing quantitatively, the average energy consumption per comparison for EPC is

$$E = 2IV_{\mathrm{DD}}\frac{\pi^2}{\Sigma}S\left(\frac{M}{\Sigma}\right) \tag{10}$$

Where M and Σ are the "drift" and "diffusion" coefficients of this random process defined as

$$M \equiv \frac{\mu\Delta\phi}{\tau} = 4\pi f_0\frac{v_{\mathrm{in}}}{V_{\mathrm{ov}}} \tag{11}$$

$$\Sigma \equiv \frac{\sigma_{\Delta\phi}^2}{\tau} = 8\pi^2 f_0^2\frac{kT}{I}\left(\frac{2}{V_{\mathrm{ov}}}(\gamma_N+\gamma_P)+\frac{2}{V_{\mathrm{DD}}}\right) \tag{12}$$

Also, the scaling factor, which is dependent on the ratio M/Σ, is defined as

$$S(k) \equiv \frac{\tan h\,(k\pi)}{k\pi} \tag{13}$$

The function S(k) decreases as |k| becomes larger, reflecting the automatic energy scaling behaviour of EPC comparator. Figure 18 shows the scaling factor S is about 1 when Vin is at the noisy region. In contrast, it will decrease rapidly towards 0 when it is out of the noisy region. As a result, the comparator can save approximately all the energy in most of the voltage regions except for the small noisy region.

To evaluate the EPC's energy efficiency compared with other comparators, a norm is defined as

$$N \equiv E \times \frac{\sigma_{v_n}^2}{V_{\mathrm{DD}}^2} \tag{14}$$

The formula illustrates the energy consumption per SNR assuming maximum signal power is VDD2. After deriving the expression for EPC comparator, single-stage comparator and two-stage comparator [8-9]. The ratios among those norms are

$$N_{\mathrm{EPC}}: N_{\mathrm{SS}}: N_{\mathrm{TS}} = S\left(\frac{A}{B}\right)\frac{\pi^2/3}{V_{\mathrm{DD}}}: \frac{7}{V_{\mathrm{th}}}: \frac{4}{V_{\mathrm{th}}} \tag{15}$$

According to (15), the EPC has relatively smaller norms than the other two kinds of comparators even when the input voltage and scaling factor do not benefit the EPC at Vin = 0 and S = 1. The simulation result for the three comparators is shown in figure 19. It demonstrates that with similar input signal difference and overdrive voltage V_{OV}, the EPC shows much better performance by saving energy for 86% compared to the other two types. Apart from that, distinguishing from the other two types with constant energy consumption. Figure 19 also illustrates the EPC saves energy through automatic energy scaling.

In addition to energy saving, the design also shows great performance in input noise tunability. The noise rms level σ_{Vn} can be expressed as

$$\sigma_{v_n} = \sqrt{\sigma_{v_n}^2} = \frac{\pi}{\sqrt{3}} f_0 \frac{kT}{I}\left(\frac{2}{V_{\mathrm{ov}}}(\gamma_N + \gamma_P) + \frac{2}{V_{\mathrm{DD}}}\right) V_{\mathrm{ov}} \tag{16}$$

Figure 20(a) shows that with the increase in delay cell size, the noise rms level approximately follows the inverse of the total capacitance. As shown in figure 20(b), due to the positive feedback the noise change is more sensitive than expected. This positive feedback will affect more with less stages and this is alike to the regeneration of the output signal in traditional comparators. Nevertheless, it does not consume much energy while the conventional comparators consume a fixed amount of dynamic energy. Therefore, the positive feedback further increases the tuneable noise range and even with few stages, the EPC comparators can still exhibit better energy efficiency.

In summary, the proposed edge-pursuit comparator is an innovative structural design which dramatically improves the energy efficiency and tunability with input-referred noise compared with the conventional comparators with an automatic energy scaling capability according to the input difference. This new design is different from the conventional SA latch + pre-amplifier structure, it measures the phase difference between the two input edges and then determine the comparison result. It provides a new perspective for the designers when improving the performance of comparators.

5. Edge-race comparator

In Section 4, the proposed EPC improves the energy efficiency and input-referred noise greatly compared with the conventional comparators [6]. However, it has limitation that in fine comparisons, the large delay is not negligible. In 2020, H. Zhuang proposed a novel voltage comparator named edge-race comparator (ERC) which overcomes this limitation, saving significant energy ad time in comparisons. As can be seen in figure 21, ERC consists of inverter delay units and NAND gates.

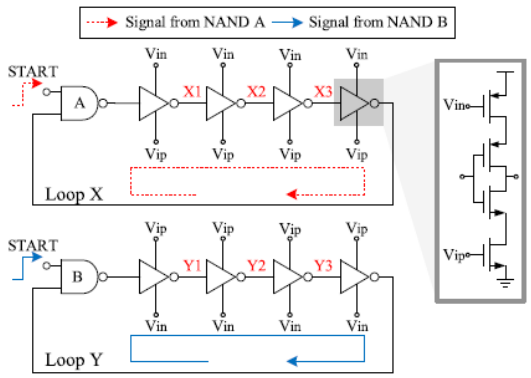

Figure 21. The ciurcuit of proposed ERC.

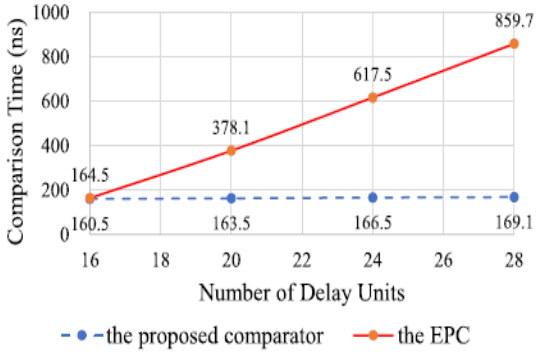

Figure 22. Number of delay units versus comparison time.

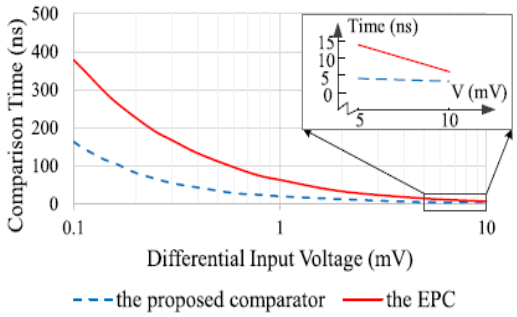

Figure 23. Comparison time versus differential input voltage.

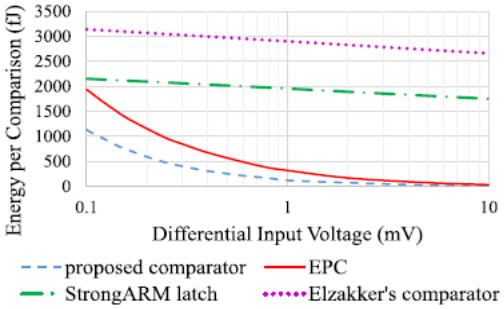

Figure 24. Energy per comparison at the same 50-μV input-referred noise.

When START rises to high, two propagating edges are generated by the two NAND gates, and they then start to race with each other. Due to the different propagating speed, the distance between them will gradually increases and finally reaches a pre-set value d0. Afterwards the comparison stops, and the comparison result is determined by the winner. The pre-set value d0 is 2 inverter delays which is 2.5 time smaller than that of the EPC, which is 5 inverter delays, thus the proposed type will have much faster comparison speed. The comparison time for both EPC and ERC can be calculated as follows:

$$t_{\text{comp}} \approx \frac{C_{\text{L}} V_{\text{DD}} d0}{g_{\text{m}}\left(V_{\text{ip}} - V_{\text{in}}\right)} \tag{17}$$

Where C_L is the load capacitance of each delay unit and gm is the transconductance of the transistor connected to V_{ip} or V_{in}. Figure 22 describes the delay time performance for ERC and EPC with different number of delay units. It can be observed that the ERC comparator is both shorter and more stable under different amounts of delay units than EPC type at V_{ip}-V_{in} = 0.1 mV. In figure 23, with the differential input voltage increasing, the result also reveals the better time delay performance of the proposed comparator. The comparison time is inversely proportional to the differential input and the time of the ERC comparator is 2 times smaller than the EPC type.

Apart from the faster comparison speed, the proposed ERC comparator also greatly optimizes the energy efficiency. Figure 24 demonstrates the energy consumption of 4 different types of comparators at the same 50-μV input-referred noise. As can be found that the StrongARM latch and the Elzakker's comparator consume relatively constant high energy. Meanwhile, the ERC and EPC can effectively adjust the energy with various differential input voltage and significantly save the energy consumption.

To further compare the performance between the ERC and EPC type, a norm for comparison is defined:

$$\mathrm{NM} \equiv t_{\mathrm{comp}} \times E_{\mathrm{comp}} \times \sigma^2_{\mathrm{n\_comp}} \tag{18}$$

In the norm ratio, the comparison between the EPC and ERC is given as follows:

$$\mathrm{NM_{EPC}}:\mathrm{NM_{ERC}} = d0_{\mathrm{EPC}}: (1.42 \cdot d0_{\mathrm{ERC}}) \tag{19}$$

When there are 20 inverter delay units, $d0_{EPC}$ is 11 inverter delays while $d0_{ERC}$ is 2 inverter delays. Under this circumstance, the norm ratio is 11:2.84 and shows that the ERC comparator is approximately 4 times better than the EPC type.

Moreover, the input-referred noise analysis should also be noticed. Assuming each loop is equivalent to a voltage-controlled inverter chain, the input-referred root mean square (rms) can be expressed as:

$$\sigma_{\mathrm{n}} = \frac{1}{\sqrt{N \cdot C_{\mathrm{L}}}} \frac{2I_{\mathrm{SS}}\sqrt{\alpha kT}}{V_{\mathrm{DD}} g_{\mathrm{m}}} \tag{20}$$

Because the EPC comparator has a longer comparison time, it performs noise averaging, for which reason the EPC should have a smaller input-referred noise than the ERC. However, as shown in the simulation result, the EPC has much larger noise than the ERC under 16 and 20 delay units. This comes from the coupling of parasitic capacitance, degrading the noise performance.

Table 1. Comparison of the four comparators.

	[4]	[5]	[6]	[7]
Process [nm]	65	180	40	40
Architecture	Dynamic Bias	Proposed FIA+SA	SAR (EPC)	SAR (ERC)
Energy [pJ]	0.034	0.98	0.2	0.1
Noise [μV]	400	46	65	74
Area [μm^2]	125	9800	315000	-
Comparison Time [ns]	-	-	63.1	19.9

6. Comparison result

Table 1 summarizes the measured performance of the four reviewed comparators, and they all have outstanding performance in a certain field. The comparator with dynamic floating inverter amplifier has the smallest input referred noise. The Dynamic Bias Latch-Type Comparator has the lowest energy consumption per comparison. These two different comparators are designed based on the conventional latch-type comparators. Due to the process of the FIA, the size of it is inevitably large. However, it resolves the relatively high noise lies in the dynamic bias comparator also stays in low level of energy consumption compared to the conventional comparators [9, 10]. Thus, they are all outstanding reformative designs. Besides, the idea of EPC is innovative, distinguishing from the traditional designs, it does comparisons by measuring the phase difference between two input edges. The performance of EPC is very impressive, it reaches both high energy efficiency and low input referred noise. ERC can be treated as the modification for the EPC comparators. It comprehensively improves the performance compared with the EPC especially for the comparison time. That is because it only needs two inverter delays during comparison thus greatly optimizing time efficiency. Also, as the development of manufacturing process, the overall performance in energy efficiency and input referred noise is getting better.

7. Conclusion

This paper presents four innovative designs dynamic-bias comparator, comparator with dynamic floating inverter amplifier, edge-pursuit comparator, and edge-race comparator. All these new designs improve the energy efficiency and input-referred noise performance. There exist trade-offs when designing, so these four innovative designs can meet various requirements. The modifications methodology of the dynamic bias and FIA comparators are based on gm/Id, which uses the voltage overdrive V_{OV} as the key parameter and it is strongly related to the performances of analog circuits, giving an indication of device operating region and tools for calculating the transistors dimensions. For the EPC and ERC comparators, they provide a brand dimension when designing comparators, measuring the phase difference between input edges and scale automatically to various input voltages. The new perspective of these kinds of innovations will inspire a lot for designers and is valuable when exploring new ways to optimize the devices' performance.

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