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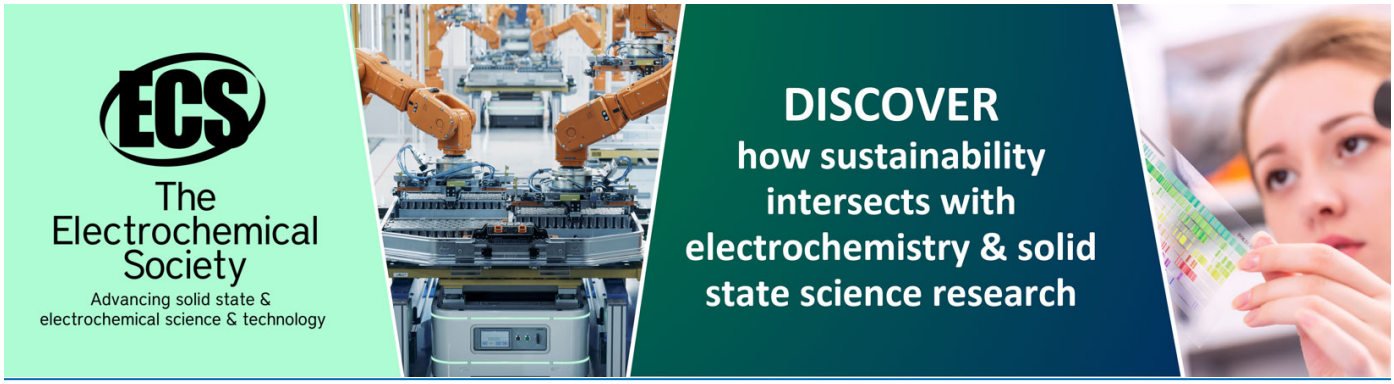

Design of high voltage electrostatic protection device for CAN bus

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Abstract: The Dual-Direction Silicon Controlled Rectifier (DDSCR) device has dual-direction electrostatic protection function and strong current discharging ability, which is widely used in ESD on-chip protection. In this paper, a high performance symmetric high voltage Dual-Direction Silicon Controlled Rectifier with floating P+ (HVDDSCR_FP+) is designed for CAN bus under 0.18 μm BCD process. In order to predict and verify the ESD performance of the device, TCAD two-dimensional device simulation and Transmission Line Pulse (TLP) test system were used. The experimental results show that the HVDDSCR_FP + structure has not only symmetrical positive and reverse I-V curves, but also the characteristics of high holding voltage and high failure current. Compared with the traditional HVDDSCR, HVDDSCR_FP+, at 25V forward and reverse trigger voltages (V_t), has increased its holding voltage (V_h) from 12V to 20V, failure current (I_{t2}) from 5A to 35A. In the actual tape-out process, it is found that the width of the N-well has a great influence on the performance of the device. After analyzing the reason and improving it, the leakage current of the device is reduced from μA level to nA level.

1 Introduction

With the rapid development of electronic technology, automobile electronization is increasingly growing faster and higher. Harsh application environments and complex electronic systems bring great challenges to the design of on-chip electrostatic discharge (ESD) protection [1-3]. ESD protection of automotive communication ports usually requires high holding voltage (V_h) to avoid circuit latch-up and high failure current (I_{t2}) to have good ESD robustness [4-6]. In practical electrostatic protection schemes, transient voltage suppressor (TVS) devices integrated on the chip are generally used. TVS devices have the advantages of high temperature resistance, high voltage resistance, small parasitic capacitance and fast response speed in electrostatic protection. Among them, the silicon controlled rectifier (SCR) is a very attractive choice, and the dual-directional silicon controlled rectifier (DDSCR) provides bidirectional ESD protection for circuits in compact devices. However, its high trigger voltage makes SCR prone to core damage and low holding voltage leads to latch-up issue , which is an urgent problem to be solved in the industry [7]. The holding voltage of high voltage SCR is usually dependent on the doping concentration and depth of substrate, P-epi and NBL, but this adjustment has

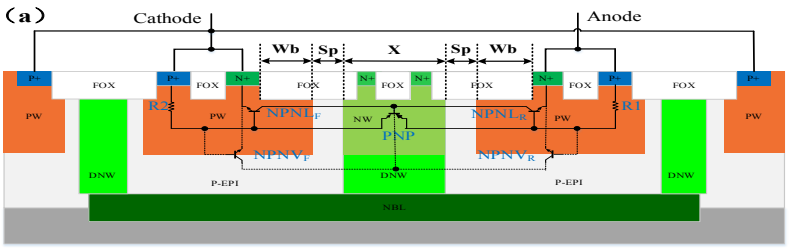
great limitations. At present, the proposed holding voltage improvement technology includes the insertion of floating N+ in the N-well [8] and segmented emitter layout [9][10]. These technologies improve the holding voltage (V_h) to a large extent, but significantly reduce the failure current (I_{t2}), which also increases the difficulty of design. Literature [11] analyzed and verified that the holding voltage (V_h) and failure current (I_{t2}) of DDSCR could be significantly increased by adding N-type buried layer. Literature [12] introduces an asymmetric DDSCR structure, in which a floating P+ is inserted into the P-well of the device, and its holding voltage and failure current are greatly improved. This provides a great design scheme for designers to optimize the holding voltage and failure current of devices.

In this paper, symmetric HVDDSCR devices were studied under 0.18 μm BCD process. In order to achieve the design purpose of high holding voltage and high failure current, the structure and working mechanism of HVDDSCR_FP+ are proposed and discussed on the basis of traditional symmetric HVDDSCR devices, and the effect of the width of N-well in the structure on the performance of HVDDSCR_FP+. The theoretical analysis is carried out by using TCAD two-dimensional simulation software. The performance of the device was verified by tape-out and transmission line pulse test (TLP).

2 Device structure and working mechanism

The cross-section view of a conventional symmetric HVDDSCR device is shown in Fig.1 (a). Either the cathode or the anode has the lateral parasitic transistor NPN ($NPNL_F$ or $NPNL_R$) with N-well as collector and the vertical parasitic transistor NPN ($NPNV_F$ or $NPNV_R$) with N-type buried layer (NBL) as collector. Forward SCR path is composed of P-well resistors R1 and R2, parasitic transistor PNP, $NPNV_F$ and $NPNL_F$. The equivalent circuit of forward SCR is shown in Fig.1 (c). The reverse SCR path consists of P-well resistors R2 and R1, parasitic transistor PNP, $NPNV_R$ and $NPNL_R$, and the equivalent circuit of reverse SCR is shown in Fig.1 (d). The distance between PW and NW was denoted as Sp, the distance between the N+ and the breakdown surface was denoted as Wb, and the width of the N-well in the middle of the device was denoted as X.

The symmetrical HVDDSCR is completely symmetrical in structure and can discharge current in both positive and negative directions. As shown in Fig.1 (a), when the anode of HVDDSCR receives ESD forward pulse and reaches the breakdown voltage at the breakdown surface, avalanche breakdown will occur in N-well and P-epi, which will generate a large number of electron-hole pairs and the holes will reach the cathode P+ of the device through P-epi resistance R2. As the number of holes increases, the junction voltage V_{be} derived from the base and emitter of $NPNV_F$ and $NPNL_F$ will increase gradually. When V_{be} increases to 0.7V, $NPNV_F$ and $NPNL_F$ will turn on. The parasitic transistor $NPNV_F$ and $NPNL_F$ provide current to the base of the parasitic transistor PNP after opening, making the parasitic transistor PNP turning on. A positive feedback mechanism will be formed between the two kinds of parasitic transistor, making the device in the latch-up state, and the device begins to release the current. Current discharge path P1 is composed of the $NPNL_F$ and the parasitic transistor PNP, and path P2 is composed of the $NPNV_F$ and the parasitic transistor PNP, forming forward SCR paths P1 and P2, as shown in Fig.1 (c). The working mechanism of the reverse path is the same as that of the forward path.



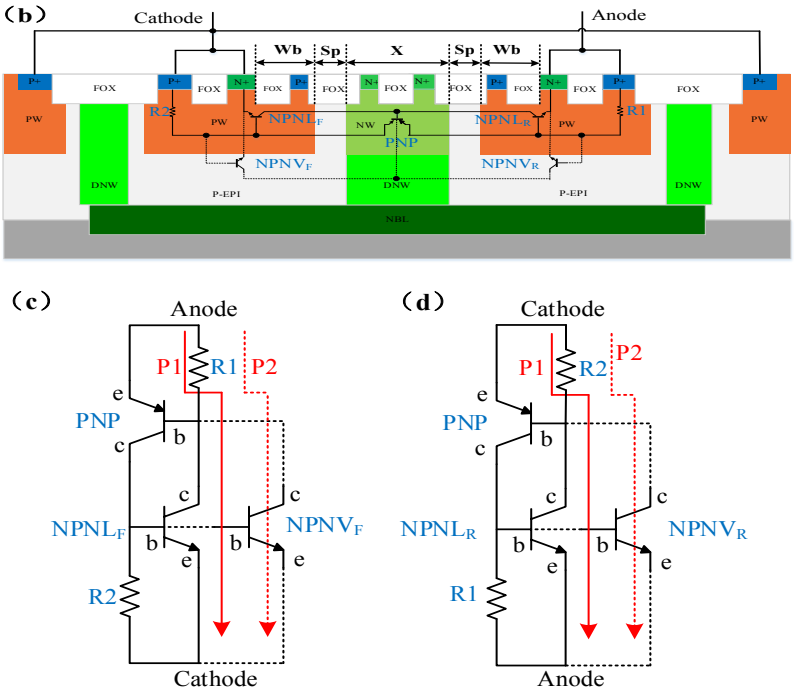


Fig.1 (a) Cross-section view of the HVDDSCR ; (b) Cross-section view of the HVDDSCR_FP+; (c) Forward equivalent circuit; (d) Reverse equivalent circuit.

In the traditional symmetric HVDDSCR structure, because of the deep N-type buried layer (NBL), the width of the base of the vertical parasitic transistor NPNV is much wider than that of the lateral parasitic transistor NPNL, so the current amplification factor β of the parasitic transistor on the lateral path is larger. The current discharge path P1 is the main discharge path, and P2 is the second path. Widening the distance of the Wb can increase the lateral parasitic transistor NPNL base of effective width, inhibite the lateral current amplification factor β, nominate the discharge current path (P2) as main discharge path. It makes the discharge path longer and hence holding voltage higher. The wider the Wb gets, however, the larger the chip area will be, which contributes to the device improperly working.Therefore, the symmetric HVDDSCR_FP+ structure studied in this paper is to insert floating P+ at the Wb position of the traditional symmetric HVDDSCR structure. The purpose is not to increase the lateral size of the device, make P2 the main current release path, and improve the performance of the device. The cross-section view of symmetric HVDDSCR_FP+ is shown in Fig. 1(b), and its equivalent circuit diagram is the same as that of traditional symmetric HVDDSCR, as shown in Fig. 1(c) and (d).

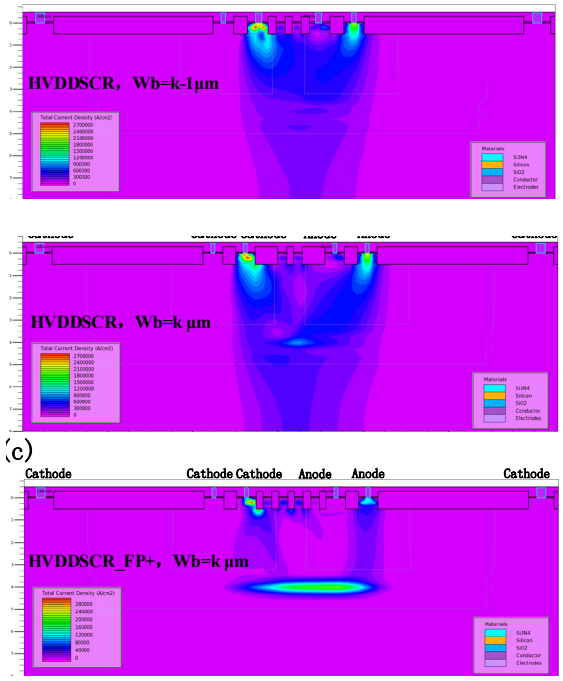


Fig.2 TCAD simulated forward current density in the HVDDSCR, Wb=k-1μm (a) and the HVDDSCR, Wb=k μm (b) and the HVDDSCR_FP+, Wb=k μm (c), under 0.1A forward current pulse.

3 TCAD simulation analysis

3.1 Performance simulation of HVDDSCR and HVDDSCR_FP+ devices

Through transient simulation of TCAD, HVDDSCR with Wb as K-1 μm and Wb as K μm and HVDDSCR_FP+ with Wb as K μm were simulated to study the working mechanism of the device. A square wave current pulse similar to TLP was applied to the anode with a pulse amplitude of 0.1A and a pulse duration of 100ns, and the cathode was grounded. Fig. 2 (a) When the Wb of HVDDSCR is K-1 μm, the current is mainly emitted by the SCR path P1 formed by the $NPNL_F$ and the parasitic transistor PNP. Fig. 2 (b) When the Wb of HVDDSCR is K μm, the current begins to go deep into the buried layer of the device, and the SCR path P2 is released by the $NPNV_F$ and the parasitic transistor PNP. Fig. 2 (c) shows the HVDDSCR_FP+ with Wb as K μm. It can be observed more significantly that a large amount of current is concentrated in the buried layer.

The Widened Wb increases the effective base width of the NPNL and inhibits the current amplification factor β of the NPNL. The current discharge move toward the vertical parasitic path inside the device rather than toward the surface of the device. However, when floating P+ is inserted into the device, the current path walk deep inside the device, causing the main current discharge path to change from P1 to P2. P2 has a longer current path and thus the device obtains a higher holding voltage. Its mechanism can be explained from the following two aspects:

1) Under the action of transient forward electrostatic pulse, because floating P+ and Ground have the same potential, floating P+ will block part of the electron flow from the emitter (N+) to the collector (NW) in the $NPNL_F$, and the current will flow deeper into the device, resulting in a longer current path and a higher holding voltage.

2) When floating P+ is inserted into the P-well, the base width and the base doping concentration of the NPNL increase, resulting in a decrease of the current amplification factor β of the NPNL, and the current discharge path P2 becomes the main path, resulting in a higher holding voltage of the device [13].

3.2 Effect of N-well width X in HVDDSCR_FP+ on device performance

It can be seen from the cross-section view of HVDDSCR_FP+ device that the N-well and the deep N-well in the middle of the device (the width of the N-well and the deep N-well is the same) play a role of isolation in the structure. In ideal scenario, no current should flow from anode to cathode until the device has reached the trigger voltage, and in practical applications, the leakage current of the device is generally required to be nA level. TCAD two-dimensional device simulation software was used to simulate HVDDSCR_FP+ structure X is t μm and 2t μm respectively. Fig. 3 shows the current density distribution of the device when the N-well is not broken down. When the width of the N-well X is t μm, due to the depletion of PN junction, a small amount of current will pass through the N-well before breakdown, resulting in large leakage current of the device, which leads to the device cannot be used properly. The position of device penetration due to depletion is marked with red circles in Fig. 3 (a). When the width of the N-well X is 2t μm, the device is not penetrated when the N-well is not broken down, which is also marked with red circle in Fig. 3(b). For HVDDSCR_FP+ , the smaller the X distance, the narrower the base width of the parasitic transistor PNP, the larger the current amplification factor β, and the SCR formed with the parasitic transistor NPN is easier to open, but the

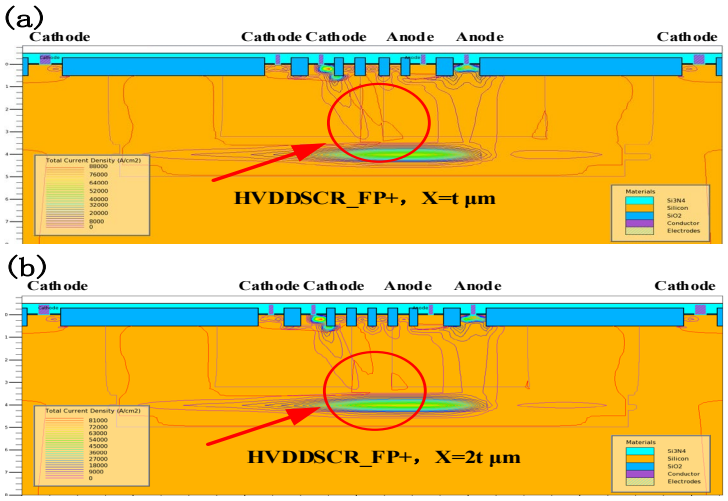


Fig.3 TCAD simulated forward current density in the HVDDSCR_FP+ （a）X=t μm（b）X=2t μm, under 0.1A forward current pulse.

simulation results show that the small X will make the device punch through, and large leakage current. Secondly, in order to improve the device holding voltage, it is feasible to widen X distance appropriately. The mechanism is not only to increase the resistance along the discharge path, but also to reduce the current amplification factor β of the parasitic transistor PNP, and weaken the positive feedback of SCR. However, the N-well width X should not be too wide, because too wide X will make the SCR to hardly open.

4 TLP test verification

4.1 TLP test of HVDDSCR and HVDDSCR_FP+

The traditional symmetric HVDDSCR and the symmetric HVDDSCR_FP+ with floating P+ were fabricated and their performance were verified under 0.18μm process. The layout of each structure mentioned in this paper was drawn with finger length of 50μm and eight-finger pattern, Fig. 4 is the image of HVDDSCR_FP+ under metallographic microscope. The main application scenario of the 20V device is the vehicle network CAN bus, and the normal operating voltage of each port is ±12V. Thus, in the TLP test, the leakage current was measured at 13.2 V DC voltage (1.1 times the operating voltage).

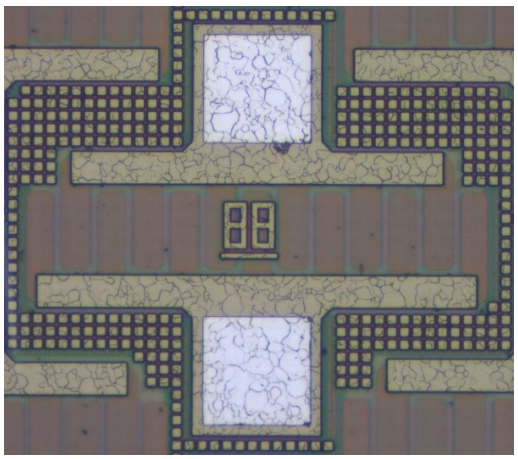


Fig.4 HVDDSCR FP+ eight-finger diagram.

TLP test is a method to measure the I-V characteristics of ESD protection devices under high current stress by using rectangular short pulses. It is also an important test method to evaluate the ESD protection technology of integrated circuits. Fig. 5 shows the TLP test results of HVDDSCR with Wb as K-1 μm and Wb as K+1 μm, and HVDDSCR_FP+ with Wb as K μm. The specific data are shown in Table 1. The diagram shows the structure of HVDDSCR. When Wb is K-1 μm, the forward and reverse holding voltages are 12.5V and 12.3V, the forward and reverse failure currents are 4.8A and 5.9A, and the forward and reverse leakage currents are about 20nA. When Wb is k+1 μm, the forward and reverse holding voltages of the device are 21.5V and 20.6V, and the forward and reverse failure currents are 35.3A and 33.6A respectively. Both the holding voltage and failure current of the device increase greatly, but the forward and reverse leakage currents are 53nA and 134nA. In the HVDDSCR_FP+, Wb is K μm, the forward and reverse holding voltage and failure current are higher than 22V and 35A, respectively, and the forward and reverse leakage currents are less than 20nA. Through comparison, it can be found that the performance of the device can be improved by widening Wb and inserting floating P+, but the method of inserting floating P+ can ensure that the holding voltage and failure current can be improved under the condition that the size of the device is basically unchanged.

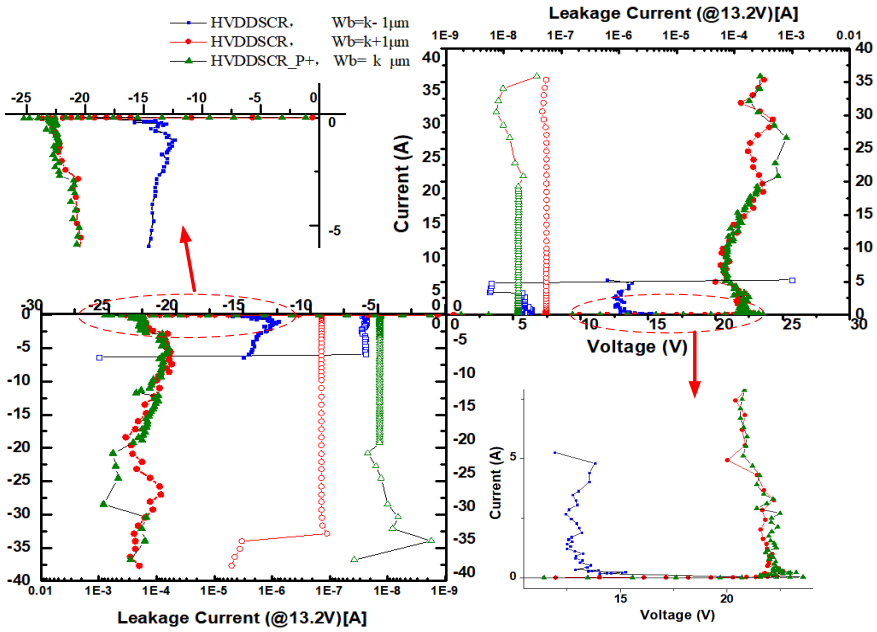


Fig.5 TLP test curves of traditional HVDDSCR with Wb=K-1 μm and Wb=K+1 μm and HVDDSCR_FP+ with X= k μm respectively.

Tab.1 TLP test data for HVDDSCR and HVDDSCR FP+

Device name		V_t (V)	V_h (V)	I_{t2} (A)	$I_{leakage}$(nA)
HVDDSCR Wb=k-1 μm	Forward	21.5	12.5	4.8	21.0
	Reverse	20.6	12.3	5.9	26.2
HVDDSCR Wb=k+1 μm	Forward	22.6	20	35.5	53.0
	Reverse	23.7	20.6	33.6	134.0
HVDDSCR_FP+ Wb=k μm	Forward	23.5	22.3	35.8	17.4
	Reverse	25.2	22.8	36.8	13.0

4.2 TLP test of N-well width X in HVDDSCR_FP+

The performance of HVDDSCR_FP+ device with three sizes of t μm, 2t μm and 4t μm was verified by tape-out. Fig. 6 shows the TLP test results of the three structures respectively, and the specific data are shown in Table 2. It can be seen from the diagram that when X is t μm, the forward and reverse holding voltage and failure current of the device reach 16V and 15A respectively. However, under the operating voltage of 13.2V, the leakage current is more than 1μA before the device is turned on, and the device cannot be used normally. When X is 2t μm, the device performance is great, the forward and reverse holding voltage and failure current of the device are increased to 22V and 35A, respectively, and the forward and reverse leakage currents are less than 20nA. When X is 4t μm, the failure current of the device is very low. The main reason is that the SCR is not open normally and this curve is not shown. The measured TLP data of the three structures also verified the correctness of the TCAD simulation results in Section 3.2.

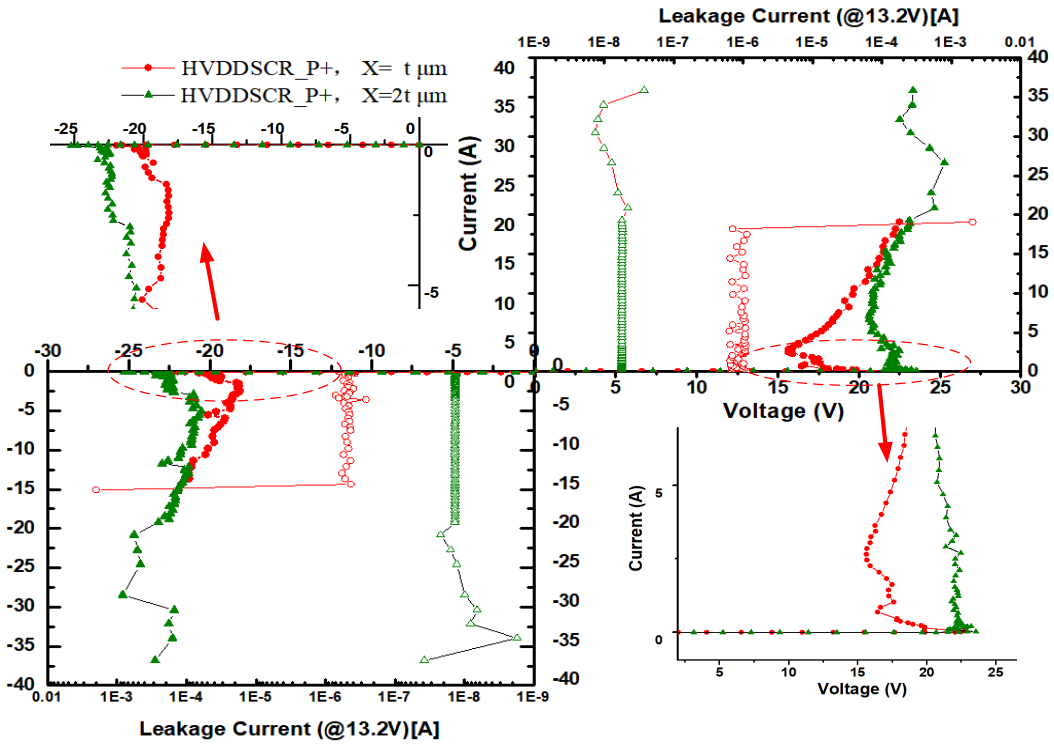


Fig.6 TLP test curves of HVDDSCR_FP+ structure with X = t μm and X= 2t μm.

Tab.2 TLP test data of HVDDSCR_FP+ structure with X = t μm and X= 2t μm.

Device name		V_t (V)	V_h (V)	I_{t2} (A)	$I_{leakage}$(nA)
HVDDSCR X=t μm	Forward	22.7	16.4	18.2	1030.0
	Reverse	21.9	18.1	15.0	1070.0
HVDDSCR_FP+ X=2t μm	Forward	23.5	22.3	35.8	17.4
	Reverse	25.2	22.8	36.8	13.0

5 conclusions

Under 0.18μm BCD process, theoretical analysis, TCAD simulation and tape-out verification show that the floating P+ can greatly improve the holding voltage and failure current of symmetric HVDDSCR devices. Secondly, the effect of N-well width X in symmetric HVDDSCR devices on device performance is discussed. The work in this paper has a certain guiding significance for the design of HVDDSCR electrostatic protection devices.

Acknowledgments

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