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# Low Power High Performance Current Mirror – A Review

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**Abstract.** In VLSI technology the circuit has small size. The efficient size gained due to decreasing chip design to nano-scale. But as chip size becomes very less the factor which adversely affects the design is maintaining constant current in CMOS integrated circuit. Current mirror replicates input current at the output. There is need to design current mirror circuit such that it works efficiently with low power requirement. In this work the survey of different CM circuits analysed and studies. Each CM has its advantages, limitations and research gap which is noted and applicable for further development.

**Keywords-** nano-scale, current mirror, VLSI, power dissipation, CMOS integrated circuit, amplifier, resistance, self-biased current mirror, MOS current mirror, cascode current mirror

## 1. Introduction

Current mirror is an electrical circuit. It is basically used to maintain constant current in the network. Recently the size of integrated circuits scaled down. Today the transistors size is available in nano-scale. As the transistors size is very less the channel length modulation effect arises [1,2,3]. Due to this effect the value of current does not maintain constant in the integrated circuit. To maintain constant value of current in the integrated circuit there is need to deploy current mirror in the circuit [4]. The basic current mirror circuit is as shown Fig 1.

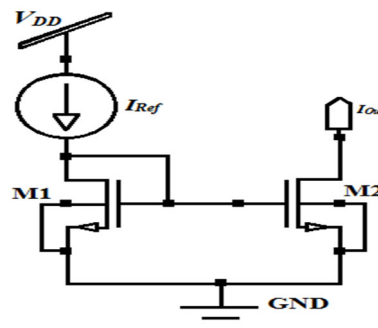


Fig. 1.1 Current Mirror

Above circuit is two transistor current mirror circuit. At input the  $V_{dd}$  supply is applied. As the voltage supply is provided the input current start to flow in the circuit this current is called as reference current. The drain and gate of the first transistor are directly connected to each other. This is diode



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connection formation ensures transistor in saturation and provides proper biasing. As the source terminals of both transistors connected to ground the gate source voltage of both transistors are same. The voltage drop across the terminal gate to source of transistor  $M_1$  is equal to the voltage drop across gate to source of transistor  $M_2$ . if both the transistors are identical the output current ( $I_{out}$ ) is equal to reference current ( $I_{Ref}$ ). Current mirror is a circuit that generates the replica of current flowing through an active device onto the other side, irrespective of loading [5]. It is extensively used for manufacturing operational transconductance amplifiers (OTA), comparators, analog to digital converters, digital to analog converters, amplifiers and filters [6]. In analog circuits operational transconductance amplifier (OTA) is important for low power amplification [7]. Drain current equation for MOSFET operating in saturation region:

$$I_D = \left(\frac{1}{2}\right) \mu_n C_{ox} (W/L) (V_{GS} - V_t)^2 \quad (1)$$

## 2. Different Current Mirrors

Recent different current mirror designs are available. But in this paper the current mirrors defined uses low power. The current mirrors are explained as bellow,

### 2.1. Low voltage low power body driven current mirror

With body driven current mirror the output impedance is increased [8]. By adding MOSFET  $M_5$  at the output side enhances output impedance and improves current transfer accuracy with  $g_m$  values.  $M_1$  to  $M_4$  are four transistor cascade current mirror [9]. The  $M_5$  accepts the signal from transistor  $M_4$  through amplifier stage which keeps transistor in saturation region. As the transistor set in saturation drain current maintains at constant level.

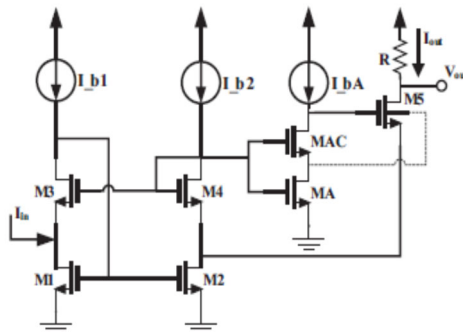


Fig. 2.1 Low Voltage Low Power body driven current mirror

Output impedance of this current mirror is increased by factor of

$$(r_{o2} \parallel r_{o2}) / (1 - g_{m2}g_{m1}R_2R_3 / (1 + g_{m1}R_3)) [g_{m5}r_{o5}(1 + g_{mA}R_{omA})] \quad (2)$$

From above output impedance is very high. Input impedance is equal to

$$R_{in} = g_{m1}g_{ds3}g_{ds1}(A+1) - g_{m1}g_{m3}^2 / g_{m1}g_{m3}^2g_{m5}(1+A) \quad (3)$$

$$R_{in} = 1 / \{ ((g_{m1} + g_{m3}g_{m1}/g_{m5}(1+A)) ((g_{m3}^2g_{m5}(1+A)) / (g_{m5}g_{ds1}g_{ds3}(1+A) - g_{m1}g_{m3}^2)) \} \quad (4)$$

From above equation input impedance is low. Accuracy of mirroring is

$$I_{out} = \lambda \cdot I_{in} \quad (5)$$

Where

$$\lambda = 1 / (1 + g_{ds1} / \{ (g_{m5} + g_{mb5})(g_{mA} R_{obA}) \}) \quad (6)$$

As the  $g_m$  of circuit increased to high value ideally the ratio  $g_{ds1} / ((g_{m5} + g_{mb5})(g_{mA} R_{obA}))$  reaches unity value. Hence accuracy is very high.

### 2.2. Quasi-floating gate current mirror

As we move towards low power application of MOS devices the problem of noise signals and variation of threshold voltage ( $V_T$ ) occurs. Consequently  $V_T$  limits low voltage operation for analog design [10]. The ultimate solution for this is the quasi floating gate MOSFET's in which threshold voltage can be lowered from its conventional value with reduction in capacitive trap voltage [11].

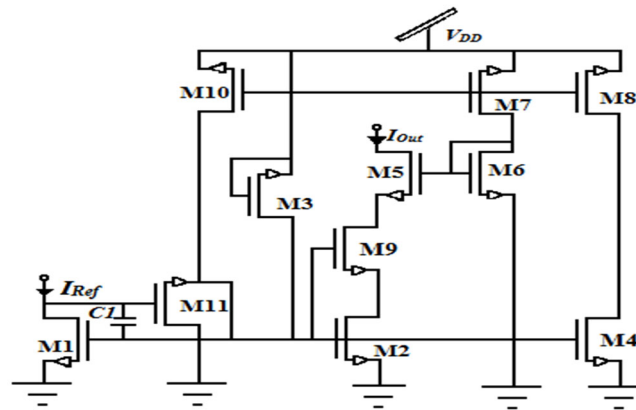


Fig. 2.2 Quasi-floating gate current mirror

In this current mirror  $M_{11}$  is used as level shifter which is biased by MOSFET  $M_{10}$ . MOSFET  $M_6$  and  $M_7$  are used for biasing output. The drain of  $M_5$  gives output value.  $M_2$  and  $M_9$  are in cascode structure to give very low current transfer error. The limitation of this current mirror is that it has more size.

### 2.3. Bulk driven self-biased cascode current mirror

In bulk driven technique threshold voltage is reduced without using extra circuitry.  $M_1$  and  $M_2$  are in saturation due to resistance  $R$ . At low supply voltage MOS works non-linear in which output values does not vary in proportion along with input values. It gives current mismatch.  $I_{offset}$  current is used to reduce mismatching of current. In this circuit effective is increased which allows larger bandwidth for operation [12, 13].

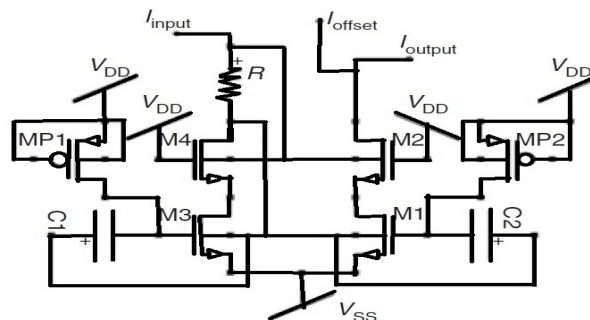


Fig. 2.3 Bulk driven self-biased cascode current mirror

The MOSFET  $M_1$  is quasi-floating form due to transistor  $MP_1$  and capacitor  $C_1$ . Similarly MOSFET  $M_3$  is quasi-floating form due to transistor  $MP_2$  and capacitor  $C_2$ . Transistor  $M_2$  and  $M_4$  are

configured as simple bulk-driven with their gates connected to positive supply. The output is obtained due to resistor R as it keeps M1 and M2 in saturation. The research gap is the complexity in the formation of capacitor and resistor within chip. The input and output resistance are calculated as

$$R_{in} = R + 1/(k g_{m3} g_{mb3}) \quad (7)$$

$$R_{out} = (g_{m1}^2 + g_{mb3}) r_{o1} q f g_{ro2} \quad (8)$$

The bandwidth of this current mirror is given as

$$\omega_o = \sqrt{((g_{m2}(k g_{m1} + g_{mb2})/C_{gs2}(C_{sb1} + C_{sb3})))} \quad (9)$$

#### 2.4. Dual current mirror

Level shifter is used to shift input low voltage signal to above threshold voltage signal. As for circuit low voltage is used power consumption of the circuit is very less. In this current mirror circuit consists of virtual current mirror (VCM) and Auxiliary current mirror (ACM) [14, 15].

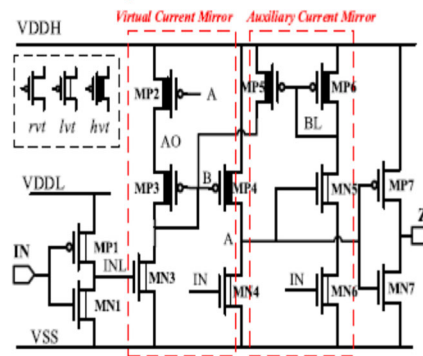


Fig. 2.4 Circuit diagram of dual current mirror

In low threshold (lvt) region VCM and ACM eliminates voltage drop to operate circuit correctly and robustly. In the high threshold (hvt) region VCM and ACM provides pull up to reduce leakage current [16]. This tells performance remain same with lvt and hvt hence by implementing lvt power consumption significantly reduced.

#### 2.5. Amplifier based low voltage current mirror

In this low voltage current mirror two voltage amplifiers are used to decrease supply voltage requirements [17, 18, 19]. Biasing amplifiers A<sub>1</sub> and A<sub>2</sub> keep M<sub>3</sub> and M<sub>4</sub> in ON condition during same time M<sub>1</sub> and M<sub>2</sub> in saturation region. Hence current mirroring occurs in the circuit with less modification. In this circuit as amplifier gain increases the input resistance is less and output resistance is high [20].

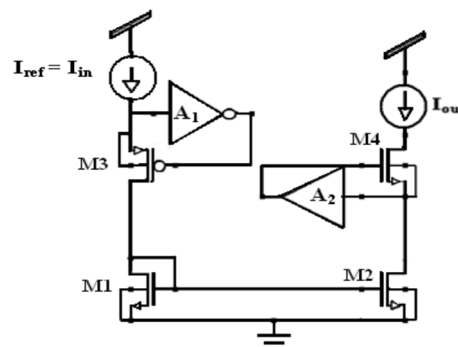


Fig. 2.5 Amplifier based low voltage current mirror

The input resistance is given as

$$R_{in} = r_{ds3}/(1 + g_{m3} r_{ds3} (A_1 + 1)) \quad (10)$$

The output resistance is given as

$$R_{out} = g_{m4} r_{ds2} r_{ds4} A_2 \quad (11)$$

### 2.6. Extremely low voltage & high compliance CM

The problem with CM is that the input/output voltage requirement for proper operation is considerably large. To minimize compliance voltage requirement an alternatively positive and negative circuits are inserted in the CM [21]. The low voltage high compliance current mirror is shown in fig 2.6.

This current mirror consists of transistors  $M_{C1}$  and  $M_{C2}$  which forms current compensated structure. The transistors  $M_1$ - $M_4$  used to provide positive feedback and the transistor  $M_2$ ,  $M_4$ - $M_5$  and amplifier '-A' used to provide negative feedback [22,23].

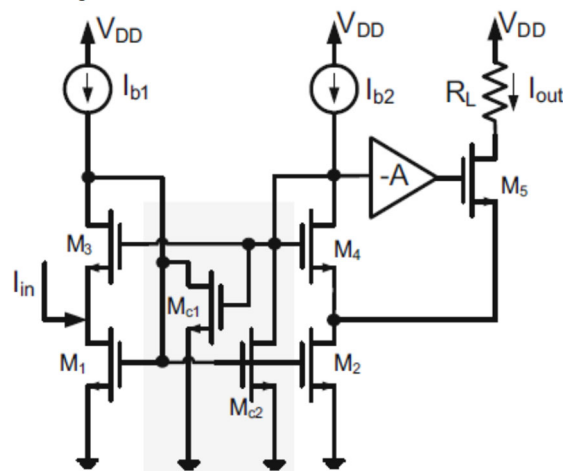


Fig. 2.6 Extremely low voltage high compliance current mirror

The positive feedback at low voltage plays an important role to improve the performance of current mirror with better stability. At large input voltage negative feedback stabilizes the output current with variations in output voltage. Hence the combined utilization of positive-negative feedback the current mirror circuit works at extremely low voltage with high performance.

### 3. Summarized Results

After the analysis of different current mirrors the parameters are summarized in to tabular form. This approach gives clear-cut variations due to different designs of current mirrors. The basic parameters considered for the comparison are input resistance, output resistance, input current, bandwidth of operation, power and technology used to scale the current mirror. The table.1 shows that current mirrors compared require low power for giving output.

Table 1. Summary of different parameters of different current mirrors

Reference	[9]	[10]	[12]	[14]	[17]	[22]
Input Resistance, $R_{in}$ (K $\Omega$ )	13000	240	675	-	0.18	0.01
Output Resistance, $R_{out}$ (K $\Omega$ )	39500	115	485	-	6.25	121300
Input Current, $I_{in}$ ( $\mu$ A)	15	447	500	8	-	320

Bandwidth (MHz)	216	655	2.5	1	98.50	211
Power	42.5 $\mu$ W	825 $\mu$ W	-	91pW	46 $\mu$ W	42.5 $\mu$ W
Supply Voltage (Volt)	1	$\pm 5$	-1	0.2-1.1	0.8	1
Number of Transistors used	7	11	10	13	10	10
Technology	0.18 $\mu$ m	0.13 $\mu$ m	0.18 $\mu$ m	40nm	90nm	180nm

#### 4. Conclusion and Future Work

From the study of various current mirrors and their summarised results it is seen that low voltage high compliance current mirror has highest output resistance and bandwidth. As this current mirror has highest output resistance it can drive large number of circuits easily. But the major drawback of body driven technique is that it has large input resistance which is inappropriate. This drawback has removed by low voltage high compliance current mirror. For considering operating frequency range Quasi-floating gate current mirror is appropriate as it works satisfactorily over high swing. Bulk driven self-biased cascade current mirror optimum solution for design. It has stable biasing which gives within range parameters of current mirror.

For power performance dual current consumes least power. It has smallest input current and voltage requirement but it uses more transistors so it is bulky. Low voltage improved performance current mirror is the best current mirror which requires low voltage and power. The voltage required to operate current mirror is 0.8 volt and power required is 46  $\mu$ W which is 6 times and 17 times less than quasi floating gate current mirror respectively. The scaling technology used is 90nm and transistors used are also less.

For future scope there is need to enhance parameters of low voltage improved performance current mirror. The output resistance and BW of the circuit must be increased by adding extra circuitry so that it becomes capable to drive large number of circuits with better performance. These current mirrors will be used to design the OTA for high frequency applications.

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