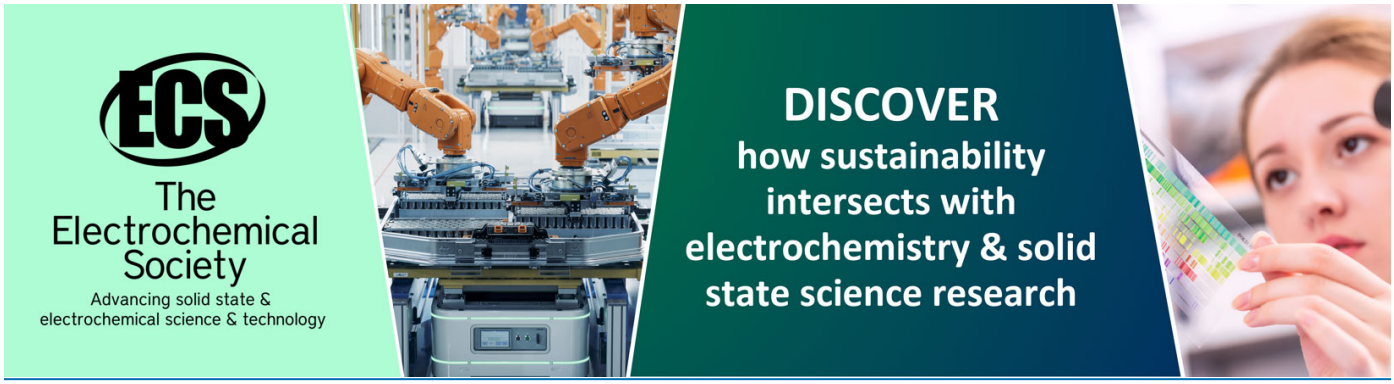
The Design and Simulation of Beidou Navigation Receiver LNA in B3 Frequency Band



The Design and Simulation of Beidou Navigation Receiver LNA in B3 Frequency Band

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Abstract. The Beidou satellite navigation receiver needs to receive Beidou signals efficiently in a complex environment, and the design of receiver front-end is the key link. According to the Beidou receiver front-end system indicators, such as noise figure, gain, etc., we propose a low-noise amplifier design scheme which is based on Infineon's broadband NPN RF bipolar transistor BFP740FED, and employ ADS to simulation and optimization tests. The results show that the low noise amplifier has a noise factor NF < 0.7dB, gain Gain > 35dB, gain flatness less than 0.5dB, input-output standing wave ratio less than 1.5 in the B3 band. This system has high noise performance of the amplifier, which can support the further development of Beidou navigation receiver application.

1. Introduction

Beidou positioning system is currently widely applied to ships, aircraft, mobile equipment, etc. [1-4]. The signal received by its wireless receiving system is often mixed with many noise signals [5]. To ensure an effective receiver main signal, it is important to design the front-end part of the RF receiving system. The low-noise amplifier is the key link of the front-end module [6], which can amplify and filter the received wireless signal into the signal required by the RF die. The overall noise performance of the RF receiving system is mainly affected by the sensitivity of the first-stage low-noise amplifier [7]. According to the Beidou satellite system index, we propse an LNA design scheme which is based on BFP740FESD. In addition, we employ ADS platform to simulation and optimization tests. The experimental results show that the system is suitable for Beidou B3 frequency band.

2. The design of low noise amplifier index

The third Generation Beidou satellite has opened and authorized service signals in the B3 frequency band. The Beidou B3I signal has a nominal carrier frequency of 1268.520MHz and a signal bandwidth of 20.46MHz. The minimum power level at which the B3I signal transmitted by the satellite reaches the output of the receiver antenna is -163dBW, and the designed LNA gain is greater than 30dB. We set the design index as follow:

Frequency range: 1.250 GHz ~ 1.286 GHz; Noise Figure: NF < 1.5 dB; In-band gain: G ≧ 30dB; In-band flatness ≦ ± 0.5dB; Input and output standing wave ratio < 1.5.

3. Design of low noise amplifier based on BFP740FESD

3.1. Bias circuit condition selection

Fig. 1 and Fig. 2 are the amplification die gain curve and noise curve, respectively, under the condition of bias voltage V_{CE} = 3V, bias current I_C = 25mA, operating frequency = 900MHz, NF_{min} = 0.55dB, the maximum gain is 26.5dB ; At 1.5GHz, NF_{min} = 0.55, the maximum gain reaches 24dB.

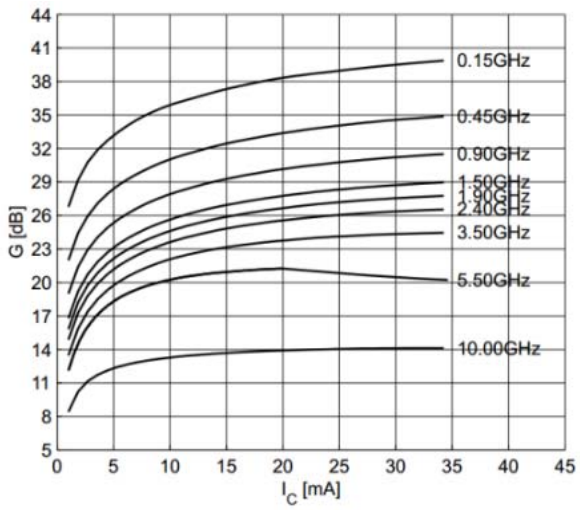

Figure 1. The relationship between Gain and I_C at different frequencies.

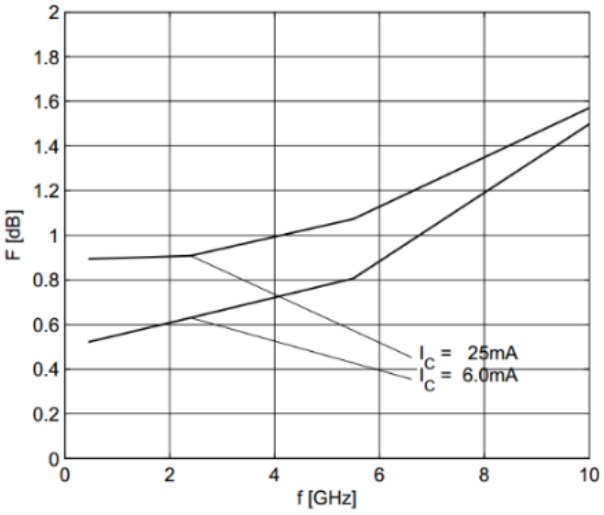

Figure 2. Frequency *f* and noise index.

The first step in the low-noise amplifier design is to design a bias circuit network. The layout bias circuit should fully consider some subsequent influencing factors such as noise and stability. To reduce the noise index, a reactive component should be added between the resistor bias circuit and the amplifier pins during design. It can maximize isolation such as power supply noise and thermal noise, etc., to improve transistor amplification performance and maintain the integrity of the main signal. The design should supply its bias voltage and bias current through the distribution of various reactances. Considering comprehensively, we set the bias voltage V_{CE} = 3.0V and I_C = 6mA. Finally, the BFP740FESD bias circuit is shown in Fig. 3.

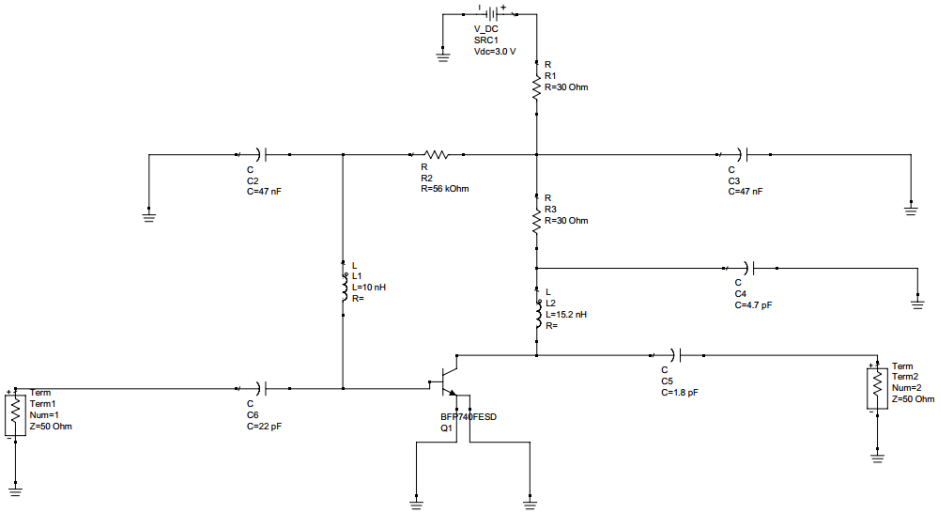

Figure 3. Bias circuit.

3.2. Stability analysis

Keeping the amplifier stable allows the low-noise amplifier to work properly. We employ the ADS2008 software to simulation and analyse the stability of the device BFP740FESD. It can be observed whether the amplifier circuit can maintain absolute stability in the frequency range of 1.250GHz-1.286GHz under normal bias conditions.

When the low-noise amplifier is not connected to the load, we set $K > 1$ and $|\Delta| < 1$ to maintain absolute stability of the bias circuit. When both conditions hold, $|\Delta|$ and K are expressed by the S parameter as follows:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{1}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{11}||S_{21}|} \tag{2}$$

In the later stage, the circuit can be adjusted according to the S parameter, so that the K value is greater than 1. Fig. 4 shows the results of preliminary bias circuit stability simulation.

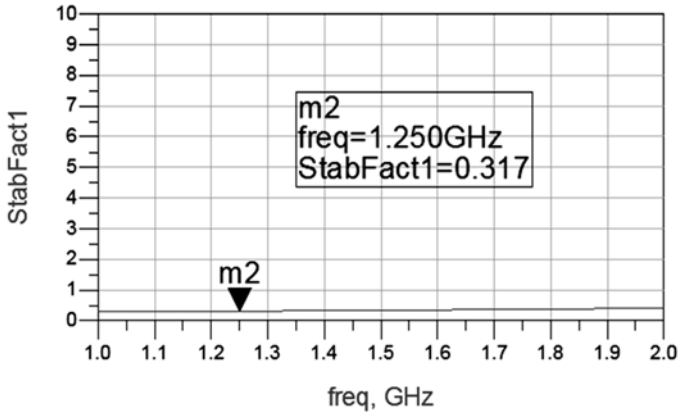

Figure 4. Stability index.

It can be seen from Fig. 4 that the amplifier stability coefficient $K < 1$ in the B3 band indicates that the circuit is in an unstable state. Therefore, on the one hand, the output port is connected in parallel with a resistor R to eliminate the negative resistance component and make it stable in design. On the other hand, the emitter pin of the BFP740FESD chip is connected to the small inductors L_1 and L_2 for negative feedback to improve the working stability. The results of stability improvement are shown in Fig. 5.

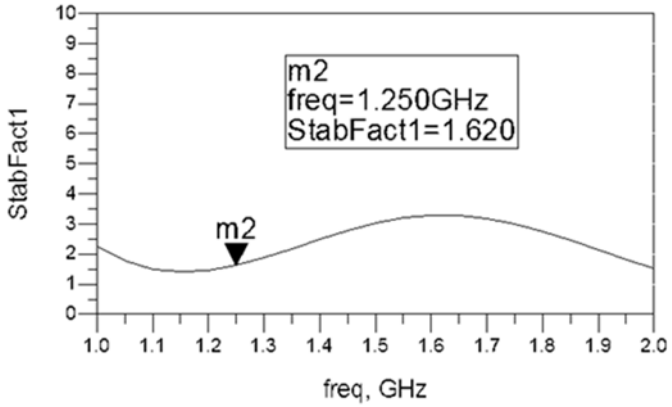

Figure 5. Stability coefficient after circuit improvement.

Comparing Fig. 4 and Fig. 5, the stability of the amplifier is significantly improved after adding negative feedback circuit and other measures. The subsequent circuit components *RLC* and microstrip line will be tuned and optimized in the simulation of the amplifier to maintain the noise index and gain based on the stability balance.

3.3. Noise analysis and matching circuit design

For low-noise amplifiers, it is unrealistic to achieve the minimum noise performance and the maximum gain at the same time. The increase of the gain will inevitably cause a relative increase in the noise index. The principle of large enough gain should be follow in test experiments. The circuit's initial noise figure circle and gain circle are shown in Fig. 6. Using the Smith chart matching tool in the ADS software to adjust the value of the capacitor inductance in the circuit, and finally match the noise figure circle center to the center. It indicates that the circuit has reached the best noise performance. Fig. 7 and Fig. 8 show the circle diagram and circuit after matching. *M4* is the input impedance at maximum gain; *m5* is the input impedance at minimum noise. The source impedance (50 ohms) of both ends of the first-stage amplifier is matched with the load impedance at the expense of a certain gain. The noise factor *NF* = 0.575dB and the gain *G* = 20.95dB.

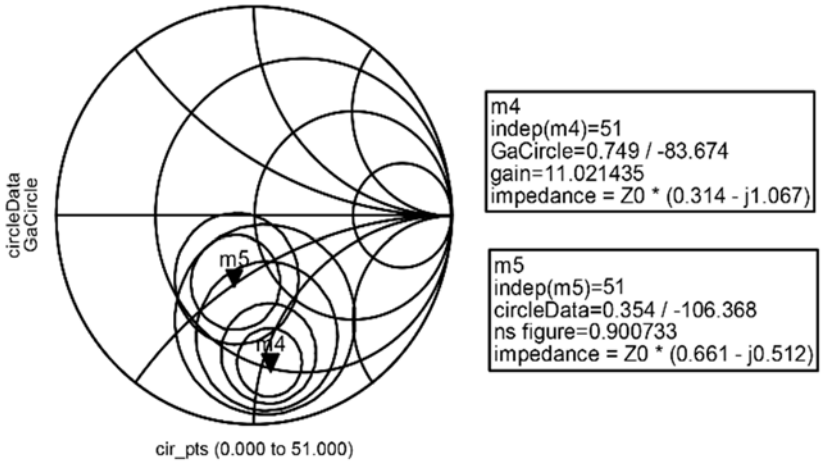

Figure 6. Noise index circle and gain circle.

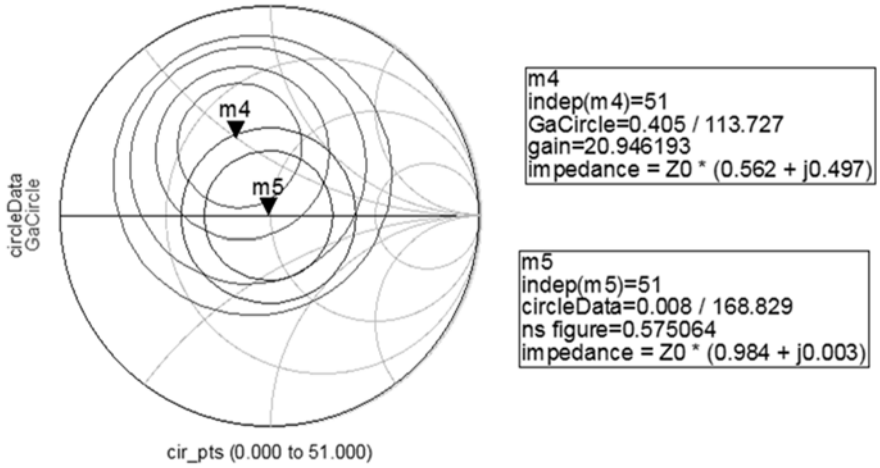

Figure 7. Best noise index matching circle.

To further balance the relationship between noise and gain for output matching, the input and output impedance matching of the BFP740FESD is shown in Fig. 8. The reactance components on the microstrip line analog circuit have a line width of W = 9.73mil. Fig. 9 shows a single-stage amplifier circuit. Adding a radio frequency choke circuit LC to the amplifier feed path, inductively isolating high-frequency signals, and bypassing capacitor filtering can suppress the influence of interference noise on the main signal.

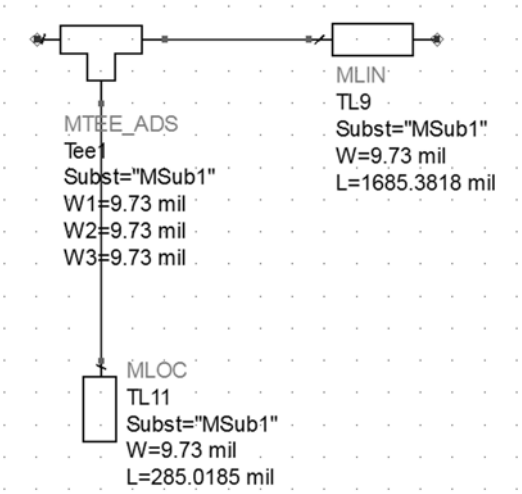

Figure 8. Best noise figure matching circuit.

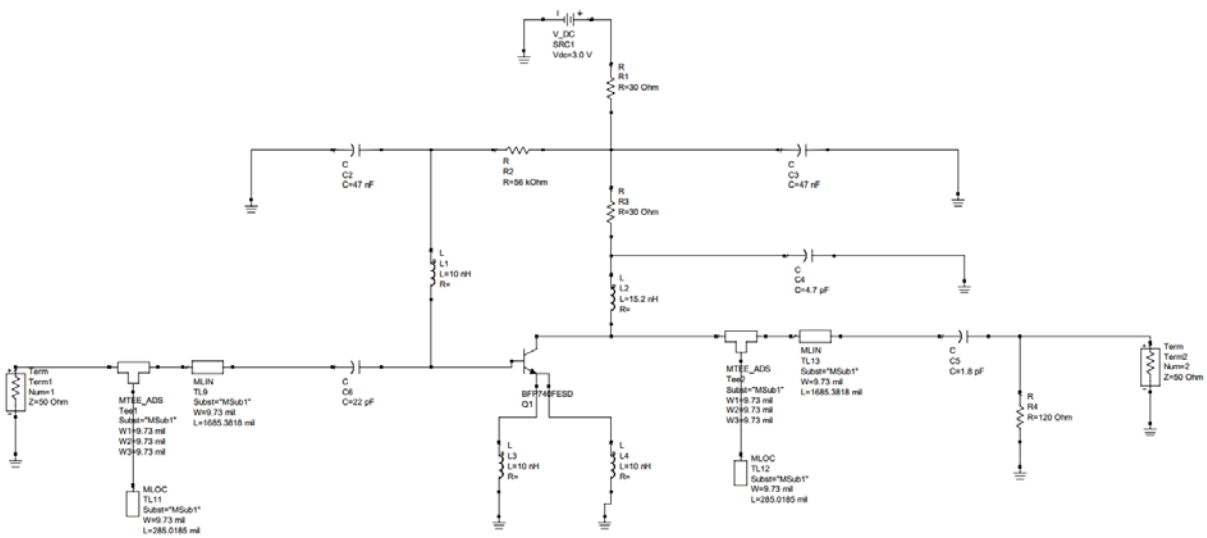

Figure 9. BFP740FESD single-stage amplifier circuit.

3.4. Two-stage amplifier design

The two-stage amplifier is based on conjugate matching, and the overall gain can reach more than 30dB. According to the principle of noise, the first stage noise of the amplifier has the largest impact on the overall noise performance of the system. Its circuit design mainly makes the noise factor as small as possible; the goal of the second stage is to increase the gain which is based on the output noise of the first stage. The design circuit is shown in Fig. 10. The connection between the two stages is a π-type matching design, which effectively isolates the return loss of the two stages to prevent it from weakening the system performance.

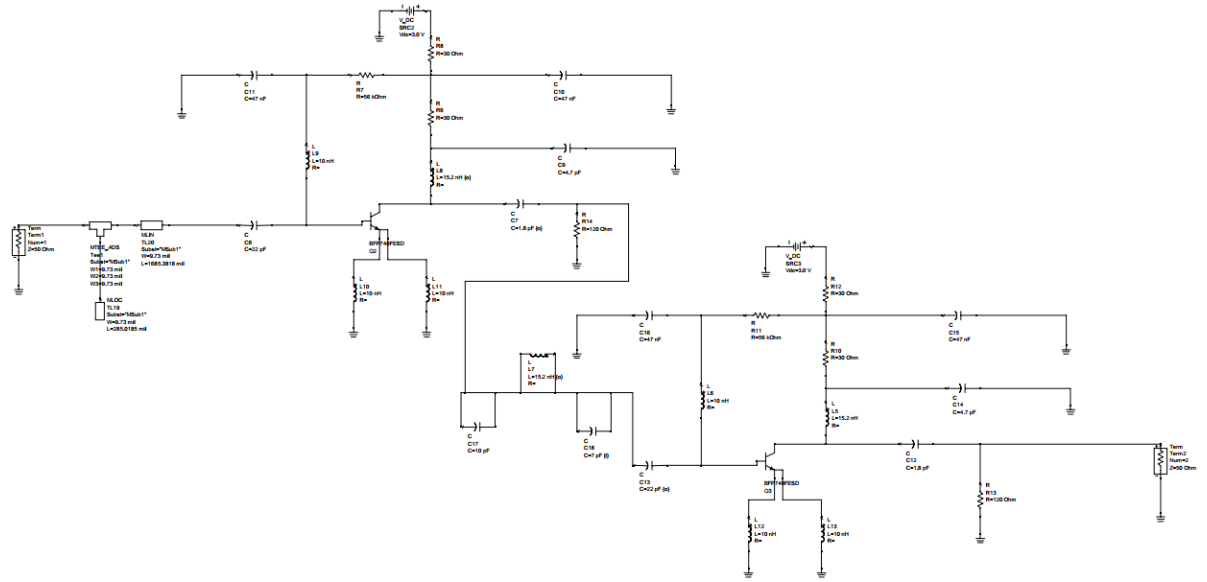

Figure 10. Two-stage amplifier circuit.

To filter out the noise interference caused by the power supply, two large capacitors which are 4.7nF and 47nF are designed in parallel at the power supply end. Due to their different self-resonant frequencies, they can effectively ground RF interference to ground. At the same time, the microstrip line matched between the stages is replaced with a parallel 7pF, 10pF capacitor and 15.2nH inductance to

obtain better gain flatness. High gain will affect the noise index and input standing wave ratio, so through the ADS tuning function, the size of the microstrip line on the matching circuit is adjusted to achieve a relatively ideal result for each index.

4. Simulation results and actual testing and analysis

4.1. Amplifier-S parameter simulation results

Fig. 11 shows the results of *S* parameter optimization, and Fig. 12 shows the results of noise figure and gain flatness. The simulation results show that at the center frequency of 1.25GHz, the noise figure *NF* = 0.574dB and the gain *S* = 40.904dB, which has reached the design requirements. The passband gain flatness is minus the value at m20 by the value of m19, the result is 0.426dB , *S* = 17.156dB, *S* = 10.307dB, input and output standing wave ratio < 1.5, designed to meet the requirements of the index, can be further applied to the subsequent development and application of Beidou navigation receiver.

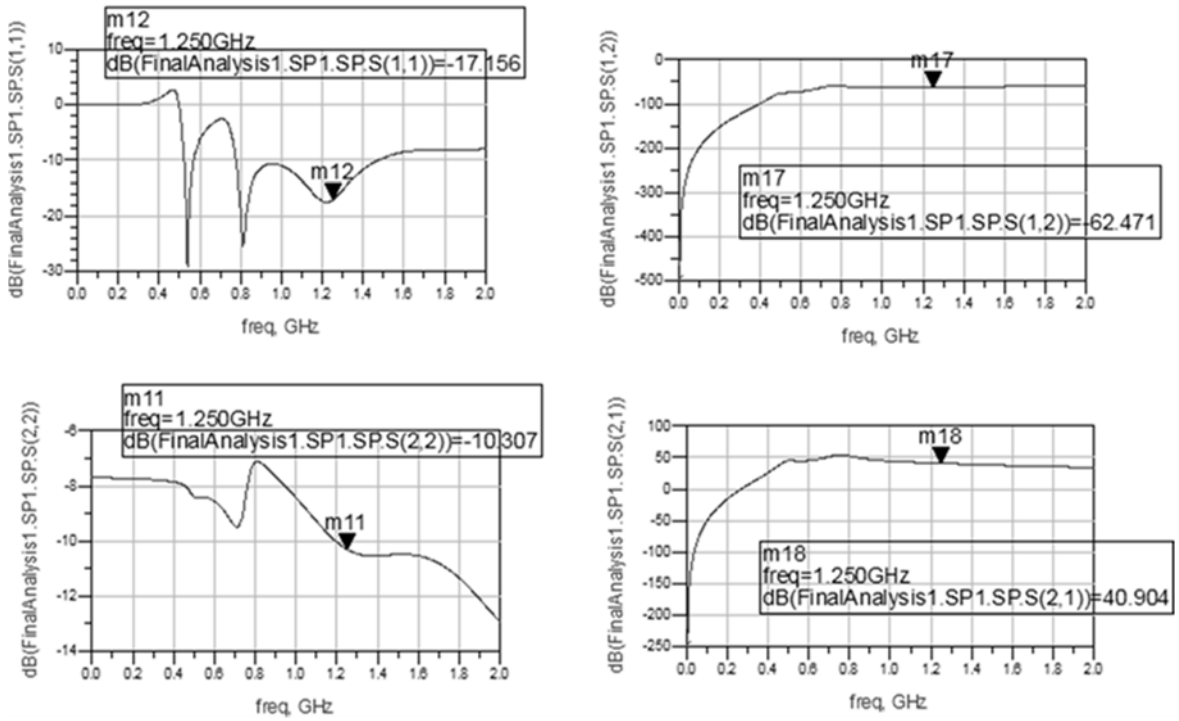

Figure 11. The results of *S* parameter optimization.

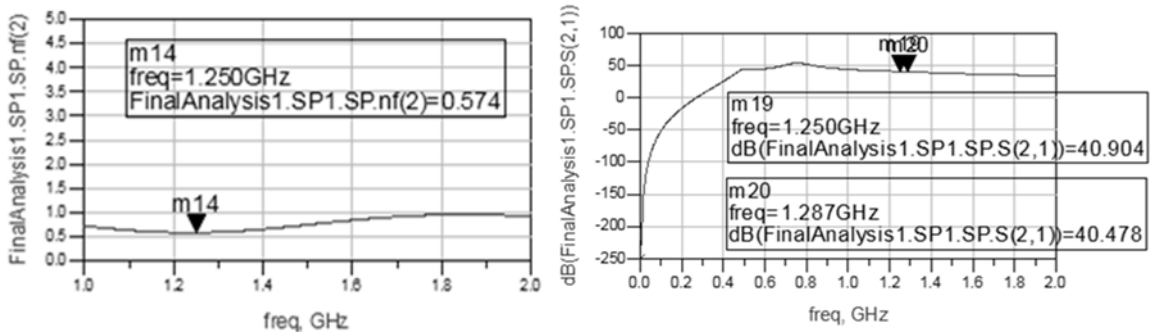

Figure 12. Noise index and gain flatness

5. Conclusion

To meet the requirements of the Beidou user receiver, this paper proposes a low-noise amplifier design based on the Infineon broadband NPNRF bipolar transistor BFP740FESD, and simulation and optimization tests were performed using classic ADS2008 software. According to the simulation data analysis, it shows that the transistor has good performance compared with the existing low-noise amplifier design solutions on the market. The performance of the low-noise and high-gain are improved, which provides the necessary conditions for the further development and application of the front end of the Beidou receiver.

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