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Submodelling method for modelling and simulation of high-density electronic assemblies

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Abstract. In order to enable the computation of fatigue life prediction of high-density electronic assemblies (solder joints > 4000), a modified submodelling approach was developed to integrate the detailed interconnections into equivalent layers with consistent mechanical parameters and thus reduce the complexity of modeling and simulation. The approach incorporates the uniform equivalent interconnect layers into the global model and simulate the general system response to thermo-mechanical loads. Displacements calculated from this first simulation are fed into a local model with more details of worst-case solder joints, in order to obtain local indicator of fatigue life. In this paper, referred to mechanical experimental methodology, a FEA process was used to extract the mechanical parameters of the equivalent layer. The validity of the modified submodelling approach was verified on fatigue life prediction of a high-density flip-chip package under thermal cycling.

1. Introduction

With the increasing of modern electronic devices integration and the number of internal transistors, the requirement of I/Os in an assembly also rapidly increasing. In order to increase I/O density, the type of external interconnection is being transformed from peripheral pins to area array (such as ball grid array, BGA), while the type of internal interconnection is being transformed from wire-bonding to flip-chip. This trend is expected to accelerate as the performance of electronic devices continues promoting.

High-density array packages typically manufacture submillimeter solder bump arrays on a die, which are mounted on a substrate or interposer as an intermediate layer, and then mounted to printed circuit board (PCB) through solder balls (2.5D/3D package could consist of more than one die or intermediate layer). Due to the difference between thermal expansion coefficients (CTEs) of the chip and substrate (or substrate and PCB), significant thermal stresses and strains are imposed on solder joints during thermal loading. Thus, the thermo-mechanical stress on solder joints leads to serious fatigue issue under assembly procedure or cyclic thermal loading of field use condition. In practical the thermal fatigue failure resistance of components is usually examined by means of thermal cycling (TC) and power cycling test.

In order to help the development of new packages or failure analysis of products failed in a qualification test, analytical models were developed by researchers to simulate the response of solder joints under cyclic thermal stress and predict fatigue life [1]. These models all include an indicator to characterize the extent of fatigue fracture and utilize finite element analysis (FEA) to calculate the indicator accumulated during thermal or power cycling with plastic or creep constitutive relations to describe the strain-stress curve of solder materials. Yet this method runs into efficiency and feasibility



issues, as the large number of interconnections require highly detailed modeling, despite their physical scale gap with the device and package. Besides, the highly non-linear inelastic deformation process is hardly accurately captured without adequately modeling the individual joints [2].

Different approaches have been developed to tackle these issues in the last few years, including the improvement of hardware performance and more efficient finite element methods. Through all these approaches, submodelling is the one of the most commonly used methods, and has been applied in thermal cycling fatigue life prediction of BGA components and flip-chip packages.

Generally speaking, submodelling is used in FEA to finely model tiny structures in a coarser, large model [2]. As such, the localized results of the coarse large model (called “global model”) provide boundary conditions of the finer tiny model (called “local model”) to run a second analysis on features that were ignored in the global model. In References [2, 3], the boundary displacement results from the global model of the whole package were loaded on the local model of the “critical” interconnection, mostly the solder joint at the corner or edges. However, once the total number of interconnections increases to thousands, it becomes difficult to properly mesh the global model because of the tradeoff between mesh quality—accuracy and quantity—computability, which could easily exceed one million even if the model is relatively coarse.

A modified submodelling approach is discussed in this paper, where uses an equivalent layer with uniform mechanical parameters for the interconnections. The material used in these layers of equivalent elements is an abstraction of the detailed interconnection region. The equivalent parameters are calculated through a simple finite element simulation, which makes the boundary conditions calculated from the global model more precise. The procedure of this approach is given below and the efficiency is confirmed by thermal cycling fatigue life prediction of a high-density flip-chip package.

2. Equivalent interconnect layers

In traditional submodelling approach [3], simplified configuration of interconnections and quite large element size are adopted to reduce the calculated amount. As the number of interconnections in high-density array packages continuously increasing, these methods become less effective while introducing more errors. In this case, researchers start to represent the actual interconnection area with an equivalent uniform material.

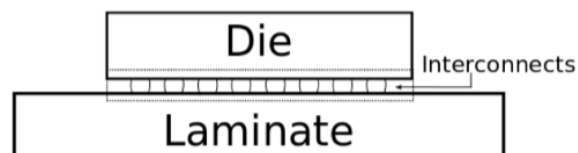


Figure 1. Abstracted zone of the global model.

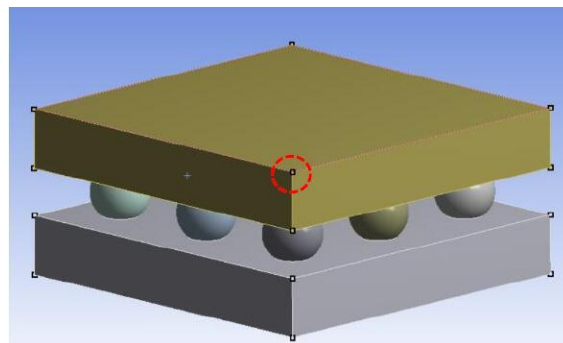


Figure 2. Simplified interconnection region model (quarter-symmetry model).

In Reference [2], the interconnections in the global model are represented via uniform equivalent layers, in a region shown as the dotted box on Figure 1. The elastic modulus and CTEs of equivalent interconnect layers' material are volume weighted averages of all the materials found in the

corresponding local models. A validation of the approach in Reference [2] was performed on a simplified interconnection region model with 6×6 joints array (Figure 2) by applying a thermal load on it. The interconnection area was equivalent to a homogeneous part using volume-weighted average method. And the simulated displacements of the same node at the upper corner of the chip (in the dotted circle) obtained with and without the volume-weighted average method are plotted in Figure 3.

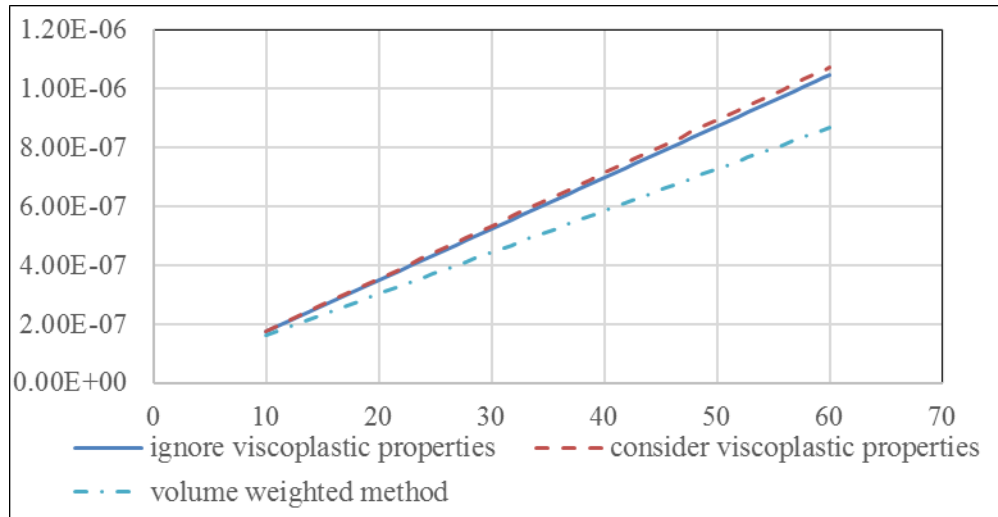


Figure 3. Total displacement of the node at up corner (red circle) calculated with and without volume-weighted equivalent layer (body temperature rises from -65°C to 150°C in 60 seconds).

The results plotted in Figure 3 show that there is a great difference on the slope between two curves calculated from original model and volume-weighted equivalent model. While the volume-weighted average method failed to precisely describe the equivalent mechanical properties of the interconnection region, it could be found that both the boundary displacements of the original and equivalent model approximate to straight-lines. Besides, whether the viscoplasticity of the solder joints is considered hardly impact the results of boundary displacement. Therefore, the methodology of equating the interconnection area to equivalent layers with uniform linear elastic material is feasible provided that the material parameters are appropriate.

3. Method for solving equivalent material parameters

3.1. FEA procedure for equivalent Young's modulus and Poisson's ratio

Young's modulus and Poisson's ratio are the two significant parameters of linear elastic materials. In this paper, a FEA methodology was proposed for calculating equivalent mechanical parameters for the equivalent layers, where finite element simulation was utilized to simulate the practical experiment in engineering application.

Table 1. Stepped tension loads applied on the upper boundary.

Time (s)	Tension (Pa)
0	0
1	1×10^5
3	2×10^5
5	3×10^5
7	4×10^5
9	5×10^5

In practice, the Young's modulus and Poisson's ratio of linear elastic materials can be obtained from static tensile tests, which can be implemented by finite element simulations. In this section, an

example of an interconnection region made up of 6×6 solder joints array and a fraction of the substrate (or PCB) and die (or substrate) is given (as Figure 2). In order to ensure the accuracy of the calculation, a series of stepped tension loads (listed in Table 1) are applied on the upper boundary of the model, while the bottom interface is fixed longitudinally.

The average longitudinal displacement of the upper boundary u_L is captured from the simulation. For the equivalent homogeneous material, the equivalent vertical strain ε_L is obtained by:

$$\varepsilon_L = \frac{u_L}{L} \quad (1)$$

where L is the total longitudinal length of the interconnection zone. The value of the equivalent stress σ is equal to the uniform tension T . According to linear elastic constitutive relation, the equivalent Young's modulus

$$E = \frac{\sigma_L}{\varepsilon_L} = \frac{T \cdot L}{u_L} \quad (2)$$

Similarly, the average transverse displacement of the right (asymmetric) boundary u_T is captured from the simulation. For the equivalent homogeneous material, the equivalent transverse strain ε_T is obtained by:

$$\varepsilon_T = \frac{u_T}{W} \quad (3)$$

where W is the total transverse width of the interconnection zone. According to linear elastic constitutive relation, the equivalent Poisson's ratio

$$\nu = \frac{\varepsilon_T}{\varepsilon_L} = \frac{u_T \cdot L}{u_L \cdot W} \quad (4)$$

In this approach, the least-square regression analysis is used to extract the equivalent Young's modulus and Poisson's ratio from a set of stress-strain and longitudinal-transverse strain data.

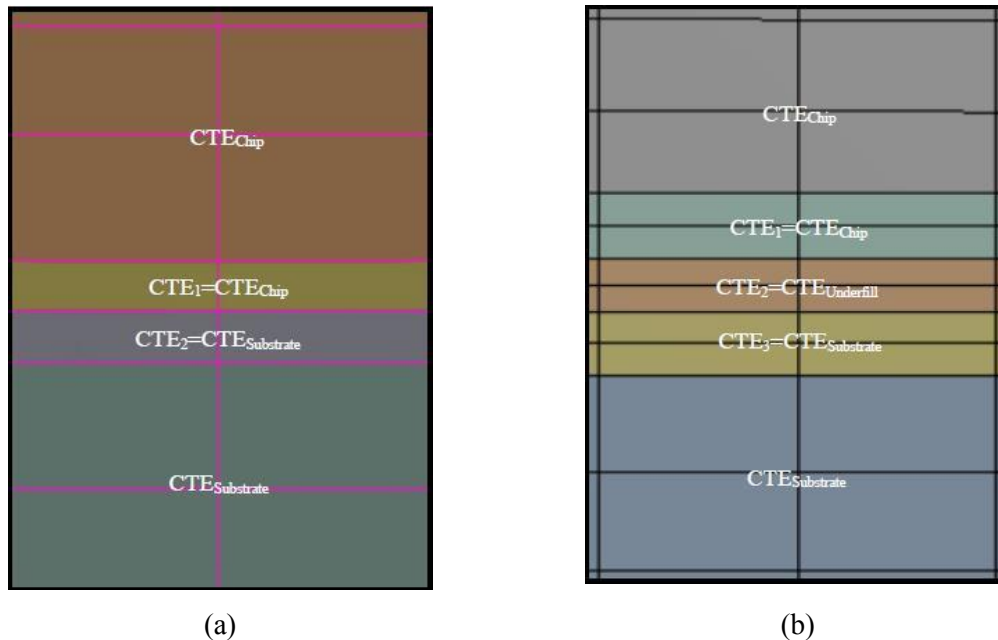


Figure 4. Cross-sections of the abstracted interconnection zone: (a) the assembly has no underfill; (b) underfilled.

3.2. CTE of the equivalent layers

The thermal expansion behavior of the interconnection zone is closer to that of the thermal bimetal or tri-metal model rather than a homogeneous material. Here, if there is no underfill, the equivalent layers

are split into two parts of the same thickness; otherwise the equivalent layers are split into three parts and the thickness of the middle part is the same as the underfill region. shown in Figure 4. A simplified processing is adopted to simulate real thermo-mechanical loading on the interfaces of the equivalent region, where the CTE of the part on chip side is consistent with the chip, while the CTE of the part on substrate side is consistent with the substrate material, and the CTE of the middle part, if any, is consistent with the underfill material. It is assumed that the error introduced by the simplification is acceptable.

4. Fatigue life prediction by modified submodelling approach

In order to use the method of the modified submodelling approach as a basis for thermal-mechanical fatigue life prediction of high-density array packages, its validity was verified by FEA of a high-density flip-chip package under TC condition. The predicted fatigue life of solder was evaluated through the simulation results of the local model. Then, the predicted life was compared with the experimental fatigue failure data by TC test.

4.1. High-density flip-chip model

The attributes of the test vehicle (shown in Figure 5) are given in Table 2 and the geometry of a bump is given in Figure 6. The flip-chip interconnect consists of 4320 solder bumps with a minimum pitch of 0.191mm and a maximum pitch of 0.339mm (Figure 7). 3D finite element model was constructed using the commercial software ANSYS Workbench to execute the package TC simulation and analysis. A quarter-symmetry model was used to increase the computational efficiency.

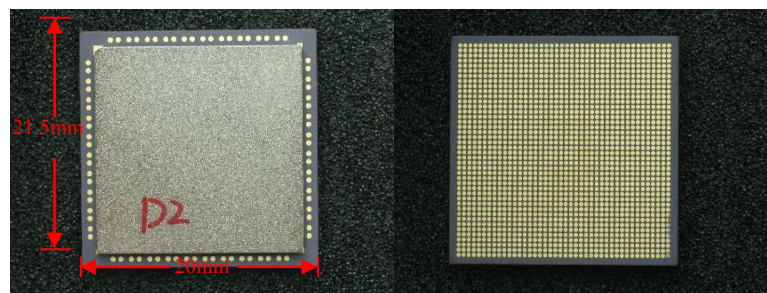


Figure 5. Schematic diagrams of test vehicle.

Table 2. Dimensions for modeling of flip-chip package.

Feature	Dimensions (mm)
Die	16 (L) $\times$ 13 (W) $\times$ 0.75 (T)
Ceramic substrate	21.5 (L) $\times$ 20 (W) $\times$ 2.4 (T)
Solder bump	0.06 (Top/bottom interface diameter), 0.11 (Middle diameter), 0.08 (T)

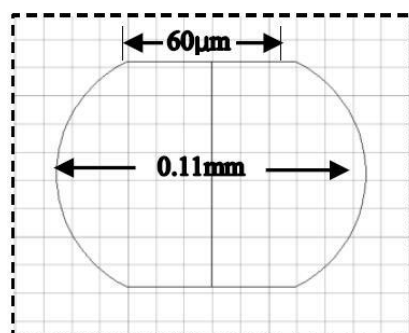


Figure 6. Bump dimensions.

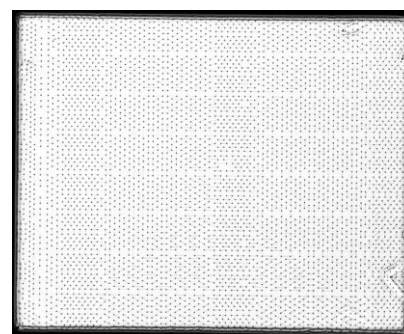


Figure 7. Flip-chip package interconnect layout.

In the modeling process, the heat sink was ignored to increase the computational efficiency. A rational assumption was made that the fatigue of solder bumps is dominated by global thermal mismatch between the chip and substrate [4]; so that the local CTE mismatch phenomenon was ignored and detailed features of pads and UBM materials were omitted in the modeling process. The material properties of the package are shown in Table 3.

The constituents of the substrate and Si die were considered as linear elastic materials. And the creep constitutive relation of 90Pb10Sn solder was modeled using Anand's model, the parameters of which were shown in Table 4. Moreover, the mechanical property variations of the underfill material at a temperature above T_g (88°C) was considered to increase the accuracy of life prediction.

Table 3. Material properties of package components.

Feature	Young's modulus (GPa)	Poisson's ratio	CTE ($10^{-6}/^{\circ}\text{C}$)
Si die	130	0.278	2.8
Substrate	241	0.25	7
Solder bump	19.03	0.35	28
Underfill	11.5	0.3	31
	0.25 (>88°C)		87 (>88°C)

Table 4. Anand's parameters for 90Pb10Sn.

Material parameter	90Pb10Sn
S_0 (MPa)	15.09
Q/R (K)	15583
A (s^{-1})	3.25×10^7
ξ	7
m	0.143
h_0 (MPa)	1787
$\hat{S}$ (MPa)	72.73
n	0.00438
a	3.73

The thermal cycle simulated was -65 to 150°C, with 1-minute ramps and 10-minute dwells. Two thermal cycles were performed in the simulation and the plastic work density increment during the last cycle was used as the fatigue damage indicator of solder bumps.

4.2. Submodelling process

Based on the modified submodelling approach, an interconnection zone in the global model was replaced by uniform equivalent layers. Here, the fraction thicknesses of the substrate and die in the abstracted zone are both 1 μm . In the modeling process, the real bump layout was replaced by a regular bump array with a pitch of 0.2mm to reduce the complexity of modelling. By this process, the uniform material parameters of the large-scale equivalent interconnect layer can be solved by a much smaller FE model with the same bump pitch instead of modelling all the interconnections (>1000). Nevertheless, it is not recommended to use a model containing only one bump to calculate the equivalent parameters, as the displacement distribution of the upper interface obtained by the tensor test simulation will be so dispersed that the average longitudinal displacement u_L is no longer valid to calculate the equivalent strain ε_L by Equation (1).

In this paper, the "equivalent parameters solution" FE model contained a 3×3 solder bump array, shown as Figure 2. The four interior faces were imposed symmetric constraints. The method described in Section 3.1 was used to obtain the equivalent material parameters of the abstracted interconnection zone with and without underfill, respectively. Equivalent Young's modulus and Poisson's ratios through the least square method are shown in Table 5.

Then, the equivalent interconnect layers in the global models with and without underfill were split into three and two parts, respectively. CTEs of the die, substrate and underfill were attributed to these parts according to the method described in Section 3.2 (Figure 4).

Table 5. Equivalent Young's modulus and Poisson's ratios.

	No underfill	Underfilled
Young's modulus (GPa)	7.12	45.4 8.26 (>88°C)
Poisson's ratio	0.012	0.137 0.059 (>88°C)

The finer local model (as shown in Figure 8) are located at the outer corner of the interconnection region in the global model. This model contains the bump at the outmost corner of the array where inelastic energy is higher in TC, as well as other three bumps next to it considered the potential local interaction between adjacent bumps.

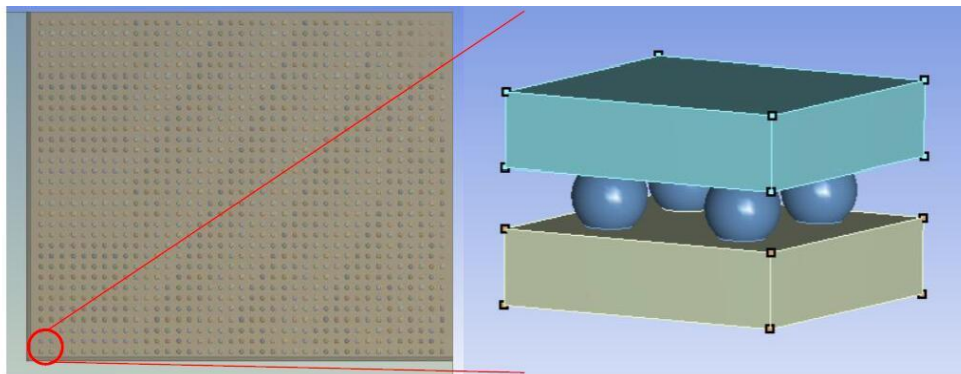


Figure 8. Schematic of the local model and its correlation of the global model.

4.3. Fatigue life prediction

In this paper, Darveaux's fatigue life prediction theory was adopted to predict the fatigue life based on the simulation [1, 3, 5]. Since the parameters given in [1] are for eutectic solder, characteristic life will be lower for the 90Pb10Sn solder being used here and solder will go through less temperature cycles.

Following the procedure to calculate fatigue life in Darveaux's theory, one needs to calculate the inelastic strain energy density (SED) per cycle first. In this case, the inelastic strain energy density could be expressed as the plastic work per unit volume in the ANSYS code. Note that Darveaux fatigue life prediction parameters given in [1] are for board level interconnections, a modification has been employed for smaller-size flip chip solder joints [6]. Based on Darveaux's theory, the inelastic SED increments per cycle were averaged over first two or three element layers next to the package interface. In modified Darveaux's model, the increment of average inelastic SED per cycle ΔW_{ave} is modified with the size factor multiplied as the following equation:

$$\Delta W_{ave} = \frac{\sum (\Delta W \cdot V)}{\sum V} \times \text{size factor} \quad (5)$$

Where the size factor is the ratio between the applied height of the solder bump and the height of the BGA used in the Darveaux's model. For the model in the present study, inelastic SED was averaged for the first two layers (7.5um thickness, shown in Figure 9) of the solder bump on the interface where the most SED concentration occurs [5].

Then, the number of cycles for crack initiation and crack growth rate are calculated using the Equations (6), (7):

$$N_0 = K_1 \Delta W_{ave}^{K_2} \quad (6)$$

$$\frac{da}{dN} = K_3 \Delta W_{ave}^{K_4} \quad (7)$$

Where N_0 is the number of cycles to crack initiation, and da/dN is the crack growth rate.

Then calculate the Characteristic life α_w , failure free life N_{ff} and the cycles to first failure N for a particular sample size based on the following equations:

$$\alpha_w = N_0 + \frac{a}{da/dN} \quad (8)$$

$$N_{ff} = \alpha_w / 2 \quad (9)$$

$$N = N_{ff} + (\alpha_w - N_{ff})(-\ln(1-F))^{1/\beta_w} \quad (10)$$

$$F = (1-0.3)/(S_s + 0.4) \quad (11)$$

Where a is the joint diameter at the interface, F is the cumulative distribution of failures for the 3P Weibull distribution, β_w is the shape parameter which indicates the amount of scatter in the data (was assumed to be 2.6), and S_s is the sample size.

Ki parameters from Darveaux's theory are given in Table 6 [1]. The simulation results show that the inelastic SED is the highest at the substrate interface when there's no underfill and at the die interface with underfill. A summary of the calculation results is given in Table 7, where the First Failure for the model with underfill was calculated for a sample size of 4.

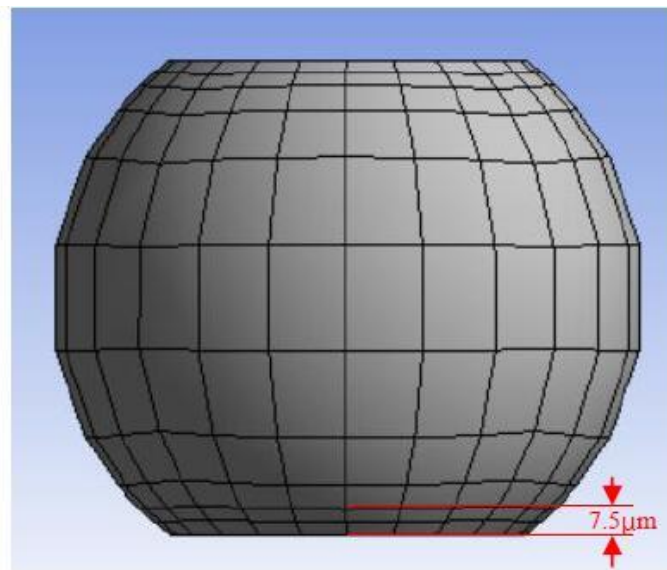


Figure 9. Model of solder bump: two layers near interface are 3.75um thick each.

Table 6. Darveaux's crack growth correlation constants.

K_1 (cycles/psi)	71000
K_2	-1.62
K_3 ($\times 10^{-7}$ in/cycle/psi)	2.76
K_4	1.05

Table 7. Fatigue life prediction summary.

	ΔW_{ave} (psi)	N_0 (cycles)	da/dN ($\times 10^{-7}$ in/cycle)	N_{ff} (cycles)	First Fail (cycles)	α_w (cycles)
No underfill	104.56	38	364.13	51	/	103
With underfill	19.168	594	61.323	489	522	979

4.4. Effect of multiple joints

The fatigue life calculated by Equations (8) - (11) are actually the life of the worst-case joints. In Reference [1], the effect of multiple joints is considered that all joints act in series and the failure of any one joint will cause failure of the component. In this paper, it is assumed that the fatigue life of the flip-chip package is controlled by the worst-case solder bumps at the corners. The fatigue life prediction results of the overall package α_p can be correlated to the fatigue life prediction results of the critical joint α_j by

$$\frac{\alpha_p}{\alpha_j} = \frac{1}{2} \left\{ 1 + \left[-\ln \left(1 - \left(\frac{0.7}{q + 0.4} \right) \right) \right]^{\frac{1}{\beta_w}} \right\} \quad (12)$$

Where q is the number of worst-case joints, typically 4.

5. Results and discussions

Five daisy-chain specimens were tested under experimental thermal cycling test, one of which has no underfill. The electrical conductivity of the specimens was tested every 100 cycles. According to the experimental results, the one without underfill failed within 100 cycles; through the underfilled samples, one failed between 300-400 cycles while all the others failed between 500-600 cycles.

Table 8. Package fatigue life prediction results.

	N_{ff} (cycles)	First Fail (cycles)	α_w (cycles)
No underfill	38	/	77
With underfill	367	392	734

The fatigue life prediction results of the overall package by Equation (12) are listed in Table 8. The predicted characteristic life is somehow higher than the practical fatigue life. Nevertheless, this deviation is acceptable, considering that local thermal mismatch was ignored in this simulation and the Darveaux's parameters used are for eutectic solders [3, 5]. Except for the characteristic life, it can also be seen that the failure free life and the number of first failure cycles are significant in predict the lower bound of the fatigue life distribution of a batch of components.

Another remarkable fact is that the overall simulation procedures were finished on 4 CPU cores in parallel (Intel i5-6700, 2.5GHz) and the computation time of the underfilled model (over 4000 interconnections) was only about 1hour 30mins, while it may take nearly a day using general submodelling method with the same hardware configuration, as the overall number of elements could be up to a million.

6. Conclusions

In this study, the authors investigated a modified submodelling approach and optimized the modeling method of the global model. In conclusion, the actual interconnection zone is equivalent to uniform interconnect layers and the equivalent mechanical parameters are obtained by tensile test simulation, which significantly reduce the complexity of modeling high-density array electronic package. The modified submodelling procedure was proved to significantly reduce the computation period without introducing excessive errors in the simulation process. Additional work is required on different assembly models to verify the stability of this approach on "relative" fatigue life prediction. Furthermore, the method of modeling the equivalent thermal mismatch behavior of the interconnection region and handling the irregular solder joint array still needs further research.

Acknowledgement

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