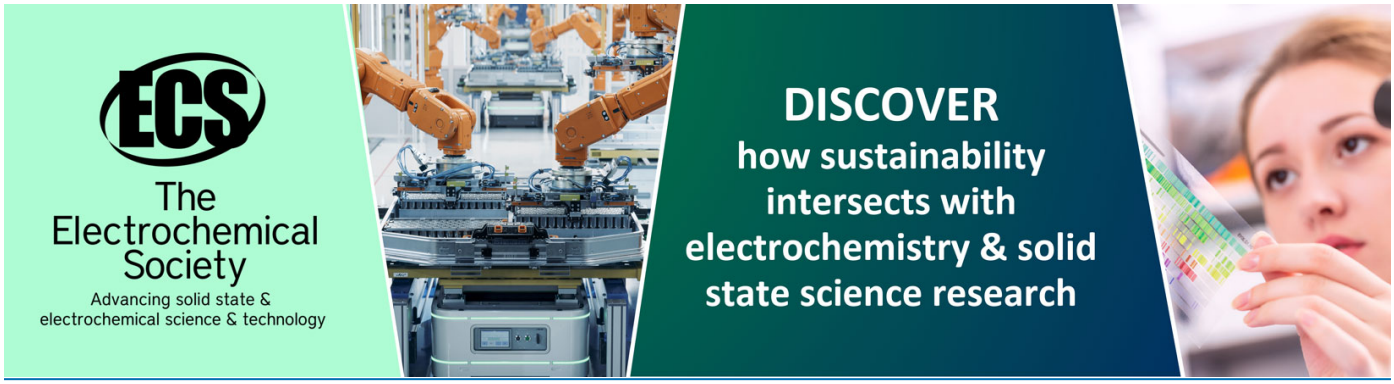
A Novel Sleep Scheduling Strategy on RISC-V Processor



A Novel Sleep Scheduling Strategy on RISC-V Processor

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Abstract. With the development of the Internet of Things, low-power technology has gradually become a primary factor in processor design. Processor sleeping mode is considered as an effective low-power technique. However, operation errors may occur if the long cycle instruction has not been completed during sleeping mode switch. To solve this problem, a novel sleep scheduling strategy based on RISC-V instruction set architecture is proposed. In this paper, the structure of RISC-V processor with task dispatching mechanism is described firstly. Then, WFI instruction and gating clock technology are adopted to realize the sleep scheduling strategy. Finally, hardware simulation is executed to demonstrate the feasibility of the novel sleep scheduling strategy.
Keywords. RISC-V; processor; task dispatching; sleep mode; clock gating,

1. Introduction

With the promotion of RISC-V instruction set architecture, RISC-V microprocessor has been widely used in a variety of application scenarios. Microprocessor is the core component of information collection and network communication in IoT (Internet of Things) [1]. As one of the core devices in the development of information society, the power of microprocessor is facing great challenges. With the improvement of manufacturing technology, processor performance has made a great progress. However, due to various reasons, the performance of single-core processors gradually slows down after about a decade of rapid growth. Meanwhile, power consumption becomes one of the main factors that influence and restrict the development of processors [2]. High power consumption can cause many problems: it usually brings high cost, affects the portability of the equipment and the reliability of the processor [3]. In order to extend the working life of processor, power consumption must be reduced as much as possible and sleep mode is considered as one of the most effective ways. However, sleep mode is hard to be switched directly while the processor is running, which may cause function errors due to incomplete instructions.

To solve the problems above, a novel sleep scheduling strategy based on RISC-V instruction set architecture is proposed in this paper. First of all, the sources of power dissipation and low power technology are discussed. Then it presents a two-stage pipeline RISC-V processor and the theory of the novel sleep scheduling mode strategy. The WFI (Wait for Interrupt) sleep instruction and clock gating are used to optimize the power while the task dispatching mechanism can ensure the processor

to run correctly. Finally, experiments are carried out to prove the feasibility of the novel sleep scheduling strategy.

2. Low Power Technology

The power dissipation in one circuit falls into two broad categories: dynamic power and static power [4]. Dynamic power is the power dissipation when the circuit is active and is mainly composed of two kinds of power: switching power and internal power. Static power is dissipated in several ways which mainly results from source-to-drain subthreshold leakage and current leaks between diffusion layers and substrate.

In synchronous circuit design, the circuit dissipates power as long as the clock is on. And much of the power is redundant. In many cases, clock gating technology provides a power-efficient implementation of register banks that are disabled during some clock cycles [5]. As long as a certain Verilog HDL (Hardware Description Language) coding style is followed, the EDA (Electronic Design Automation) tools can infer clock gating directly from the code style to reducing dynamic power [6]. RISC-V instruction set architecture provides a WFI instruction for sleep mode [7]. When the processor executes the WFI instruction, it will stop the current instruction flow and enter a sleep mode. Due to the existence of multi-cycle instructions, entering the sleep mode while the instructions are not completed should be prevented, or it may cause function errors. In this paper, it adopts the WFI instruction and clock gating to implement the novel sleep scheduling strategy. A task dispatching mechanism is designed to ensure that the current instruction run has been finished when the processor enter the sleep mode.

3. Theory of the Sleep Scheduling Strategy

The processor used in this paper is a two-stage pipeline processor, which bases on the RISC-V instruction set architecture as shown in figure 1. The first pipeline stage is IFU composed of fetch unit that can fetch instructions from the memory. The second pipeline stage is EXU composed of decode unit, task dispatch unit, arithmetic unit, sleep control unit, write-back unit and register files. Table 1 summarizes the functions of units.

The task dispatching mechanism is divided into task dispatching and task committing. As shown in figure 2, the task dispatch unit is composed of FIFO. It will dispatch a task when an instruction decode happens; it will commit a task when the result is written into the register files. After the task is committed, the task is considered as finished. Task clear signal will finally switch to 0 after all the tasks are completed.

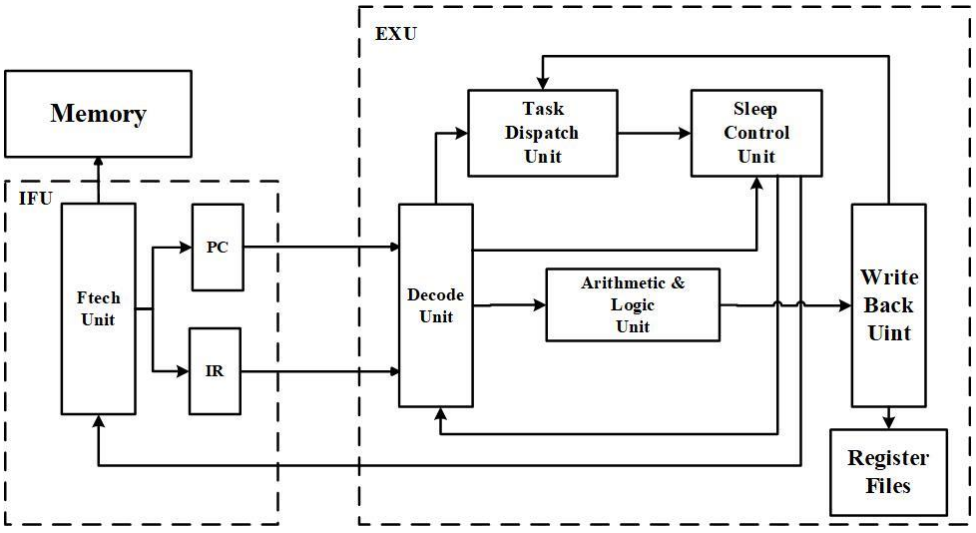

Figure 1. Processor architecture.

Table 1. Functions of units.

Name	Functions
Fetch Unit	Fetch instruction from the memory and send the instruction to the decode unit.
Decode Unit	Decode instruction and send the instruction information to the task dispatch unit and the arithmetic & logic unit.
Arithmetic & Logic Unit	Perform arithmetic operations and send the result to the write back unit.
Write Back Unit	Write the result back to the register files and send the information of result to the task dispatch unit.
Task Dispatch Unit	Dispatch and commit instruction tasks.
Sleep Control Unit	Receive the instruction information from decode unit and send sleep signal to fetch unit and decode unit.

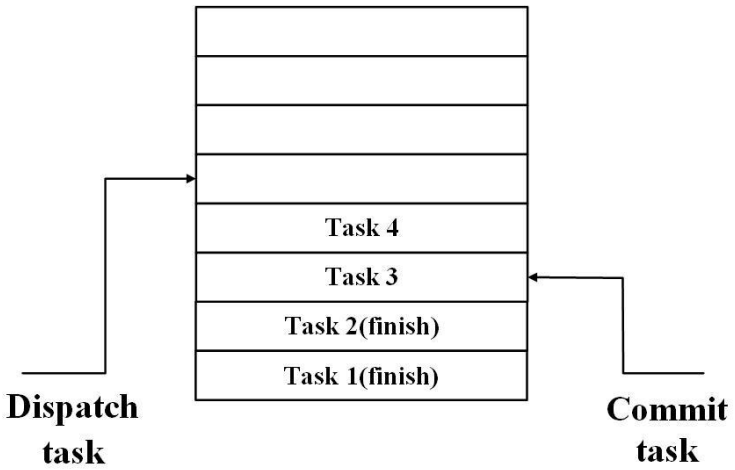

Figure 2. Task dispatching architecture.

The working mechanism of novel sleep scheduling strategy is implemented through the following steps, as shown in figure 3:

(1) After decoding a sleep instruction, a sleep command signal will be generated and sent to the sleep control unit by decode unit;

(2) Sleep control unit generates a sleep signal (0 signal) and transmits it to IFU and EXU respectively to control the clock signal of the two-stage pipeline;

(3) As clock of the fetch unit is gated with the sleep signal, when sleep signal is 0, the clock cannot enter the IFU and fetch unit will stop working;

(4) If the processor still has unfinished instructions, such as multi-cycle multiplication and division long instructions, the EXU will continue working.

(5) After all instructions are completed, a task clear signal (0 signal) will be sent by the task dispatch unit and go through OR gate with the sleep signal to generate a new signal. This signal will be 0 if the task clear signal is 0. In such a situation, the EXU will stop working because the clock cannot enter the EXU.

(6) Sleep control unit will receive the task clear signal then outputs a core sleep signal to indicate that the processor core has stopped working.

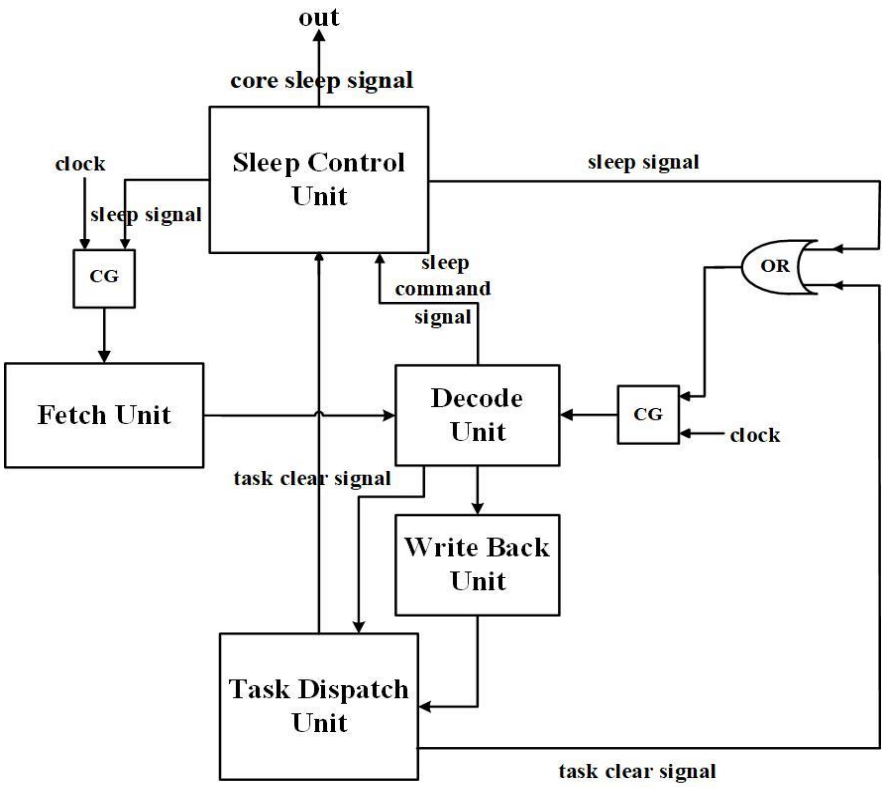

Figure 3. Novel sleep scheduling strategy mechanism.

4. Experiment

Figure 4 shows the full flow of the experiment. The riscv-gcc compiler translates assembly code of the instructions into binary and stores them in a separate file [8]. Then Tsetbench is coded to load this file and VCS+VERDI is applied for hardware simulation to analyze the waveform of the design. The detailed analysis of the waveform is as below:

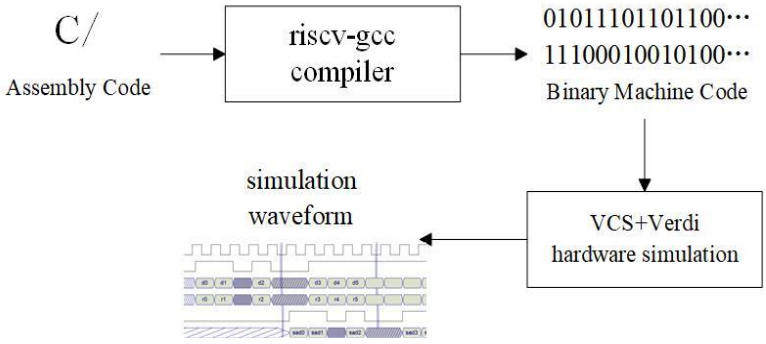

Figure 4. Experiment flow.

If the processor is not currently executing multi-cycle instructions, when the WFI instruction comes, the simulation waveform is shown in figure 5. The wfi_control signal (sleep signal) switches to 0 when sleep command signal comes and the task_done signal (task clear signal) is also 0 since no multi-cycle instruction is running. So, the gating enables signals ifu_clk_en and exu_clk_en will switch to 0, causing the clock signals clk_ifu and clk_exu to be 0. Finally, the core_wfi signal (core sleep signal) will switch to 1 which indicates that the core has entered sleep mode.

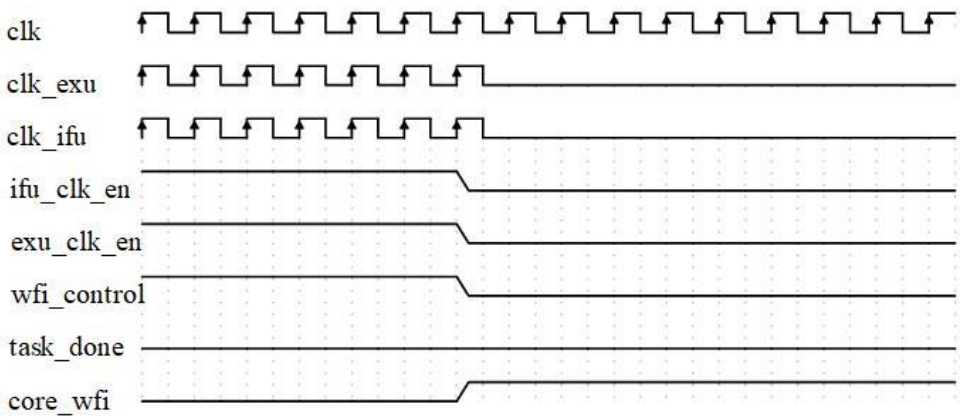

Figure 5. No Multi-cycle instruction simulation waveform.

If the processor is currently executing multi-cycle instructions, when the WFI instruction comes, the simulation waveform is shown in figure 6. The wfi_control (sleep signal) signal switches to 0 when sleep command signal comes but the task_done (task clear signal) signal is 1 since multi-cycle instruction is running. In order to prevent the processor issues caused by execution of multi-cycle instructions, only the gating enable signal ifu_clk_en switches to 0, causing the clock signal clk_ifu to be 0. After the multi-cycle instruction has been completed, the rask_done (task clear signal) signal will switch to 0. Then the signal exu_clk_en switches to 0, causing the clock signal clk_ifu to be 0. Finally, the core_wfi signal (core sleep signal) will switch to 1 which indicates that the core has entered sleep mode.

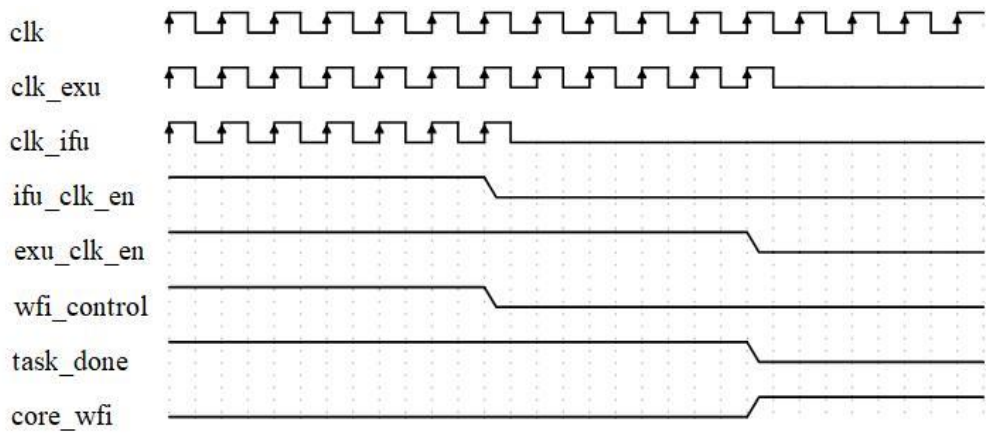

Figure 6. Multi-cycle instruction simulation waveform.

5. Conclusion

A novel sleep scheduling strategy based on RISC-V instruction set architecture is proposed in this paper. A two-stage pipeline RISC-V processor is presented and the theory of the strategy is introduced. The WFI sleep instruction and clock gating are used to optimize the power and the task dispatching mechanism is designed to ensure the operation correction of processor. Finally, the results of hardware simulation prove the feasibility of the novel sleep scheduling strategy.

References

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