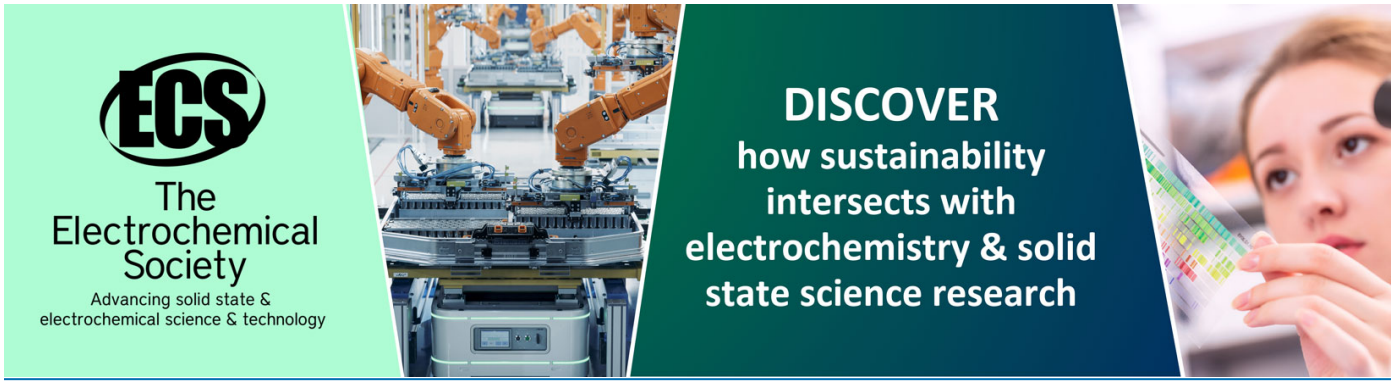
Precise clock synchronization for radio frequency positioning system based on White Rabbit PTP



Precise clock synchronization for radio frequency positioning system based on White Rabbit PTP

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Abstract. Use case of the White Rabbit Precision Time Protocol (PTP) sub-nanosecond clock synchronization system in complex with Time-to-Digital Converter (TDC) is examined for precise time of RF signal arrival capture. Implemented WR PTP core port on target hardware platform is explained. TDC placement method for Intel Quartus Prime tool is also shown.

1. Introduction

In this paper we examine use case of White Rabbit [1] network synchronization protocol for radio frequency positioning system. Our positioning system setup consists of some number of moving tags transmitting RF signal (whose coordinates are to be determined) and number of static anchors receiving RF signal (base stations). For calculation of tag location TDoA (Time Difference of Arrival) algorithm was employed. So, positioning error in this case highly depends on time of tag RF signal arrival capturing error, since frequency synthesizer devices are not perfect by their nature (because of PVT variations). Frequency drift of those is inevitable and such device on each anchor requires constant correction to be in phase with the others.

However, strict requirements for positioning accuracy and therefore for timestamping accuracy enforced us to use sub-nanosecond synchronization techniques, which were not possible to be implemented using traditional industrial standard methods (IEEE1588-2008 PTPv2) at the time development (started in 2018). Our choice was to use White Rabbit PTP protocol, actively developed in CERN, GSI and other institutions since 2009. In November 2019 IEEE 1588-2019 PTPv2.1 standard was approved, with High Accuracy Default Precision Time Protocol Profile, based on the White Rabbit PTP. Previous our approaches for solving precision positioning task can be found in [2].

For technical reasons target platform for development was selected different than platforms used in previous WR implementations and additional hardware was used to achieve sub-nanosecond timestamping accuracy in our positioning system. In this paper authors describe process and results of WR PTP IP core port onto Intel (formerly Altera) Cyclone 10 GX FPGA and creation of timestamping unit for RF synchronization signal.

2. White Rabbit PTP core port

In this section we explain the structure of WR PTP core and the modifications performed on this core in order to make it work on Cyclone 10 GX FPGA family.

So far, WR PTP core is available for various Xilinx FPGA's [3] with an exception of Intel's Arria V midrange FPGA family. For our application usage of Arria V FPGA's would be an overkill, so we decided to use a modern low-cost but still capable Cyclone 10 GX family as an RF positioning

hardware platform. Therefore, the next paragraphs describe WR PTP core port onto Cyclone 10 GX based hardware platform.

Main platform dependent parts of White Rabbit synchronization system to be ported are: transceiver PHY [9] and the set of 3 PLL's [8](System, DMTD, External reference)

Transceiver PHY should have deterministic latencies to be applicable in synchronous Ethernet application, such as White Rabbit PTP. In case of Arria V FPGA family Intel offers IP core with deterministic latencies, which could be easily configured and is the most convenient to be used. This core is a wrapper on actual PHY interface and PLL. However, such core is not available for the target platform, where bare transceiver PHY and FPLL were used.

To obtain deterministic latencies PHY should not use rate match FIFO and PCS FIFO should be in register mode, this way PCS latency is constant. RX word aligner state machine mode is set to "deterministic latency", so RX data won't be slipped after achieving sync.

PLL setup is standard and trivial and is omitted in the paper.

Low frequency output signal of Digital Dual Mixer Time Difference (DMTD) [4] phase detector was captured by SignalTap II logic analyzer, with properties similar to properties of signal from the other works.

External oscillator frequency correction circuitry was modified to exploit digitally controlled Si5340 clock synthesizers instead of DAC + VCXO combination.

Simplified structure of the developed synchronization system can be seen on figure 1.

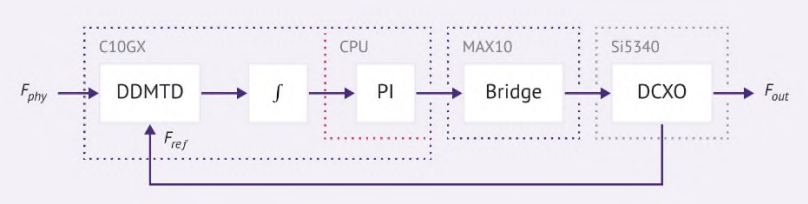

Figure 1. Simplified schematic of the modified WR clock correction circuitry.

3. Precise timestamp measurement of radio sync signal

In order to make sub-nanosecond timestamps of radio sync pulses TDC core with delay line was implemented [5,6]. Simplified delay line structure is shown on figure 2.

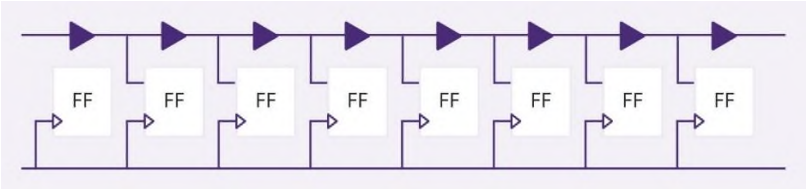

Figure 2. Delay line structure.

Intel Cyclone 10 GX fabric [8] consists of Logic Array Block (LAB) tiles, each LAB has 10 Adaptive Logic Module (ALM) blocks. ALM block consists of 2 LABCELL logic cells (with fast adders) and 4 flip-flops, 2 for each LABCELL. Fastest resource for delay line is fast adder carry chain. For example, Xilinx FPGA's have CARRY4 primitives [7] for easy carry chain exploitation, but Intel Cyclone 10 GX family has no such feature. Delay line is synthesized on LABCELL (cyclone10gx lcell comb from Intel cell library) primitives with constant inputs and the measured signal fed the carry chain. Adder output is captured by the flip-flop (cyclone10gx in cell library) on each cycle of the clock supplied by White Rabbit PTP core. Carry propagation direction through ALM is shown on figure 3.

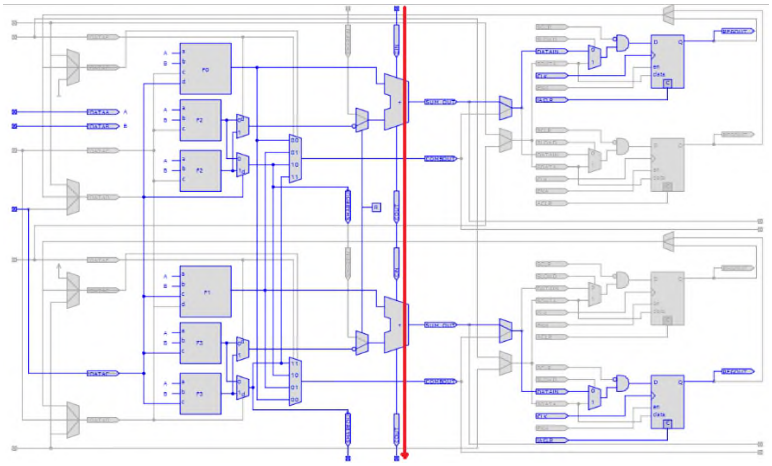

Figure 3. Cyclone 10 GX ALM structure view in Resource Property editor. Red arrow – direction of carry propagation through tile.

Each LCELL and flip-flop was placed manually by generated TCL script, which was included into Quartus settings file. This operation was performed to overcome spontaneous misplacement of flip-flops by Quartus Prime place&route flow [10], which can cause inconsistency in delays from signal source to flip-flops.

Example placement directive looks like following:

```
set_location_assignment LABCELL_X67_Y49_N6 -to
"dut|\\lcells:2:nextlcell:LCELL"
```

This way delay line is fitted by Quartus Prime tool strictly in place chosen by user, with no misplacements. Figure 4 shows the propagation path of the measured signal from signal multiplexer, through interconnect (diagonal arrow) and through carry chain (vertical line) to one of the capturing flip-flops.

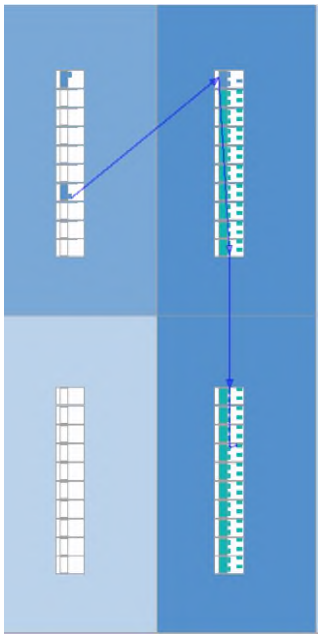

Figure 4. Delay line based on fast carry chain routed through FPGA fabric.

4. Conclusion

We implemented synchronization subsystem for radio frequency positioning system using White Rabbit PTP core for sub-nanosecond base station clock synchronization and TDC for precise tag signal timestamping. WR PTP core was ported to the target hardware platform – Cyclone 10 GX FPGA family. This way sub-nanosecond timestamp accuracy was achieved, required for precise time of arrival measurement. At this moment the developed synchronization subsystem is being integrated into the whole RF positioning project. The real synchronization and timestamping accuracy values are to be defined after completing the integration process but we expect to achieve accuracy not worse than 100ps according to the received synthesis and timing analysis results.

Acknowledgements

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