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# A two-step routing method with wire length budgeting for PTL routing of SFQ logic circuits

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Abstract. A PTL routing method for large-scale SFQ logic circuits is proposed. In this method, a routing problem is solved in two steps; global routing and detailed routing. In the global routing, a routing region is split into rectangular subregions and paths connecting them are obtained. Wire length budgeting is introduced into the global routing for allocating sufficient amount of routing resources to each net considering wire length matching in the detailed routing. In the detailed routing, exact wiring routes are determined based on a solution of the global routing and wire length matching is performed at each subregion. The global routing with wire length budgeting is formulated and an algorithm for it is proposed. In the proposed global routing algorithm, initial routes are searched at first using the rip-up and reroute technique, and then, routing resource distribution is calculated by constructing a flow-graph and solving a max-flow problem. If distribution of routing resources fails, global route extension is conducted to allocate additional routing resources to nets. The routing resource distribution and the global route extension are repeated until sufficient resources are allocated to all nets. As a design example, a 16 bit Sklansky adder was designed using the proposed method. Wire length matching in detailed routing was succeeded and the target frequency of 50 GHz was achieved.

#### 1. Introduction

Single-flux-quantum (SFQ) circuit technology is considered as a promising digital circuit technology that can follow conventional CMOS technology because of its high frequency operation up to tens of GHz with low power consumption [1]. SFQ circuits with tens of thousands of Josephson junctions (JJs) have become feasible due to the progress in the process technology [2]. Furthermore, passive transmission lines (PTLs) have been studied extensively for realizing high-speed interconnecting transmission lines with high wiring flexibility [3]-[5]. By using PTLs, it is possible to increase operating frequency and reduce circuit area. Under these circumstances, there is a growing demand on computer-aided design (CAD) tools for designing large-scale SFQ digital circuits.

In this paper, a PTL routing method for large-scale SFQ logic circuits is proposed. In this method, a routing problem is solved in two steps; global routing and detailed routing, and wire length budgeting is introduced to the global routing for allocating sufficient amount of routing resources to each net considering wire length matching. The global routing with wire length budgeting is formulated and an algorithm for it is proposed.

The computational complexity of a routing problem becomes high when a circuit size increases. To handle the complexity, global routing is performed at first to reduce the search

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space, then detailed routing is conducted. In global routing, a given routing region is split into coarse rectangular subregions and a grid graph is created from them. Then, a rough wiring route is obtained for each net by determining a path on the graph. In detailed routing, each net is then mapped to the PTL wiring tracks defined over the routing region and the layout of transmission lines are generated. Wire length matching of PTLs is also conducted in detailed routing by extending routes of nets at each routing subregion to add propagation delay. The quality of the obtained global routes affects the following detailed routing significantly and hence the quality of the final routing solution. Therefore, a global router should find a solution with high probability of routing completion called routability. Wire length matching is conducted by extending routes intensively in detailed routing, which consumes large amount of routing resources and decreases the routability. To obtain global routes with high routability considering wire length matching, wire length budgeting is introduced to global routing where the routes that sufficient routing resources can be allocated to each net without excessive use of resources are searched.

In the proposed global routing algorithm, initial routes are searched at first using the ripup and reroute technique. Then, routing resource distribution for each net is calculated by constructing a flow-graph and solving a max-flow problem. If distribution of routing resources is succeeded, then the algorithm ends. If not, the global routes are extended to allocate additional routing resources from other routing subregions. The routing resource distribution and extension of global routes are repeated until sufficient amount of resources are allocated to all nets.

This paper is organized as follows. A cell-based design of SFQ circuits and the issue about routing PTLs are explained in Section 2. Our proposed method is explained in Section 3 and a design example is shown in Section 4. A conclusion is given in Section 5.

# 2. Preliminaries

#### 2.1. Cell-based design

Cell-based design is adopted for designing SFQ digital circuits [6]. The design flow is shown in Fig. 1. The set of circuit elements such as logic gates are designed and defined as a cell library in advance. Then, a circuit layout is implemented by placing these cells and creating interconnections between them by using transmission lines.



Figure 1. Cell-based design flow of SFQ digital circuits.

# 2.2. SFQ logic gates

SFQ logic gates operate by pulse logic; the existence and the absence of a pulse in a clock period stands for logical value '1' and '0'. Each logic gate has clock input to execute its function and to output a pulse. To provide a clock pulse to all logic gates, a large clock network is needed.

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Each SFQ logic gate evaluates its input data and outputs the result at each clock cycle. Therefore, input data pulses must arrive at the gate before the beginning of the next clock cycle and every logic gate has setup/hold time constraints. In SFQ circuits, timing constraints must be met at all logic gates for correct operation.

# 2.3. Transmission lines

There are two kinds of transmission lines for connecting SFQ logic gates; Josephson transmission lines (JTLs) and PTLs.

JTLs include active JJs like other logic gates, and therefore, have greater delay and larger area than PTLs. A wiring segment of JTL is predefined in the cell library. A transmission line can be implemented by placing JTL cells in line.

PTLs, on the other hand, are simple metal lines. Pulses propagate on them at about one third of the speed of light in a vacuum without dissipation or dispersion [4]. However, an active driver cell and a receiver cell are needed at the start and the end point of a PTL. Furthermore, PTLs cannot branch and therefore active splitter cells are used for branching.

# 2.4. Wire length matching of PTLs

As mentioned in the previous subsection, JTLs and PTLs can be used as interconnections in an SFQ circuit layout. JTLs are active elements and the delay time varies depending on the bias current supplied to the internal JJs, while PTLs are passive elements and their timing variability is small. Therefore extension of PTLs is considered as a reasonable way to add signal propagation delay to match the delay caused by other PTLs, and in this case, wire length matching is performed.

PTL routing method with length matching has been studied in [8][9]. In these studies, channel routing problem is considered where cells are placed in row and PTLs are routed in the routing channel located between these placement rows. The width of each routing channel is minimized for designing compact layouts. In [8], simulated annealing is used to obtain a set of paths in a short time, while [9] considers the placement of SPLs to fully utilize routing resources. Extending routes of PTLs consumes large amount of routing resources and makes the routing completion difficult in detailed routing.

#### 2.5. Two-step routing

In designing layout of large-scale digital circuits, the computational complexity of the routing problems become high. To handle the complexity, the routing problem of a CMOS circuit is usually solved in two steps; global routing and detailed routing. In global routing, a given routing region is split into coarse-grain rectangular subregions and a path consists of a set of these subregions is obtained for each net to determine a coarse route. Then, in detailed routing, each net is mapped to the exact wiring tracks defined over the routing region based on the global routes. Global routing is effective to solve a routing problem with high computational complexity because it reduces a search space in detailed routing and also prohibit using expensive algorithm in detailed routing [10].

The solution of global routing affects significantly the following detailed routing. Therefore the global router has to obtain the routes with high probability of routing completion called routability. In general, the routability of a global routing solution is guaranteed by restricting each boundary between routing subregions to be utilized by sufficiently small number of nets compared to the number of wiring tracks running over the boundary.

# 3. Proposed routing method

#### 3.1. Overview

We propose a two step routing method of PTLs with wire length matching. In the proposed method, a global routing is conducted at first to obtain a coarse route for each net, then each net is mapped to the exact wiring tracks in detailed routing based on the obtained global routes.

Wire length matching is also conducted in detailed routing where routes of nets with small propagation delay are extended intensively at each routing subregion. To capture the amount of routing resources utilized for wire length matching and to guarantee the routability in global routing, wire length budgeting is introduced to global routing. Wire length budgeting is to allocate routing resources at each subregion on a global route to each net without excessive use of the given routing resources.

In the rest of this section, the global routing with wire length budgeting is formulated, and the algorithm for the global routing is proposed.

### 3.2. Problem formulation of the proposed global routing



Figure 2. (a)A given routing region with placed cells. (b)A grid graph for global routing.

In the global routing problem, a set of nets  $N = \{n_0, n_1, ..., n_k\}$  called netlist and placement of cells are given. Each net  $n_i \in N$  includes only two pins  $(p_{drv}^i, p_{rec}^i)$ . The position of each pin is determined by the placement.

A given routing region is partitioned into rectangular subregions as shown in Fig. 2(a) and a grid graph G(V, E) is generated. In this graph, each node  $v \in V$  represents a subregion and each edge  $e \in E$  represents a boundary between adjacent subregions. Typically the nodes are called *global cells* and the edges are called *global edges*. The generated grid graph is shown in Fig. 2(b). The global routing problem is to find a path on the generated grid graph for each net.

The wiring tracks of PTLs are running over the routing region horizontally or vertically, and a wiring capacity  $c_e$  is defined for each global edge e according to the available wiring tracks that e contains. A demand  $d_e$  on a global edge e is defined according to the number of nets utilizing the edge e, and the ratio of the demand to the capacity called routing congestion is defined as follows;

$$congestion_e = d_e/c_e \tag{1}$$

A solution of the global routing with large routing congestion makes the detailed routing hard and decrease the routability [11]. Therefore an overflow of a global edge e is defined to

be the difference between demand and capacity as follows and global routes for all nets without positive overflows are searched.

$$overflow_e = \begin{cases} d_e - c_e & (if \ d_e > c_e) \\ 0 & (otherwise) \end{cases}$$
(2)

In SFQ circuits, routes of PTLs are extended intensively in a global cell for wire length matching in detailed routing. To capture the routing resources utilized by the wire length matching, a demand  $d_v$  on a global cell v is defined as follows;

$$d_v = \sum_{n_i \in Net_v} l_v^i \tag{3}$$

where  $Nets_v$  is a set of nets whose routes run through the global cell v, and  $l_v^i$  is the wire length of net  $n_i$  utilized at v. A capacity  $c_v$  of a global cell v is defined to be the length of wiring tracks that v contains. A congestion congestion and an overflow overflow v for v is defined in the same way as global edge.

Wire length budgeting is to obtain  $l_v^i$  for each net  $n_i$  and global cell v without any positive overflow of global cells, and the proposed global routing is to obtain a path for each net with wire length budgeting.

3.3. Global routing algorithm 3.3.1. Overview



Figure 3. Flow of the proposed algorithm.

The flow of the proposed global routing algorithm is shown in Fig. 3. In the algorithm, a rip-up and reroute based route search is performed at first to obtain global routes without any positive overflow of global edges. Then wire length distribution is calculated and whether sufficient routing resources is allocated to each net considering wire length matching of PTLs is checked. If sufficient amount of routing resources are allocated to nets, then the algorithm ends. If there exists a net allocated with insufficient amount of them, the global route is extended to allocate routing resources of other global cells to the net and then return to the check phase. The details of each process are explained in the following subsections.

#### 3.3.2. Route searching phase

For each net  $n_i \in N$ , its global route on the grid graph G(V, E) is generated without any positive overflow of global edges in this phase.

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At first, an initial route is searched for each net using a maze routing algorithm [12] to find a shortest path on the grid graph. Then, a demand for each global edge is calculated and rip-up and reroute [14][15] is performed if positive overflow of edges exists. In the rip-up and reroute process, the routes of nets crossing overflowing edges are identified and the nets to be ripped up are chosen from them and new routes are searched. To remove the positive overflows, a higher edge cost is labeled to each global edge with higher congestion. Dijkstra's algorithm [13] is used for searching routes so that the utilization of the congested edges is avoided. This process is performed iteratively until all positive overflows are removed.

#### 3.3.3. Resource distribution phase



Figure 4. (a)Routed nets on a grid graph. (b)Constructed flow graph.

If global routes for all nets without any positive overflow of global edges are obtained, propagation delay of each net is calculated and additional wire length for the nets with small propagation delay is determined considering timing constraints at each logic gate. The exact propagation delay of a net cannot be calculated because the detailed route is not determined. Therefore, net delay is estimated using the global route and the position of each of the pins.

In the proposed global routing algorithm, a distribution of routing resources is calculated by creating a flow graph and solving the max-flow problem on the graph. The flow graph is constructed as follows.

- Generating a source node S and a sink node T.
- Generating a node  $v_{net}^i$  for each net  $n_i$ .
- Generating a node  $v_{gcell}^v$  for each global cell v.
- Generating a directed edge from S to  $v_{net}^{i}$  with the capacity of the additional wire length for each net  $n_i$ .
- Generating a directed edge from  $v_{net}{}^i$  to  $v_{gcell}{}^v$  if net  $n_i$  utilizes the global cell v.
- Generating a directed edge from each  $v_{gcell}^v$  to T with the capacity of the remaining routing resources of global cell v.

Fig. 4(b) shows the flow graph constructed based on the global routes shown in Fig. 4(a). By solving the max-flow problem on this flow graph, the routing resource distribution by which maximum amount of routing resources are allocated to nets can be obtained. If a flow of every edge from S to  $v_{net}^i$  reaches its capacity, then a distribution in which sufficient amount of routing resources are allocated to every net without any positive overflow of global cells is obtained.

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3.3.4. Global route extension



Figure 5. (a)A routed net and its flow graph. (b)Extended route and its flow graph.

When the wire length distribution fails, the global route extension is conducted to allocate additional routing resources to nets. A global route with insufficient amount of routing resources is shown in Fig. 5(a). The global route is extended by two global cells as shown in Fig. 5(b). When a route is extended, additional edges are added to the flow graph as shown in Fig. 5 and the max-flow will be increased.

# 4. Design example



Figure 6. The layout of 16 bit Sklansky adder.

We implemented the proposed algorithm as a CAD tool and designed a 16 bit Sklansky adder using the tool. In detailed routing, R-flip technique was used for extending routes for timing adjustment [16]. We used the cell library for the process technology of AIST Advanced Process 2 (ADP2) [7]. The cells are placed on a grid with the unit size of 30  $\mu$ m × 30  $\mu$ m and PTLs with the width of about 5  $\mu$ m are wired on two dedicated metal layers with via-holes. The circuit contains 1195 cells and 1814 connections, and the area is 36.8 mm<sup>2</sup>.

By constructing a grid graph for the global routing, there may be some connections whose pins are located in one global cell. These connections called local nets should be avoided because the proposed algorithm cannot extend their global routes in global route extension phase. Therefore, for wire length budgeting completion of the 16 bit adder, we set the length of each side of a global cell to 375 µm to restrict the number of local nets. After global routing, the maximum utilization of the routing resources of a global cell was 65 %, and the target frequency 50 GHz was achieved after detailed routing. The obtained layout of the circuit is shown in Fig. 6. A global route extended for additional routing resource allocation in the proposed method is also shown in Fig. 6.

#### 5. Conclusion

In this paper, a PTL routing method considering wire length matching for large-scale SFQ logic circuits is proposed. In this method, a PTL routing problem is solved in two steps; global and detailed routing. Wire length budgeting is introduced to the global routing for allocating sufficient amount of routing resources to each net considering wire length matching in the detailed routing. In the detailed routing, exact wiring routes are determined based on a solution of the global routing and wire length matching is performed at each routing subregion. A 16 bit Sklansky adder was designed using the proposed method, and the target frequency of 50 GHz was achieved by extending PTLs for timing adjustment.

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