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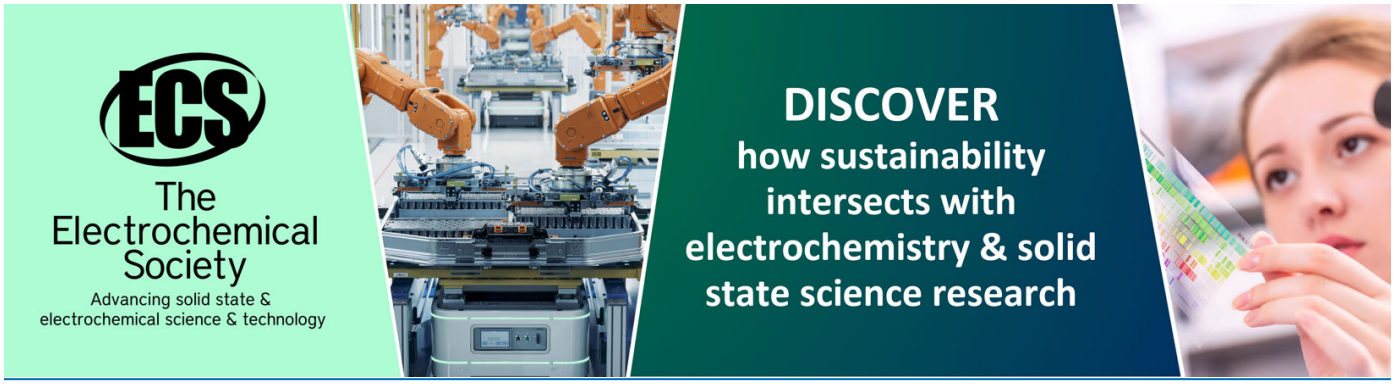

Methods for Increasing the Speed of the Analog Interfaces for Physical Quantity Sensors Based on Radiation-Hardened and Low-Temperature Technologies

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Abstract. The main circuitry methods for improving dynamic parameters in the large signal operation of the analog sensor interfaces (ASI) used in the instrumentation and automatic control systems are compared in the article. It is shown that the existing methods for increasing the slew rate (SR) of the ASI based on the operational amplifier (OA) are associated with the increase in the gain-crossover frequency of the OA due to the higher-frequency technologies (i.e., SiGe), or with the expansion of the range of active operation of the input subcircuit included before the integrating capacitor of the OA. A method for increasing the SR of the inverting ASI with an OA input stage of the dual-input class is proposed. The basis of the method lies in the introduction of two differentiating correction circuits (DCC) into the classical OA circuit, which in the large signal operation form additional overcharge currents of the integrating capacitance of the OA correction. In this case, the DCCs practically do not affect the low-signal amplitude-frequency characteristic of the OA. Such OAs have low current consumption in static mode and can be performed on the basis of standard processes, including radiation-hardened and low-temperature ones (CMOS, SOI, SOS, BiJFet, BJT, SiGe and others). The BJT OA computer simulation results show that the inverting ASI SR increases from 170 to 1800 V/μs. We consider the promising architectures of the high-speed OAs with the DCCs providing an increase in the SR in both inverting and non-inverting ASIs. The proposed ASI circuitry is designed to be used in automation devices and control systems, including nuclear and energy facilities.

1. Introduction

The CMOS ICs with a silicon-on-insulator (SOI) structure are promising electronic component base (ECB) for the harsh operating conditions of automatic control systems [1,2]. They have the increased radiation resistance in addition to a high degree of integration and low current consumption. The European Space Agency also recommends the SiGe process in SGB25RH [3,4] for space instrumentation.

Currently, low-temperature and radiation-hardened high-speed operational amplifiers (OA) [5,6] are top-requested for the tasks of analog-to-digital conversion (ADC) in demanding application devices. In this case, the dynamic parameters of the OA in the large-signal operation (the slew rate (*SR*) and the transient time t_{tr}) have a significant effect on the limiting characteristics of many computing and measuring systems [5-9].

The purpose of this article is to briefly analyze modern methods for increasing the ASI speed on the OA and to consider a new method (Patent RU 2676014) for reducing the transient time in the OA, which is based on the introduction of the nonlinear transient differentiating correction circuits (DCC) into the input stages of the OA operating only on a large signal and which have no significant effect on the low-signal gain-crossover frequency of the OA.

2. Modern methods for improving the speed of the OAs

The slew rate of the op-amp is proportional to the gain-crossover frequency of the OA f_1 and the clamping voltage of the transfer characteristic V_{lim} of the OA input stage, which provides a recharge of the integrating correction capacitance that forms the amplitude-frequency characteristics (AFCs) [10].

Currently, two basic architectures of the high-speed OAs – the voltage feedback (VF) [11,12] and current feedback (CF) circuits [11,13-15] are the most popular. Nonlinear correction circuits increasing the *SR* of the OA with the VF and having dead zones on the transfer characteristic [16,17] are quite often switched on only on a large signal, where a nonlinear mode of the main low-signal channel occurs, that is, they actually work as amplifiers with the CF. Therefore, there is a more general classification of the high-speed OAs [18] with various feedbacks, the names of which indicate:

- type of the feedback on the main channel of amplification on a small signal (VF or CF);
- type of feedback on a nonlinear parallel gain channel, which operates when a large signal overloads the main low-signal channel (VF or CF).

As a result, we can distinguish four architectures of high-speed OAs, within which the following feedbacks are possible:

a) potential-potential (P-P);
b) potential-current (PC);
c) current-potential (C-P);
d) current-current (CC).

The first word of the architecture name characterizes the type of the feedback on the small signal, and the second one – the type of the feedback on the large.

Nonlinear correction circuits and input differential stage (DS) circuits operating in class AB mode are the basis of many modern OAs, [19-21]. However, the *SR* limit values in the OAs with classical architecture are related to the static current consumption of the DS, as well as with the used element base, due to the so-called dynamic asymmetry [22,23] of the input DSs. For example, the high-speed CMOS OA is implemented in high-current mode of the input transistors, but the BJT OA *SR* almost doesn't depend on the static current of the input transistors [24,25]. This statement must be considered when designing the OAs of new generation.

3. Topology of the high-speed OAs with differentiating correction circuits in the inverting ASI

The OA is used in the inverting inclusion (figure 1) in many analog interfaces. This is one of the classic schemes of modern analog circuitry on the OAs [26], within which the simple methods can be applied for increasing the *SR*.

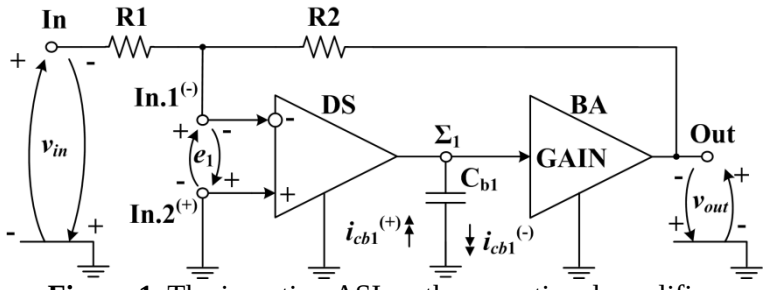


Figure 1. The inverting ASI on the operational amplifier.

The OA inputs do not operating with the common mode signal, which is a feature of the OA connection circuit of figure 1. This effect can be used to boost the processes of overcharging main integrating correction capacitance C_{b1} due to the special circuitry of the input stage of the OA (DS). This DS "senses" the numerical values of dynamic error e_1 and generates the corresponding control actions, namely the additional overcharge current of capacitor C_{b1}.

The functional scheme of the proposed OA (Patent RU 2676014) in figure 2 corresponding to the connection circuit of figure 1 contains differentiating correction circuits C_{b2} (C_{b3}), the introduction of which allows us to increase the *SR* and reduce t_{tr}.

The input voltage In.1$^{(-)}$ of the OA in figure 2 is $e_1^{(+)} \approx 0$ in steady state with a large loop gain for the connection circuit of figure 1. The value of $e_1^{(+)}$ can reach units of volts $e_1^{(+)} = V_{in}R_2/(R_1+R_2)$, and then it decreases almost to zero, during the front of the transient.

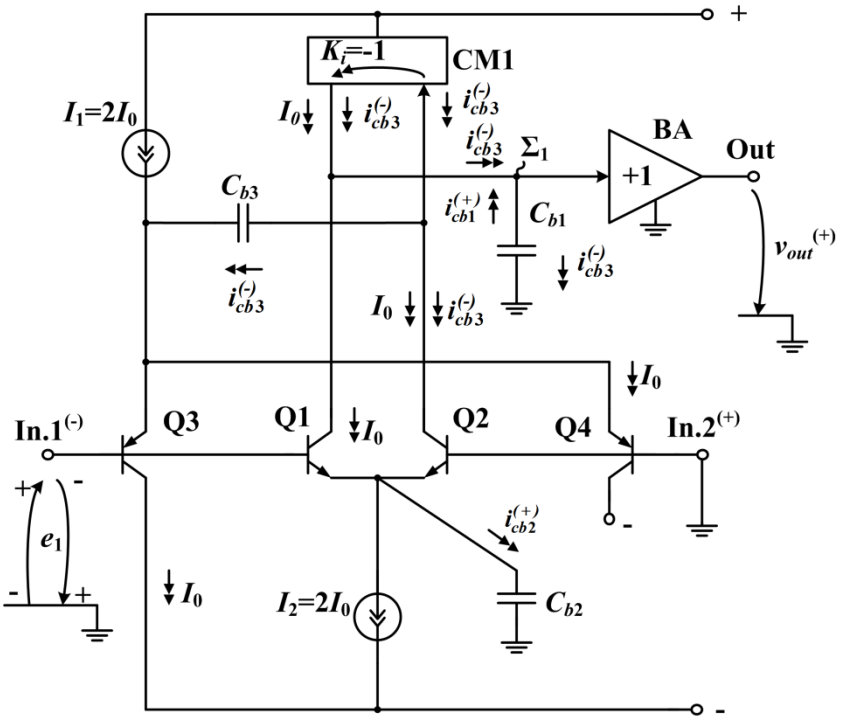


Figure 2. High-speed OA functional circuit for the ASI.

If a large pulse signal with amplitude V_{in} arrives to OA inverting input In.1$^{(-)}$ of figure 2 in the connection circuit of figure 1, this condition creates additional overcharge currents of correction capacitor C_{b1}, which are proportional to the derivative of dynamic error voltage e_1 :

$$i_{cb2}^{(+)} \approx K_i \cdot \left(de_1^{(+)}/dt\right) \cdot C_{b2} >> I_2 = 2I_0, \quad i_{cb3}^{(-)} \approx K_i \cdot \left(de_1^{(-)}/dt\right) \cdot C_{b3} >> I_2 = 2I_0 \tag{1}$$

where $K_i \approx 1$ is current transfer coefficient of current mirror CM1.

As a result, C_{b1} recharge rate increases substantially during the transient front, which leads to a significant increase in the *SR* in the large signal operation. This is due to the extremely small values of the time constants of capacitors C_{b3} and C_{b2}:

$$\tau_{cb3} \approx (r_{e3} + R_{i1})C_{b3} << C_{b1}R_i = \tau_1, \quad \tau_{cb2} \approx r_{e1} \cdot C_{b2} << C_{b1}R_i = \tau_1, \tag{2}$$

where R_{i1} is input impedance of current mirror CM1; r_{e1}, r_{e3} is differential resistances of emitter junctions of transistors Q1 and Q3; R_i is equivalent resistance in high impedance Σ_1, τ_1 is time constant of correction capacitor C_{b1}, which determines the gain-crossover frequency of the OA.

Taking into account that the Laplace representation of the corresponding voltages and currents of the circuit elements (figure 1 and figure 2) are connected by the equations

$$E_1^{(+)}(p) = \left(V_{in}^{(+)}(p)\right) / \left(1 + N_R\right) - \left(V_{out}(p) / \left(1 + N_R^{-1}\right)\right), \tag{3}$$

$$I_{cb2}(p) \approx E_1^{(+)}(p) \cdot pC_{b2}, \tag{4}$$

$$V_{out}(p) \approx I_{cb2}(p) / pC_{b1} = E_1^{(+)}(p) N_c, \tag{5}$$

it can be shown that under conditions (2) at $N_R = N_R^{-1} = 1$ and unity gain $\left(GAIN \approx 1\right)$ the output voltage of the OA is

$$V_{out}(p) \approx \left(N_c / 2 + N_c\right) \cdot V_{in}^{(+)}(p), \tag{6}$$

where in equations (3)-(6) $N_R = R_2 / \left(R_2 + R_1\right)$, $N_c = C_{b2} / C_{b1}$.

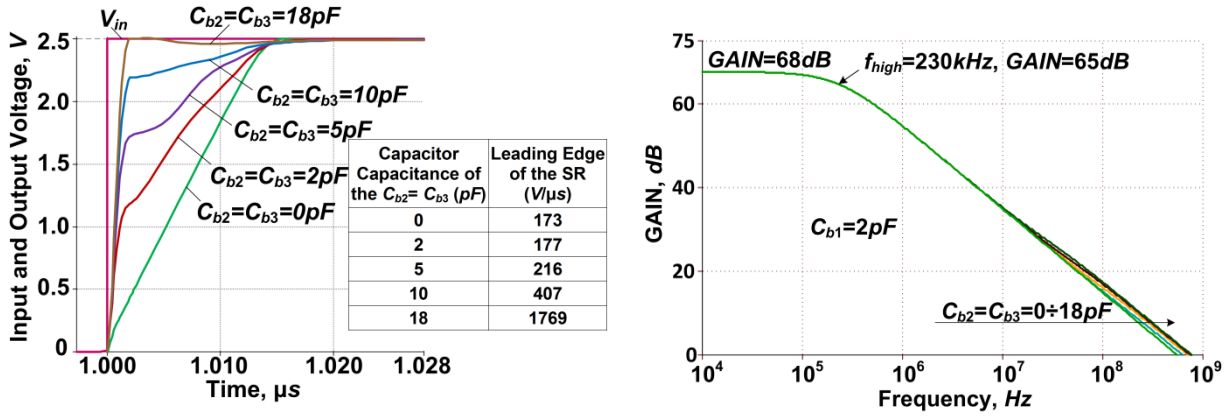
From the equations it follows that the slew rate of the OA of figure 2 in the connection circuit of figure 1 with ideal CM1 and BA is

$$\mathrm{SR} \approx \left(\mathrm{N_c} / 2 + \mathrm{N_c}\right) \cdot \left(\mathrm{dv_{in}^{(+)}} / \mathrm{dt}\right). \tag{7}$$

That is, the limiting values of the SR are determined by the change rate of the input signal, which is typical for inertialess links. The SR is limited from above by the influence of time constants (2), the inertia of current mirror CM1 and the buffer amplifier BA, as well as the presence of parasitic capacitors at input In.1$^{(-)}$ of the OA of figure 1, in practice.

Computer simulation of the ASI circuit with the OA of figure 2 was carried out in PSpice environment with the models of complementary transistors (BJT) manufactured by OOO "S&PE "Pulsar" (Moscow). We investigated transients (figure 3a) with static currents I_1=100μA, I_2=500μA, and resistances of feedback resistors R_1=R_2=1$k\Omega$.

Thus, the *SR* of the leading edge of the OA reaches 330 *V*/μs, the *SR* of the trailing edge is 200 *V*/μs with C_{b2}= C_{b3}=100*pF*, and the transient response time t_{tr} decreases with the 10 % dynamic error zone by more than 10 times on the OA of figure 2. The *SR* of the OA increases from 98 *V*/μs to 966 *V*/μs at C_{b1} = 0.5*pF*, if I_1=I_2=50μ*A* is selected.



(a) (b)

Figure 3. The transient of the AIS scheme on the OA of figure 2 (a) and the AFC of the OA (b).

The amplitude-frequency characteristic of the high-speed OA of figure 2 with an open feedback loop characterizes the graphs of figure 3b. The conclusion follows from the graphs that capacitances C_{b2}, C_{b3} practically do not affect the AFC and the low-signal gain-crossover frequency.

The effectiveness of the developed circuitry solution was tested by implementing the OA of figure 2 on CMOS SiGe TSMC_035_T65 transistors with the width *W*=10μ*m* and the length *L*=0.35μ*m* of the

channel in microcurrent mode $I_1 = 100\ \mu A$, $I_2 = 200\ \mu A$. The corresponding transient characteristics are shown in figure 5 at $C_{b1} = 2pF$ and different values of C_{b2}=C_{b3}=0 ÷ 100pF. The resistances of the feedback resistors are 5$k\Omega$.

Consequently, the *SR* of the micro-power OA with a dual-input-stage current consumption of 100 μA increases by 15 times and reaches 200 $V/\mu s$ in the basis of CMOS technologies, for example, TSMC_035_T65.

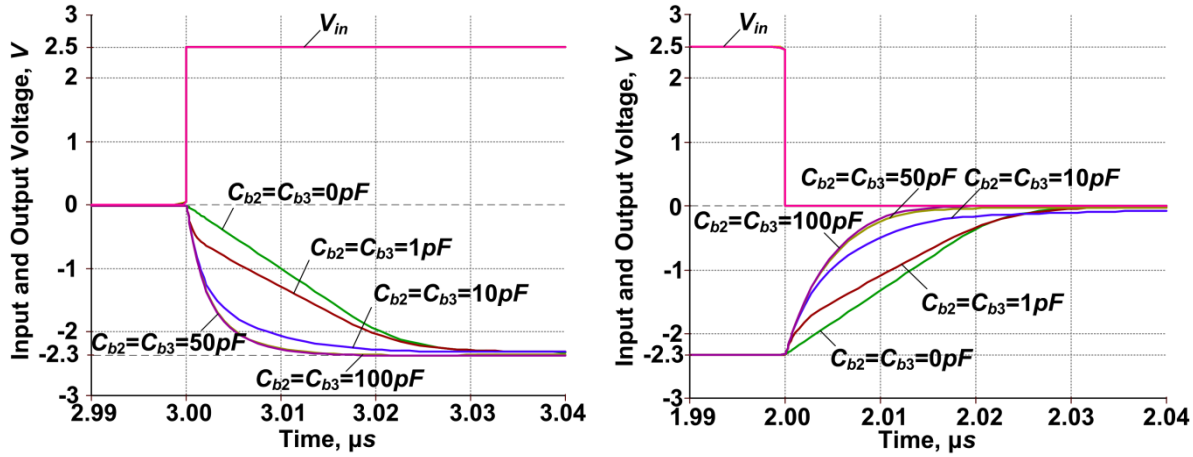


Figure 4. The inverting AIS transient on the CMOS OA of figure 2 for the leading (a) and trailing (b) edges.

4. Differentiating correction circuits in the SOI OA with a differential input

The OAs with a differential input are more universal ECB. An unconventional [27,28] circuit method for increasing the SR in the operational amplifiers of this subclass, including when implemented using the SOI technology will be discussed below. The method is based on introducing a nonlinear differentiating correction circuit (DCC) – C_{b2} capacitor into the well-known classical SOI OA structure [26] (figure 5a and figure 5b).

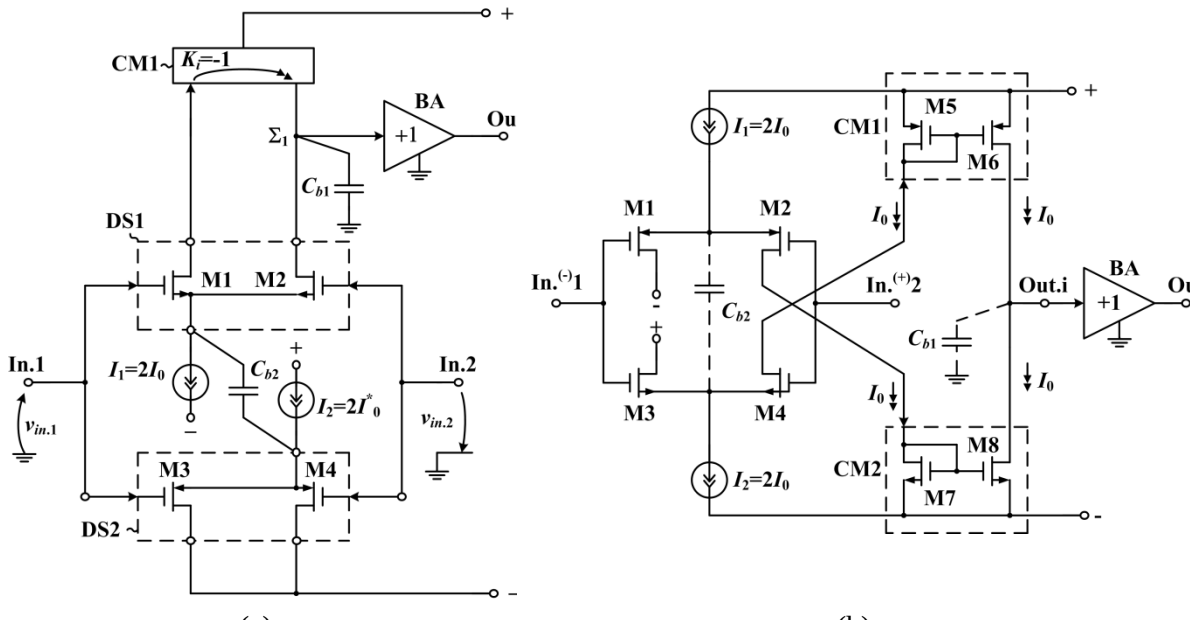
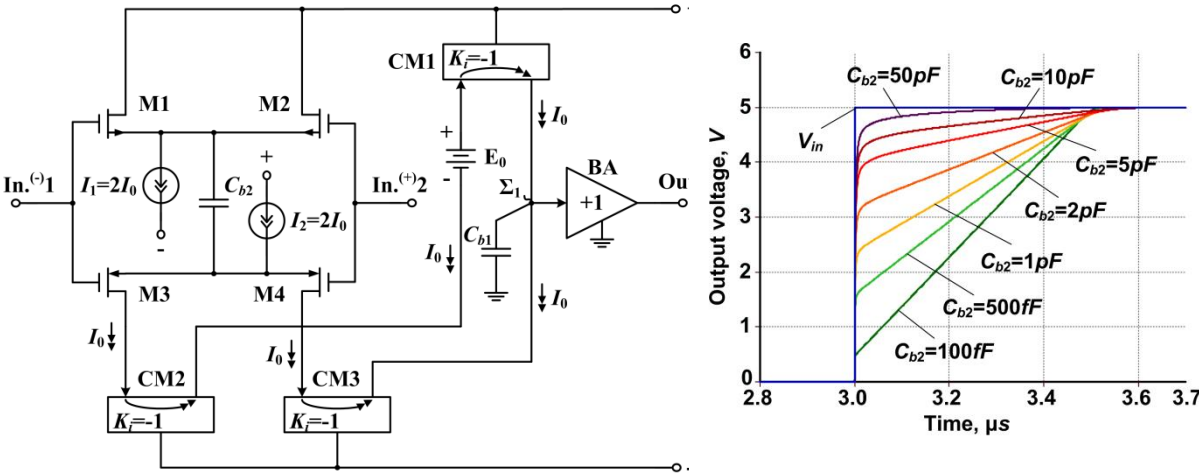


Figure 5. The first (a) and the second (b) SOI OA architectures with a nonlinear differentiating correction circuit of the transient.

The mathematical analysis and computer simulation of the transients of the OA of figure 5 in the large signal operation show that this simple circuitry method [27,28] makes possible to increase the SR by 5-20 times. At the same time, the efficiency of connection of C_{b2} increases with the choice of static currents of the input transistors of the OA within the range of tens microampere.

The introduction of the DCC is promising not only in the input differential stage circuits [27,28], but also in the OA intermediate stages (patent RU 2684500), as well as in the OA buffer amplifiers (patents RU 2668985 and RU 2673003). At the same time, the DCCs on the small signal practically do not affect the low-signal of the AFC of the OA, which is traditionally formed by integrating correction capacitance C_{b1} in the high-impedance node of the OA.



(a) (b)

Figure 6. High-speed CMOS operational amplifier (a) and its leading edge transient (b).

5. Conclusion

The article provides a brief comparative analysis of modern circuitry techniques for improving the dynamic parameters of the OAs in the large signal operation.

The considered method for improving the dynamic parameters of the inverting AIS on the OA provides an increase in the SR by 5-20 times without increasing the current consumption in static mode. The proposed OA architectures are designed to be used in the ADC drivers, cable lines, power amplifiers and other automation devices and control systems.

The use of the array chips as active elements of the OA makes it possible to provide the operability of the analog sensor interfaces at low temperatures, as well as under conditions of radiation exposure [29].

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