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To cite this article: I Donmez et al 2019 J. Phys.: Conf. Ser. 1407 012097

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Improved micronanogenerators based on silicon compatible materials and processing

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Abstract. Our work on all-silicon thermoelectric micro power generation is reviewed including the latest improvements. Our devices use low-dimensional silicon-based thermoelectric material, namely Si and (for the first time) SiGe nanowires. A new redesign leading to a significant reduction in parasitic device thermal conductance and lower electrical resistance has been tested and a route for the integration of a heat exchanger onto it has been recently attempted. Power densities of a few tens of μ W/cm² have been achieved.

1. Introduction

Thermoelectricity offers a way of converting waste heat into electricity. While waste heat recovery scenarios for improving the energy efficiency of engines or industrial processes demand large size thermoelectric generators, energy harvesting in IoT scenarios open a window of opportunity for microgenerators (μ TEGs). In this context, our two groups have collaborated in an approach for devising all-silicon μ TEGs [1]. Silicon itself is not a good thermoelectric material because of its large thermal conductivity but low-dimensional silicon offers a way of circumventing this handicap [2,3].

2. Device description and improvements

The core of the μ TEG is a planar micromachined device featuring a 1 mm² suspended micro-platform, defined by MEMS processes, surrounded by a bulk Si rim as shown in figure 1. The device is built on 500 μ m thick SOI wafers with a 15 μ m thick (110) Si device layer. The platform vertical walls are aligned to (111) planes. Three of the sides contain 1-4 trenches that will be filled with nanowires, and the fourth contains the mechanical supports attaching the platform to the rim and providing the electrical connections to the platform.

Dense arrays of Si and SiGe NWs have been grown on the device as a post-process in a CVD reactor following a Vapor-Liquid-Solid mechanism after seeding selectively the vertical trenches with catalytic gold nanoparticles [4]. NWs grow horizontally from (111) surfaces and eventually bridge the gap between the platform and the Si rim (figure 2). The attachment of the NWs to the silicon walls is quasi-epitaxial, leading to low electric and thermal contact resistances.

PowerMEMS 2018

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1407 (2019) 012097 doi:10.1088/1742-6596/1407/1/012097

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The thermal performance of the microplatform was first enhanced by replacing the long and narrow bulk Si connecting bridges used originally with a thin and wide dielectric membrane with low thermal conductivity reducing the parasitic heat flow between the platform and the rim [5]. The electrical performance of the μ TEG has been also enhanced by decreasing the device internal resistance through redesign and additional processing steps minimizing the metal/Si contact resistance. As a result, the device internal resistance has decreased 7 to 20 times compared to previous designs. Two additional actions attempted to improve the thermal performance of the device have been the substitution of Si NWs by SiGe NWs, which feature a much lower intrinsic thermal conductivity, and the integration of a heat exchanger onto the device. SiGe NWs are obtained following the same process than Si NWs. It is worth mentioning, though, that the average diameter of Si NWs was 100 nm in our case, while SiGe one was 60 nm. Irrespective of the thermal properties of the thermoelectric material, the poor thermal connection of the platform to the environment, precludes a significant part of the available temperature difference to establish across platform and rim unless forced convection is used. In natural convection scenarios, a heat exchanger is instrumental as shown in figure 3. We have devised a route for integrating such an element contacting only the suspended platforms of the four chips present in our $7x7 \text{ mm}^2$ chip in a way that is compatible with the limited robustness of those elements.



Figure 1. Sketch of the unit cell of the thermoelectric microgenerator



Figure 2. Sketch of selective gold nanoparticle seeding with galvanic displacement method and NWs growth by CVD-VLS.



Figure 3. FEM simulations of in-chip temperature distribution at a hotplate temperature of 100 °C when (a) the heat sink is not present and (b) when it is. In the first case, only a fraction of 1K is captured across the rim (heat source) and the micromachined platform (heat sink), while the improved thermal connection to the ambient provided by the heat exchanger increases this ΔT about 30 times.

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3. Performance results

3.1. In-chip thermal and electrical improvements

The impact of the in-chip thermal and electrical improvements mentioned earlier (engineering of the thermal conductance of the platform support and of electrical contacts and connections) has translated into a higher Seebeck voltage and lower device internal electric resistance leading to a much larger power density. Indeed, second generation chips populated with Si NWs show power densities of 0.2 μ W/cm² at 200 °C, which are 20 times higher than first generation devices.

3.2. Replacing Si by SiGe

Replacing Si NWs by SiGe NWs offered a much better power output, around 7 μ W/cm², under the same conditions (figure 4). This dramatic improvement was solely due to the better thermal properties of SiGe NWs, namely lower intrinsic thermal conductivity and smaller diameter. The resulting lower thermal conductance of the SiGe NWs arrays bridging platform and rim allowed to capture a much larger fraction of the externally available temperature difference. Ten times larger Δ T were estimated for SiGe (14 °C vs 1.5 °C). On the other hand, the electrical characteristics of the SiGe NWs ensemble were worse than the ones of Si NWs. The internal device resistance was 30% larger and Seebeck coefficient was measured 30% lower. In any case, these detrimental electrical aspects did not overshadow the terrific thermal improvement.

3.3. Integration of a miniaturised heat exchanger

The results of the simulations were confirmed and the presence of the heat exchanger led to higher ΔT between the cold platform and the hot rim, and consequently to larger Seebeck voltages (figure 5). A significant improvement has been observed for all tested $\mu TEGs$ (Si and SiGe): heat exchanger integrated devices were able to harvest 41.2 μ W/cm² (Si NWs) and 45.2 μ W/cm² (SiGe NWs) when placed on a waste heat source at 100 °C. This is up to 100 times more than similar devices without heat exchanger at the same hot plate temperature. Although SiGe NWs clearly outperformed Si NWs in devices without heat exchanger, the difference between both types of materials apparently diminishes drastically when this element is in place. Although we cannot preclude that part of this lack of difference is due to a still non-optimized heat exchanger itself is enabling most of the temperature difference across the NWs, their thermal properties lose relative importance in terms of power with respect to the electrical ones, which were better for Si NWs in our case.



Figure 4. Obtained power density is much higher for SiGe NWs devices than for Si NW devices clearly pointing to the intrinsic lower thermal conductivity, which is instrumental when the thermal contact to the environment is poor as for devices without heat exchanger.

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1407 (2019) 012097 doi:10.1088/1742-6596/1407/1/012097



Figure 5. The presence of a heat exchanger increases the ΔT than can develop across the micromachined device, and this translates into a much higher Seebeck voltage for a given hot plate temperature. The plot exemplifies the Si NWs case.

4. Conclusions

An all-silicon micro-thermocouple fabricated by means of top-down silicon technologies and bottomup deposition techniques has been optimized by using dense arrays of SiGe nanowires as thermoelectric material, and outperformed the one previously attempted with Si nanowires. Performance boosted even more after assembling a small size heat exchanger reaching power densities in the range of 40 μ W/cm² when resting on a hotplate at 100 °C, which are adequate for powering IoT nodes. Usual IoT targets of 10-100 μ W/cm² would then be achievable at 50-150 °C temperature scenarios under natural convection.

Acknowledgements

This work has been supported by projects TEC2016-78284-C3-1-R (AEI/FEDER, EU) MINAUTO and TEC2016-78284-C3-2-R (AEI/FEDER, EU) SIGGNAL. A Stranz wants to thank European Commission funding through the MSCA COFUND program P-SPERE, GA 665919

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