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Research on topology cascade simulation of power switch converter

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Abstract. With the improvement of the performance of the equipment, the requirement of power supply is improved, it puts forward different requirements on the suitability of power supply, electromagnetic compatibility, power density, output quality, efficiency, development cycle and so on, even in the future, the model of power supply in digital simulation of the whole equipment has already put forward the preliminary request, Therefore, the simulation research of power supply is imminent. Through the tireless efforts of power engineers, a variety of basic topology simulation model has been readily available, but given the optimal design and diversification of power supply requirements, a single basic topological model is obviously far from the degree of engineering applications. This paper, inspired by the basic modelling method, provides an effective method for the simulation research of the power system through the research of the topological mutual cascaded modelling.

1. Introduction

With the popularization and development of the network and the intelligent equipment, the power supply of the equipment is also put forward higher requirements. In the early stage of equipment application by digital means to the early simulation of the application, can effectively detect the failure of the earlier problems of the model, can greatly improve the reliability and practicality of the product.

It is obviously more necessary and practical to simulate the cascade topology power supply with the simple power supply with relative basic topology.

With regard to the power switch converter, there are four basic topologies of single end converters: BUCK, BOOST, Buck-boost, Cuk.

The standard circuit parameters for these four basic topologies are shown in table 1:

Table 1: CCM mode standard type circuit parameters

Name	M(D)	e(s)	j(s)	Le	Ce
BUCK	D	V/D2	$\frac{V}{R}$	L	C
BOOST	1/D'	$V(1-\frac{sL}{D'^2R})$	$\frac{V}{D'^2R}$	$\frac{L}{D'^2}$	C
BUCK-BOOST	-D/D'	$-\frac{V}{D^2}(1-\frac{sDL}{D'^2R})$	$-\frac{V}{D'^2R}$	$\frac{L}{D'^2}$	C
Cuk	-D/D'	$-\frac{V}{D^2}(1-\frac{sD^2L_1}{D'^2R}+\frac{s^2L_1C_1}{D'})$	$-\frac{V}{D'^2R}(1-\frac{sD'C_1R}{D'^2})$	$\frac{D^2L}{D'^2}$	$\frac{C_1}{D^2}$

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Steady and dynamic small signal characteristics are shown in table 2:

Table 2: CCM Mode steady state and dynamic small signal characteristics

Name	M(D)	$\frac{\hat{v}(s)}{\hat{v}g(s)}\|\hat{d}g(s)=0$	$\frac{\hat{v}(s)}{\hat{d}g(s)}\|\hat{v}g(s)=0$
BUCK	D	$\frac{D}{LC_s{}^2+\frac{L}{R}s+1}$	$\frac{V_g}{LC_s{}^2+\frac{L}{R}s+1}$
BOOST	1/D'	$\frac{1}{D'}\cdot\frac{1}{LeC_s{}^2+\frac{Le}{R}s+1}$	$\frac{V_g}{D'^2}\cdot\frac{1-\frac{L_e}{R}s}{LeC_s{}^2+\frac{L_e}{R}s+1}$
BUCK-BOOST	-D/D'	$-\frac{D}{D'}\cdot\frac{1}{L_eC_s{}^2+\frac{L_e}{R}s+1}$	$-\frac{V_g}{D'^2}\cdot\frac{1-\frac{L_eD}{R}s}{L_eC_s{}^2+\frac{L_e}{R}s+1}$
Cuk	-D/D'	$-\frac{D}{D'}\cdot\frac{1}{\Delta(s)}$	$-\frac{V_g}{D'^2}\cdot\frac{L_eC_eD's^2-\frac{L_e}{R}s+1}{\Delta(s)}$

$$\Delta(s)=C_eL_2C_2R_s{}^3+C_eL_2s^2+(C_e+C_2)R_s+1$$

2. Power supply Topology Cascade application

In some specific applications, a single simple topology does not meet the requirements of use, this time to adopt a special topology or a cascading topology. Take a device to the requirements of the power supply as an example: large power, input and output isolation, output to input as a step-up topology, load has broken short circuit characteristics.

According to the above description, the power is large, isolation boost can choose the whole bridge topology, but in order to limit the characteristics of load short-circuit, it is obvious that the buck topology has a natural advantage, so you can combine the advantages of both, the buck cascaded full bridge topology. The topology of Buck cascaded Whole bridge can be divided into two types: voltage type and current type according to the feed form. Buck Voltage-fed full-bridge topology diagram See Figure 1:

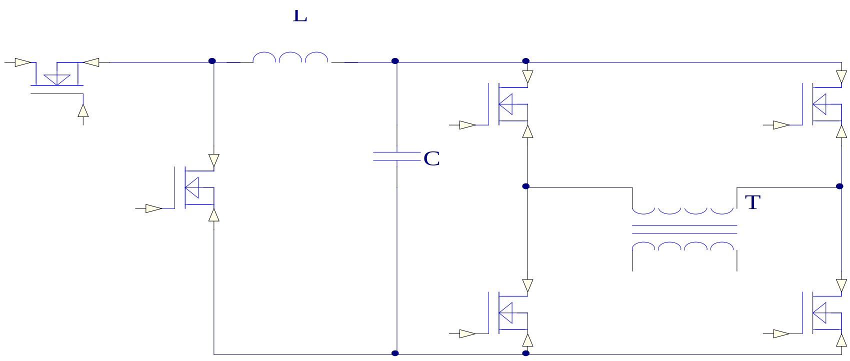

Figure 1. Buck voltage feed full Bridge block diagram

Buck Current feed full bridge topology diagram See Figure 2:

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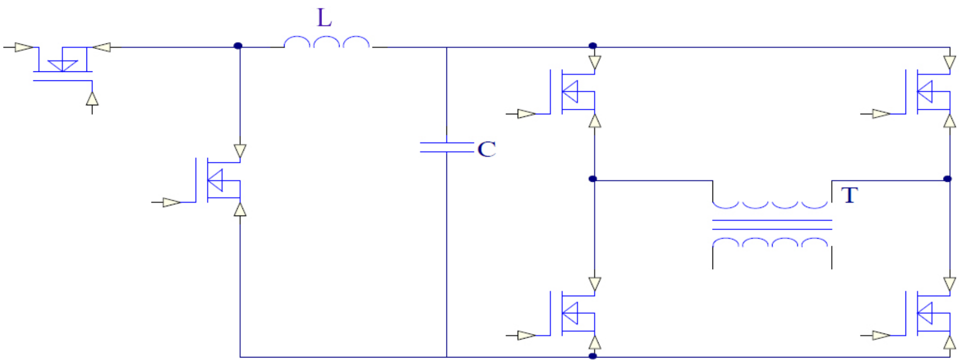

Figure 2. Buck Current feed full bridge block diagram

The difference between current type and voltage type is mainly two points: 1, the output of Buck has no filter capacitance (equivalent capacitance which is equivalent to secondary output capacitance refraction); 2, the bridge between the two of the bridge arm does not have a dead zone, but by a certain common time, in common, because of the high impedance of the inductance of the bridge, the input become a constant current source of power. These features should be fully considered when modelling.

3. Modelling of switching converters

In order to study the dynamic characteristics of DC-DC converters containing AC small signal components, a variety of AC small signal analysis methods have been proposed at present. The basic ideas are as follows:

1） Average of variables is obtained. Conditions: To satisfy the small ripple and low frequency hypothesis, the small ripple hypothesis: The converter is far less than the switching frequency of the converter; Low frequency hypothesis: The frequency of the AC small signal is much smaller than the switching frequency of the converter.

2） An average variable expression is established according to the running state of the converter in a switching period for the variable of interest.

3） Decompose the average variable and find the static working point and the nonlinear AC small signal equation.

4）Linearization of the nonlinear equation: the small signal product in nonlinear equation is neglected, and the linear small signal analytic model is obtained. Condition: satisfies small signal hypothesis, small signal assumes: the amplitude of the alternating component of each variable in the circuit is far less than the corresponding DC component.

There is a state space averaging method with good operability. By establishing the state equation, the state matrix A, the input matrix B, the output matrix C and the transfer matrix E, the concrete methods of operation are no longer repeat.

Taking the buck current-fed Full-bridge as an example, the dynamic block diagram is shown in Figure 3:

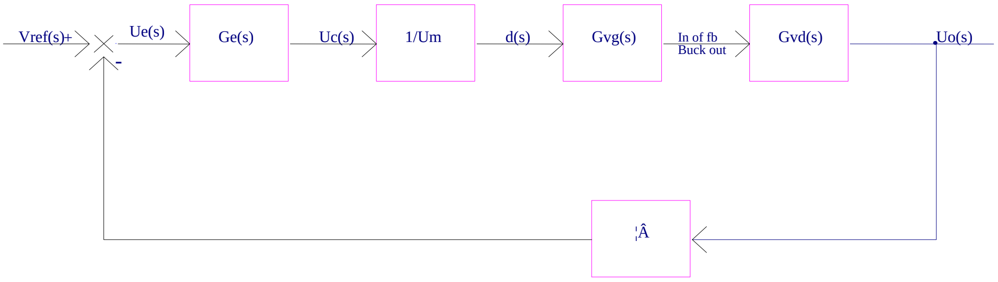

Figure 3. Buck Current feed full bridge dynamic diagram

Ge(s): Transfer function of compensation network

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Um： PWM Triangle Amplitude Value
β： Sample ratio
Gud(s)： Transfer function of buck output to duty ratio in open loop system
Gug(s)： Transfer function of total bridge output to full bridge input when the system is Open-loop

where GUD (s) is the transfer function of the output pair duty ratio of the basic topology buck, known as Um, β, Ge (s) is being asked, and then to solve Gug (s) with state space averaging.

Suppose the whole bridge parameter is: Change ratio 1:15, output 4.5kv/0.1a,β=1/1000, output inductance =10uh, output capacitor =0.1u. When the capacitance inductance is small, the transfer function of the full bridge in the buck current feed full bridge is equivalent to the proportional function (calculated process omitted).

4. Simulation application of the model

The most important purpose of modeling post-simulation is to determine its stability and dynamic performance, is designed and according to the simulation results to design the compensation network to achieve the expected requirements. The stable and dynamic response of switching converters is based on three points as below:

1. Crossing frequency is about 1/4~1/5 switching frequency
2. The slope of the gain curve near the crossing frequency is passed by-1.
3. Phase Margin ≥45°

The basic parameters are as follows:

$\omega := 2\pi \cdot f \quad s := j \cdot \omega \quad j := \sqrt{-1} \quad fs := 120\mathrm{kHz} \quad fc := \frac{fs}{4} = 3 \times 10^{4}\,\frac{1}{s}$

$Vg := 330 \quad D := 0.9 \quad L := 1000\mu\mathrm{H} \quad RL := 0.05\Omega \quad C := 22.5\mu\mathrm{F}$

$Rc := 0.02\Omega \quad R := 125\Omega$

$$\omega 0 := \frac{1}{\sqrt{L \cdot C}} = 6.667 \times 10^{3}\,\frac{1}{s} \qquad Q := \frac{1}{\omega 0 \cdot \left[\frac{L}{R} + (RL + Rc) \cdot C\right]}$$

$$\omega z1 := \frac{RL}{L}$$

$$\omega zc := \frac{1}{Rc \cdot C} \qquad fp0 := \frac{1}{2\pi\sqrt{L \cdot C}} = 1.061 \times 10^{3}\,\frac{1}{s}$$

$$\omega zp := \frac{1}{R \cdot C} \qquad fz0 := \frac{1}{2\pi \cdot (Rc \cdot C)} = 3.537 \times 10^{5}\,\frac{1}{s}$$

Main circuit section:

$$G(f) := Vg \cdot \frac{1 + \frac{j \cdot 2\pi \cdot f}{\omega zc}}{1 + \frac{j \cdot 2\pi \cdot f}{Q \cdot \omega 0} + \frac{(j \cdot 2\pi \cdot f)^{2}}{\omega 0^{2}}} \qquad \theta(f) := \frac{\arg(G(f))}{\pi} \cdot 180$$

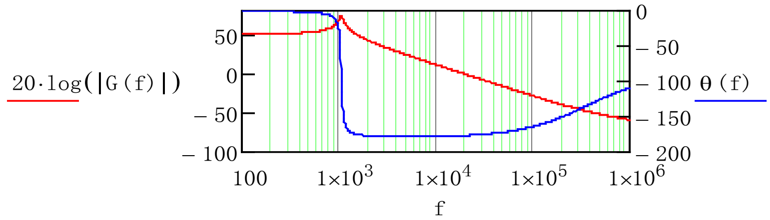

Figure 4. Main circuit Bode diagram

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From the graph above, we can calculate the voltage loop crossover frequency:

$f := 10\text{kHz}$

$\text{root}(20\cdot\log(|G(f)|), f) = 19.318\cdot\text{kHz}$

Then, we can calculate the voltage loop phase margin:

$\theta(\text{root}(20\cdot\log(|G(f)|), f)) + 180 = 3.328$

Compensation and the rest of the circuit section:

$R1 := 1\text{k}\Omega \qquad k := 1.4 \qquad f := 1, 100 .. 100\text{kHz}$

$$Fm := 15\cdot\frac{1}{1000}\cdot\frac{1}{3} = 5\times 10^{-3}$$

$$R2 := \frac{R1}{k\cdot Fm\cdot|G(fc)|} = 3.444\times 10^{5}\Omega$$

$$C2 := \frac{1}{(fp0 - 100\text{Hz})\cdot R2\cdot 2\pi} = 4.808\times 10^{-10}\text{F}$$

$$C1 := \frac{1}{R1\cdot fc\cdot 2\pi} = 5.305\times 10^{-9}\text{F}$$

$$K(f) := \frac{(1 + j\cdot 2\pi\cdot f\cdot R2\cdot C2)\cdot(1 + j\cdot 2\pi\cdot f\cdot R1\cdot C1)}{R1\cdot C2\cdot j\cdot 2\pi\cdot f}$$

$$H(f) := K(f)\cdot Fm \qquad \theta 1(f) := \frac{\arg(H(f))}{\pi}\cdot 180$$

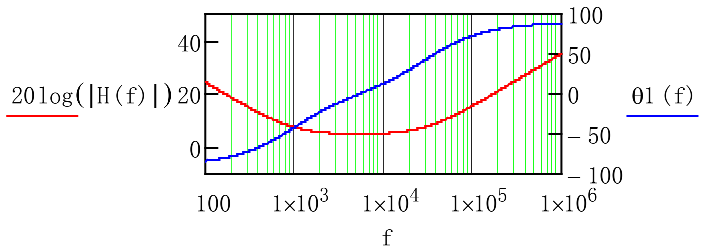

Figure 5. Compensation and the rest of the circuit Bode diagram

Total open-loop transfer function:

$Tv(f) := G(f)\cdot H(f)$

$$\theta 2(f) := \frac{\text{angle}(\text{Re}(Tv(f)), \text{Im}(Tv(f)))}{2\cdot\pi}\cdot 360 - 360$$

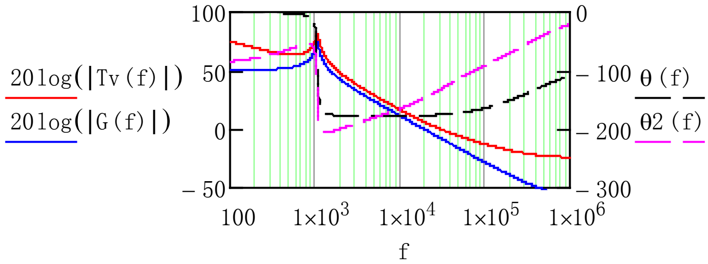

Figure 6. Total open-loop circuit Bode diagram

From the graph above, we can calculate the voltage loop crossover frequency:

$f := 30kHz$

$\mathrm{root}(20\log(|Tv(f)|), f) = 30.214 \cdot kHz$

Then, we can calculate the voltage loop phase margin:

$\theta 2(\mathrm{root}(20\log(|Tv(f)|), f)) + 180 = 48.393$

5. Conclusion
The above simulation results show that the power switch converter meets the design requirements completely after compensating the network. In this paper, the basic model and engineering modelling are combined, the application of modelling is extended to more practical and effective fields, this method is not only suitable for the topological cascade and other forms mentioned in this paper, but also improves the application range of digital simulation of power supply design, and lays a foundation for future system simulation data embedding.

Acknowledgments
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