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Design System on Chip PreAmp Embedded on Electrocardiograph Based 0,35 CMOS Technology

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Abstract. The heartbeat has frequency from 0.1 Hz to 150 Hz. The electrical signal which is resulted from the heartbeat has amplitude of 100μV - 4 mV. In order that the amplitude can be sampled by the ADC, it must be amplified 100 times, thus amplitude amplifier about 60dB it is required. In this research, the researcher designs a System on Chip ECG based on Einthoven method which has 3 Leads, so amplitude can be amplified based on the different voltage of each Lead. Differential amplifier is an initial amplifier that will amplify the difference of two inputs of voltage. Differential amplifier is designed using 3 operational amplifiers (op-amp). Op-Amp A1 and Op-Amp A2 are used for detecting and sampling the difference of two input levels. The function of Op-Amp A3 is to amplify the difference results of the sampled input level. Op-Amp A1, Op-Amp A2 and Op-Amp A3 are designed with offset voltage of Vos ≈ 0V, Open Loop Gain ≈ 66.42 dB, Phase Margin ≈ 400 and Unity Gain Bandwidth ≈ 160.7MHz. Method of the research is design and simulation using 0.35 micro Mentor Graphics technology. Result of the research is a layout of PreAmp for System on Chip ECG with gain of 62.4 dB and 0.034 mm2 area.

1. Introduction

Electrocardiograph (ECG) is a medical device that is used to measure the electrical activity of the heart. The method used is measuring the biopotential difference on every Lead. ECG signal is an AC signal with a bandwidth from 0.1 Hz to 150 Hz and amplitude of 100 uV up to 4 mV [1,2] .

The amplitude signal will be amplified to 60 dB (AV≈ 100 times) by the Pre Amplifier so that it can be processed by the ADC. The heart's biopotential pre amplifier used a circuits of operational amplifiers commonly called as Instrumentation Amplifier (IA).

Instrumentation amplifier consists of differential amplifier and buffer. The differential amplifier circuit is shown in fig 1. The differential amplifier is chosen because of its ability to remove common mode signals, so it can reduce the effect of noise / interference disturbing the ECG signal

The main components of the IA are three pieces of OpAmp (A1, A2 and A3). OpAmp A1 and OpAmp A2 are used for detecting and sampling the voltage difference between the two Leads. The function of OpAmp A3 as a buffer. Amplification of amplifier is determined by the value of Rgain.

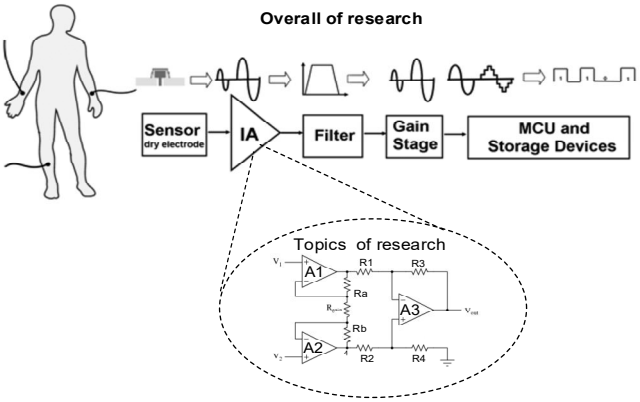

Figure 1. Block diagram of Research

The Instrumentation Amplifier as PreAmp ECG must have of several requirements as follows [3,4].

- Have a high input impedance (Differential > 2.5 Mohm and common-mode > 100 Mohm).
- High CMRR so that have ability to reduce the noise (CMRR > 80 dB).

Assuming R1 = R2 and R3 = R4, the amount ofdifferential can be determined:

$$A = \frac{Vout}{V1 - V2} = \left[1 + \frac{Ra * Rb}{Rgain}\right]\left[\frac{R3}{R1}\right]$$

The differential is a lot of influencedby the value of R*gain*.

2. Transconductance CMOS OP AMP (OTA)

Function of op-amp on IA is used on sampling of differential voltages and buffer process. Op-amp requirements and specifications on ADC are [5,6].

- Gain Open Loop (AoL) ≥ 2^{N+2} V/V.
- Gain Open Loop (dB) ≥ 20.Log 2^{N+2} V/V.
- Gain Close Loop (AcL) = 2 V/V
- Frequency Unity (fu) ≥ 0,22(N + 1) $f$clock.

Fig. 2 is op-amp OTA circuits. Differential gain (M1-4) provides two inputs, inverting and non inverting, which cause noise and offset. High gain (M9-7) is almost similiar to not gate if opamp drives low loads, then it is followed by buffer stage, and current M5 (IM5) resulted from current mirror circuits.

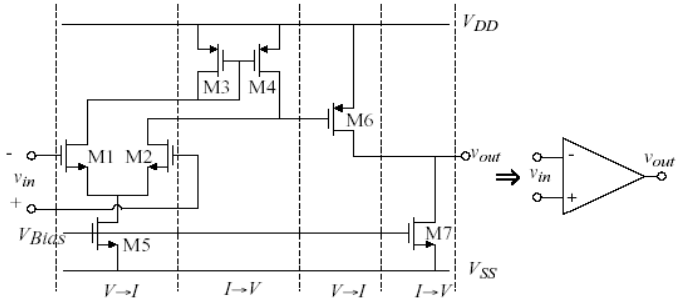

Figure 2. Diagram block of OTA Circuit

Idealop-amp has several characteristics namely unlimited open loop mode gain (AoL..), close loop mode gain = 1, unlimited input impedance, value of output impedance is nearly 0, unlimited gain of bandwidth, value of Vout=Av (V+V-), with Av used on design for open loop mode gain.

All oop-amps have restriction on its operating voltage range. CMIR limit (common input mode range) is border range scale of each op-amp input. Beyond the limit, it will cause cause output distortion or truncated.

$$CMR^{-} = V_{SS} + \sqrt{\frac{I_{D5}}{\beta_1}} + V_{in(\max)} + V_{DS5(sat)} \geq 90\%.V_{OS}$$

$$CMR^{+} = V_{DD} - \sqrt{\frac{I_{D5}}{\beta_3}} - \left|V_{TO3}\right|_{(\max)} + V_{in(\min)} \leq 90\%.V_{OS}$$

Function of current mirror as bias current source for MOS components is as controller or as driver of current source towards control current, e.g. Iref = Iout.

In fig 2, op-amp of 2 transconductance stages can be analyzed as follows:

$I_{D1} = I_{D2} = \frac{ISS}{2}$

SlewRate (SR) = $\frac{ID5}{Cc}$ $I_{SS} = I_{D5}$, $I_{D3}=I_{D4}$,

Gain of stage 1

$$AV1 = \frac{gm1,2}{gds2 + gds4} = \frac{2gm1,2}{Iss(\lambda 2 + \lambda 4)}$$

Gain of stage 2

$$AV2 = \frac{gm6}{gds6 + gds7} = \frac{gm6}{I_{D6}(\lambda 6 + \lambda 7)}$$

where
gds = parameter of transconductance drain to source
λ = parameter of channel length modulation

Transconductance type amplifiers designed with CMOS components have specifications suitable for ADC applications with capacitive loads, and large input impedances so that can to minimize noise. Specification of op amp type OTA with 2 stage circuit is shown in table 1[5].

Table 1. Parameter design of OTA

No	Parameter	Formula	Value
1	Gain AoL	≥ 20 log 2 $^{N+2}$	≥ 60 dB
2	Gain AcL	$(C_1 + C_2)/C_2$	≈ 2 V/V
3	Gain Bandwitdh	≥ 0,22(N-1).fclk	≥ 158,4Mhz
4	FcL (3dB)	≥ β*fu	≥ 79,2Mhz
5	Frequency 3dB	≥ fcL,3dB/AoL	≥ 1,32Mhz
6	Phase Margin	-0 ^{0}<PM< -180^0	-45^0
7	Slew Rate (SR)	I_{ss}/C_c	160V/uS
8	Noise (Sn)	(16KT)/3gm1,2	5ns/Hz
9	±CMR	≈ 90% OS	± 2,673 V
10	Output swing	≈ 90% ± VDD	± 2,97 V
11	Power Disipation	≤ IT*(V_{DD}+V_{SS})	≤ 5mW
12	Load Capacitif	≈ Cc/0,22	≈ 1,15pF

In designing a 2 stage OTA op-amp with topology likes figure 3, the design steps can be started as follows:

1. Determine the value of tansconductance *gm1,2* assuming fc = 250 Hz.
   $gm = f_c * 2\pi * C_c$, where Cc is the capacitor compensation, Cc = 0.25pf, then gm = 392.5µA / V, for gm2 = gm1 so the drain current passing through both components of M1 and M2 is the same, ID1 = ID2 = ISS / 2.
   $I_{D1} = I_{D2} = \frac{SR}{2} C_C = 20\mu A$
   $I_{D6,7} = SR(C_C + C_L) - 2\left(1 + \frac{C_L}{C_C}\right) I_{D1,2} = 224\mu A$
   $g_m = \sqrt{2k_n \frac{W}{L} I_D}, \rightarrow I_{D1,2} = \frac{g_{m1,2}^2}{2k_n \frac{W}{L}}$

   Where with AMS 0.35µm technology obtained parameters
   $k_n = 189\mu A/V^2$, $k_p = 64\mu A/V^2$,$V_{THN} = 0{,}46V$, $V_{THP} = -0{,}68V$.

Therefore
$\left(\frac{W}{L}\right)1{,}2 = \frac{392{,}5^2}{2.189.20} = 20.3778. \rightarrow L_{1,2} = 0{,}35\mu m$
So $W_{1,2} = 7{,}13\mu m$

2. To determine the size of M3, M4 and M5 use CMR input with transistors in the saturation region.
   $V_{DS} > V_{GS} - V_{TH}$
   $CMR^+ = -V_{SS} - (V_{GS} - V_{THN})_5 - V_{GS2}$
   Where is $I_{D1,2} = \frac{K_n}{2}\frac{W}{L}(V_{GS1,2} - V_{THN})^2$
   $(V_{GS} - V_{THN})_5 = 0{,}127\ V$
   Therefore $V_{GS1,2} = 0{,}5\ V$ and $V_{GS5} = 0{,}587\ V$
   $ID_5 = \frac{K_n}{2}\frac{W}{L}(V_{GS5} - V_{THN})^2$, so that$\left(\frac{W}{L}\right)_5 = 26{,}24$
   When$L_5 = 0{,}35\mu m$, then $W_5 = 9\mu m$
   $CMR^- = (V_{GS} + V_{THP})_4 - V_{DD}$
   Is known $(V_{GS} + V_{THP})_4 = 0{,}627V$ and $I_{D3} = I_{D4} = 40\mu A$
   $= \frac{K_P}{2}\frac{W}{2L}\left(V_{GS3,4} + V_{THP}\right)^2$, that $\left(\frac{W}{L}\right)_{3,4} = 6{,}4$
   So, for $L_{3,4} = 0{,}35\mu m$ then $W_{3,4} = 2{,}2\mu m$

3. To find the width of W by using VGS 5 = VGS 7 with ID7 = ID6 = 224µA can be recalculated:
   $I_{D7} = \frac{K_n}{2}\frac{W}{L}(V_{GS7} - V_{THN})^2$ with $V_{GS7} = 0{,}587$
   So $\left(\frac{W}{L}\right)7 = 147$. When $L_7 = 0{,}35\mu m$,
   then $W_7 = 51\mu m$, and $I_{D7} = I_{D6} = 224\mu A$.
   The value of M6 can be determined as follows:
   $(V_{GS} + V_{THP})_6 = (V_{GS} + V_{THP})_4 = 0{,}627V$
   $I_{D6} = \frac{K_P}{2}\frac{W}{L}(V_{GS6} + V_{THP})^2$. So, $\left(\frac{W}{L}\right)6 = 35{,}6.$
   For $L_6 = 0{,}35\mu m$ then $W_6 = 12{,}5\mu m$ and $g_{m6} = 1010{,}3\mu A/V$.

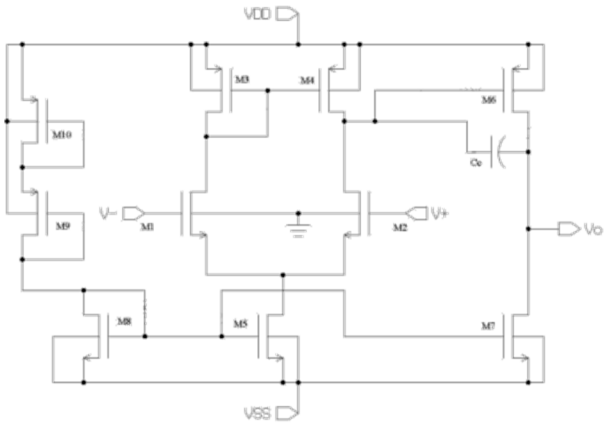

Figure 3. Basic schematic of CMOS OTA

With λ_N = 0.05V^{-1} and λp = 0.15V^{-1}, for technology 0.35 µm available of result Open Loop Gain (AoL) = 67,9 dB, Phase Margin (PM) = 59.2^0, Slew Rate (SR) = 289.86/µS and CMR = + 2.68V and – 2.85V.

Table 2. W/L OTA

MOS	$\frac{W}{L}$µm	Drain Current µA
M1	42/0.35	20
M2	42/0.35	20
M3	2.2/0.35	20
M4	2.2/0.35	20
M5	9/0.35	40
M6	12.5/0.35	224
M7	51/0.35	224
M8	0.9/0.35	4
M9	0.6/10	4
M10	0.6/10	4
Cc	0.25 pf	

3. Instrumentation Amplifier

Fig 4 shows the schematic of instrumentation amplifier for biomedical applications. This instrumentation amplifier based on OTA , which actually could accomplish the desired features of high common mode rejection .The Instrumentation Amplifier is based on a current-balancing technique . The differential inputs voltage, Vin1 and Vin2, are converted into a Differential Currents[7]

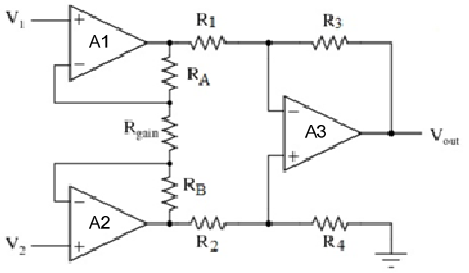

Figure 4. Instrumentation Amplifie

A1, A2 and A3 are OTA. For ideal conditions, it is determinedthat Av = 60dB, RA = RB = 10K and R1 = R2 = R3 = R4 = 100K, so that it is obtained the value of R*gain*:

Av = 20 log $[\frac{Vout}{V1-V2}]$= 60dB

Av ≈ 1000 V/V

$1000\left[1+\frac{RA*RB}{Rgain}\right]\left[\frac{R3}{R1}\right]$, R*gain* = 100K

4. Result of Simulation

A. Transconductans Amplifier OTA

The testing simulation uses CAT software mentor graphicsAMS technology 0,35µm. The testing is focused on the characteristics of the op-amp circuit applied into the ECG.

1. DC Offset (Vos) and Output Swing (OS).
   The Op Amp of OTAis giventhe power supply DC 3.3 V and - 3.3 V. The results of the simulation as in figure 5.

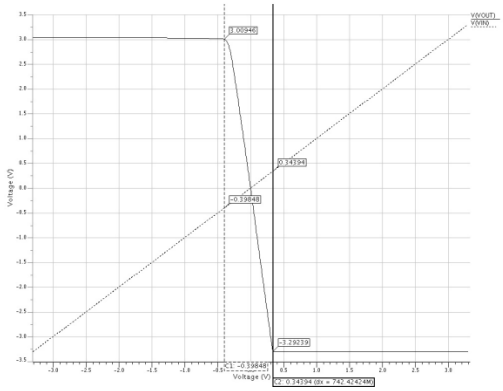

Figure 5. Characteristic of Vos and Output Swing

On the figure above, it is obtained that the value of voltage output swing (OS) with OS + = 2,87V and OS - = -3,19V. And the offset voltage approaches 0V where the meeting point (0,0) is equal to 0,0008V.

2. CMR with Input AC
   The testing of CMR using of level input AC is shown in Figure 6 below.

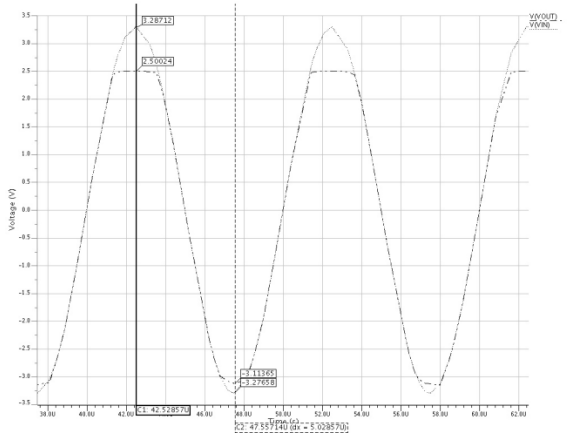

Figure 6. The result of testing CMR

The results of simulation obtained the value of CMR = + 2.673V and - 3V. There is a shift of the graph from the results of the calculation, which means there is value of W / L thatcan be lowered again. Factors shift from the ideal value can be attributed to the influence of in capacitor and the value of Kn, Kp is variable.

3. Testing of Slew Rate, AoL and Phase Margin

   The testing of Slew rate are shown as follows:

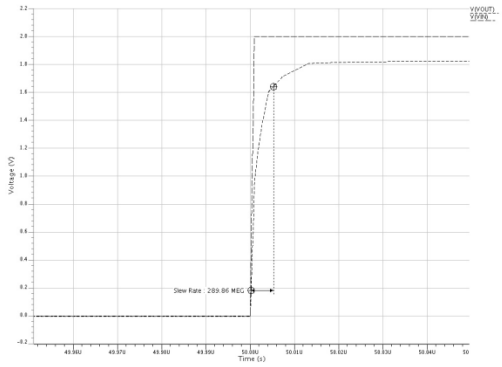

Figure 7. The Simulation Result of Slew Rate

The result of SR obtained shows that there is difference between calculation and simulation. SR calculation = 289.86V / μS and SR simulation = 130.34 V / μS. Settling time is 14nS for 1%.

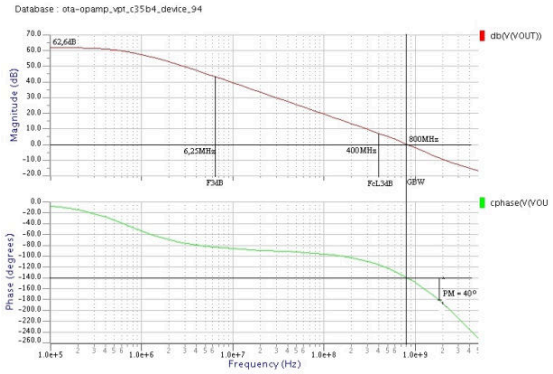

Figure 8. Simulation of AoL and PM

The calculation of simulation for W / L using the value Kn = 175μA / V and Kp = 60μA / V, obtained the value of AOL = 66.42 dB, PM = 400 and GBW = 160.7 MHz.

B. Instrumentation Amplifier (IA)

Input of simulation is a sinusoidal input and PWL signal with the characteristic of ECG.

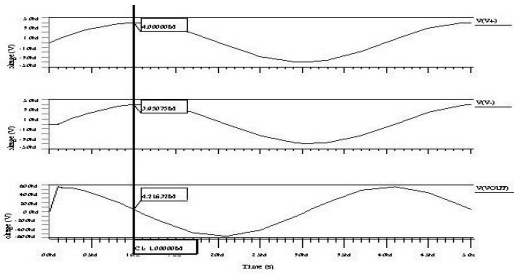

Figure 9. Simulation of IA with sinusoidal input

Input V + and V- is a sinusoidal voltage with delay V = 100 μs. The simulation results obtained of differential AV ≈ 62.4 dB. The result of gain simulation, the value is bigger 2,4 dB compared to calculation result. This is due to the instability of the OTA design, ie, the AOL simulation value is 66.42 dB from should be 67.9 dB.

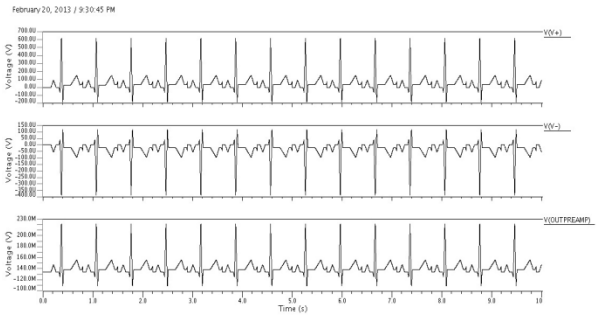

Figure 10. Simulation of IA with input PWL ECG

The method of simulation is given V+ input PWL ECG normal, while V- given input inverse of V+. To avoid the negative level, added to the DC bias of 0.24 mA so that occur a phase shift toward the positive level. It aims to PWL ECG signal can be sample perfectly to the ADC.

C. Layout IA as a PreAmp

Pre Amp layout consists of 3 layouts of Op Amp and 7 Resistor as shown in the fig 11. Size of layout is 0.034 mm2.

From simulation, obtained result power consumption is 0.065 mW, range of voltage - 3,3 V until +3,3 V.

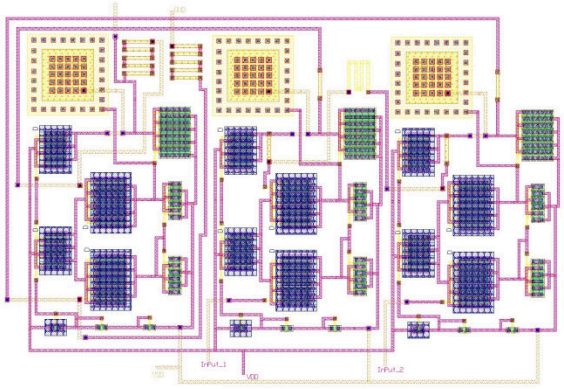

Figure 11. PreAmp Layout

5. Conclusion

The minimum requirements of differential Pre Amp for differential the ECG signal is 60 dB. The result of simulation shows the differential Pre Amp 62.4 dB. These results are ideal. If the enlarged differential, noise also increases. Output IA added DC bias of 0,24 mA. DC bias is used like a phase shifting toward a positive level, so that the rule of minimum sampling is1 LSB in ADC is full field. The resulting of size layout is 0.034 mm2.

References

[1] S. Y. Lee and C.J. Cheng, "Systematic design and modeling of a ota-c filter for ecg detection,"IEEE Transactions on Biomedical Circuits and System, Vol 3, 2009, pp 53-64.

[2] K.A.Ng and P.K.Chan, "A CMOS Analog front end IC for portable ECG/EEG Monitoring Application", IEEE Transactions on Circuits and System, 52(11):2335-2347.

[3] T. Kugelstadt, "Getting the most out of Instrumentation Amplifier design", Analog Application Journal, 2005, 18(12), pp 25-30.

[4] H. Wu and Y.P. Xu, "A low voltage low noise cmos intrumentation amplifier for portable medical monitoring system", IEEE-NEWCAS, pp 295-298.

[5] J. Baker, CMOS Circuit Design, Layout and Simulation, 3rd Edition IEEE Press on

Microelectronic System, Wiley Pub, New Jersey, 1998, pp 711-738.

[6] J. Kolezynski, "Design of Operational Amplifier with low power consumption in 0,35 μm Technology" 14th International Conference Mixdes 2007 Ciechocinek, Poland, 21-23 June 2007.

[7] T. Raj Kumar, M. Ganga Ram and M. Maheshwar, "A new high performance CMOS differential amplifier", International Journal of Electronic Engineering Research, Vol 1 no 2, 2009, pp 147-154.