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A Low Cost 4 bit 16 Giga-sample-per-second Analog-to-digital Converter for Radio Astronomy

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Abstract

In this study, a 4 bit, 16 giga samples per second analog-to-digital converter (ADC) printed circuit board assembly (PCBA) was designed, manufactured, and characterized for digitizing signals from radio telescopes. For this purpose, an Adsantec ANST7123-KMA flash ADC chip was used. Because this design of chip is not followed the serial ADC JESD204 standard completely, we used a novel channel bonding scheme developed in our previous project for the high-speed serial data input alignment. The PCBA was equipped with a field-programmable gate array (FPGA) mezzanine card (FMC) connector. FMC allowed us to use the FPGA evaluation board by Xilinx as the testing platform. The PCBA enables data acquisition with a wide bandwidth and simplifies the intermediate frequency section. In the current version, the PCBA and the chip exhibit an analog bandwidth of 16 GHz, which facilitates a second Nyquist sampling. The following minimum to maximum performance parameters were obtained from the first and second Nyquist zones: a spurious-free dynamic range of 18–33 dB and an effective number of bits of 2.1–3.7 bits. The board will be ported to the Collaboration for Astronomy Signal Processing and Electronics Research environment, which is open for use by non-profit scientific teams, including the Event Horizon Telescope.

Key words: Radio astronomy

Online material: color figures

1. Introduction

The EHT is an international collaboration that has formed to continue the steady long-term progress on improving the capability of Very Long Baseline Interferometry at short wavelengths in pursuit of directly deteciton of supermassive black holes. This technique of linking radio dishes across the globe to create an Earth-sized interferometer, has been used to image a supermassive black hole (The EHT Collaboration et al. 2019a).

By linking together existing telescopes using novel systems (The EHT Collaboration et al. 2019b), the EHT leverages considerable global investment to create a fundamentally new instrument with angular resolving power that is the highest possible from the surface of the Earth. Over the coming years, the international EHT team will mount observing campaigns of increasing resolving power and sensitivity, aiming to bring black holes into focus.

Sensitivity can be improved by adding more telescope into the array. But increasing the number of telescopes is a difficult task. Another method for increasing the sensitivity of the EHT is to capture more energy from black hole targets at each EHT site. Because black holes emit radiation at many frequencies, we can capture more energy from the black hole targets at each site by increasing the range of frequencies that are recorded during EHT observations. This in turn requires electronic systems and recording systems that operate at higher speeds. Wider the bandwidth is at a cost that is orders of magnitude smaller than increasing the number of telescopes. The sensitivity can be increased by using wider bandwidths, which requires in faster digitization at each site.

In 2017, we received funding for our study entitled "Black Hole Astrophysics in the Era of Distributed Resources and Expertise" from an international collaboration project called "Partnerships for International Research and Education." University of Arizona received primary grant from the National Science Foundation, USA and the Academia Sinica Institute of Astronomy and Astrophysics (ASIAA) received grant from Ministry of Science and Technology, Taiwan. The funding for ASIAA is for the development of next generation digital backend for an ultrawide-bandwidth EHT system. In this study, an analog-to-digital converter (ADC) printed circuit board assembly (PCBA) and a FPGA firmware were developed to increase the maximum data sampling rate by 3–3.2 times. In addition to being used in the EHT, the developed device will be ported to the Collaboration for Astronomy Signal Processing and Electronics Research (CASPER) environment which has worldwide academic users.

1.1. Benefits of Faster Sampling Rates and Large Input Signal Bandwidths

Interferometers that can capture and correlate large frequency bandwidths provide increased continuum sensitivity and enable the inclusion of more spectral lines within the observing band.

We have previously discussed the benefits of digitizing large signal bandwidths (Jiang et al. 2014, 2016). The benefits for the intermediate frequency (IF) system in terms of cost and complexity are approximately 2.4 times greater better than those obtained from the ADC and its sampling rate. The 5 giga samples per second (Gsps) ADC is operable only in the first Nyquist zone because of input signal bandwidth limitations. The input signal bandwidth of the 16 Gsps ADC is up to 16 GHz, which enables second Nyquist sampling. In terms of 5 Gsps configuration, the IF system can be simplified.

For example, an 8 GHz bandwidth digital backend: four set of 5 Gsps ADC boards, four bandpass filters, four mixers, four local oscillators and four low-pass filter (LPF) are used for frequency separation and down conversion if 5 Gsps ADC used. Using the presented 16 Gsps ADC PCBA, it needs only one ADC board, and the IF system can be simplified to include one mixer and one LPF.

In the next section, we describe, in detail, the design concept and hardware for this study. The commercial availability of high-speed, wideband ADCs is limited. Cost is another crucial factor. We compared the difference in the presented ADC chip and the JESD204 module in Section 3. A novel channel bonding method was developed to reduce costs. This is detailed in Section 4. The technical characterizations of the new PCBA are described in Section 5, which is followed by a summary of our study.

2. Device Selection and Hardware Design

After designing the 5 Gsps ADC PCBA (Jiang et al. 2014), we designed a 10 Gsps, 4 bit ADC board (Jiang et al. 2016) that was connected to an FPGA with a Zdok connector, which was used by CASPER (Hickish et al. 2016). The ADC chip (ASNT7120, Adsantec, California) used in the 10 Gsps ADC board had a low-voltage differential signaling output with parallel transmission. The Zdok connector limited the adoption by other users.

As technology innovated, FMC interface is getting popular in the market. Many FPGA platform equipped with FMC interface that motivates us to move toward that direction. We surveyed the available components on the market during 2016–2017. Fujitsu had a 56 Gsps chip (AMC590) and Micram had a 30 Gsps chip. However, these chips were not affordable because no discount to academics was offered on these chips. Weintroub et al. (2015) attempted a 20 Gsps ADC made by Hittite. Shortly they stopped the project because of the preliminary result was not as expected.

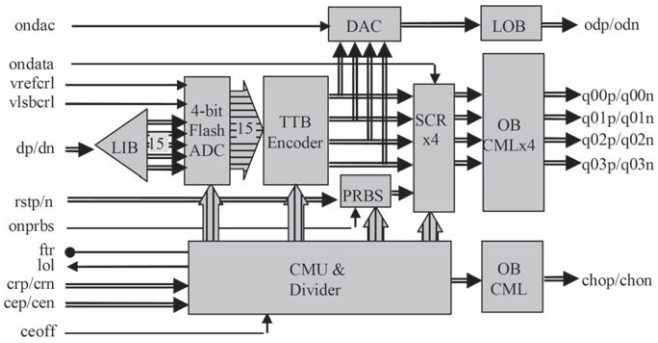

Figure 1. Block diagram of the ADC chip, ASNT7123 (www.adsantec.com).

After comparing the feasibility and unit price of various chips, we selected Adsantec Corporation's 15 Gsps, 4 bit flash ADC chip in 2018 (Jiang et al. 2019). The quoted prices of these ADC chips were approximately 10 times the material cost of this 15 Gsps ADC PCBA. To accommodate the new chip, we developed a novel ADC board by using a widely used interface for FPGAs: a FPGA mezzanine card (FMC) connector. The FMC connector contains high-speed transceivers that enable the use of a high-speed serial output ADCs. We presented preliminary results in the literature (Jiang et al. 2019). As advanced version of the ADC chip was available, we moved our development to the new chip, the 16 Gsps ADC, ASNT[3] 7123. The sampling rate of the chip is up to 16 Gsps.

The ASNT7123 chip is advanced version of ASNT7122. Both of them are 4 bit flash ADCs and wide analog front-end bandwidth. ASNT7122 can run up to 15 Gsps only and the ASNT7123 can run up to 16 Gsps. The block diagram of ADC system displayed in Figure 1. A linear input buffer in front of the chip receives the analog signal. The input buffer has a current mode logic (CML)-type input interface. The chip has thermometer-to-binary encoder to convert 15 copies of the input analog data signal to the 4 bit binary word.

The chip contains a 2^{15}–1 pseudorandom binary sequence (PRBS) generator and mixer to scramble the 4 bit data (Bardell et al. 1987). The scrambled data are sent to high speed serial output via CML interface. The chip provides control of input data on and off so that output data can have PRBS code only. Users can use the PRBS code to align the 4 lanes in FPGA firmware. We discussed the detail in our previous 15 Gsps ADC work (Jiang et al. 2019).

The material of the present study is depicted in Figure 2. Three SubMiniature Version A (SMA) connectors are mounted on the left side of the board and two are on the bottom of the board. The three connectors on the left are for the synchronization input, external clock input and internal phase lock loop reference clock. Two differential signal inputs for digitization are at the bottom.

[3] www.adsantec.com

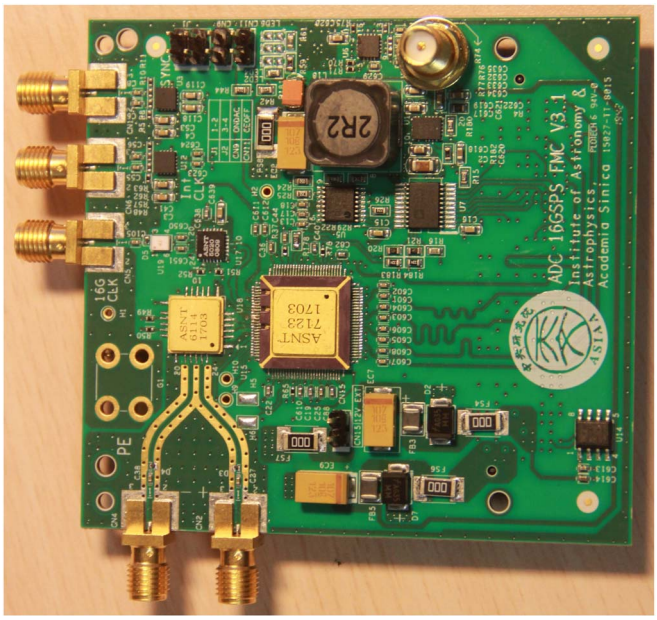

Figure 2. Four-bit, 16 Gsps ADC PCBA. The SMA connectors in the left-hand side from the top are for synchronization signal (CN1), internal clock (CN6) and 16 GHz external clock (CN5). On the bottom is a pair of differential signal input: −(CN4) and +(CN2). The jumpers from the left are for reference clock dividers (J1), enabling the digital to analog converter (ondac CN9), internal or external input clock selection (ceoff CN11). The FMC connector is on the back.

(A color version of this figure is available in the online journal.)

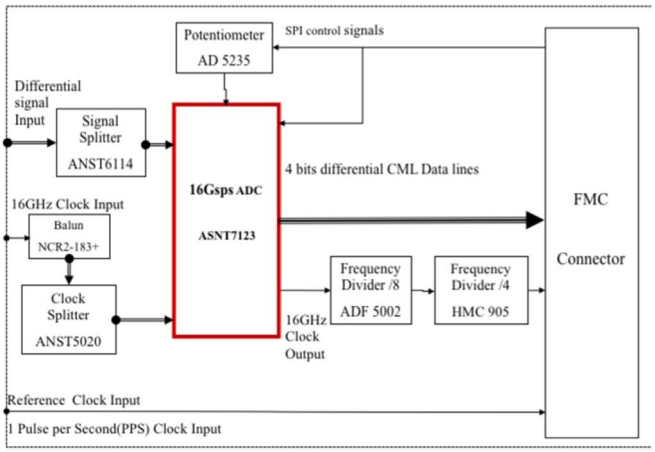

Figure 3. Block diagram of the 16 Gsps ADC PCBA. A wide-band balun, termed Mini-Circuits NCR2-183+, converts the single-ended clock into differential clock signals. ASNT 5020, a 1:2 clock buffer, distributes the clock signal to the ADC chip. The ASNT6114 clock splitter buffers the differential analog signal input. It also distributes the analog signal into two signals. Two frequency dividers, ADF 5002 and HMC 905, divide the 16 GHz clock from the chip at a frequency of 500 MHz, which serves as the reference clock of giga-transceivers in the FPGA.

(A color version of this figure is available in the online journal.)

The board (79 cm × 73 cm) is a four-layer PCB with Rogers 3003 substrates as the outer layer, which operates at a wider radio frequency range. Conventional FR-4 substrates were placed between the outer layers. The board comprised eight trace layers. Its maximum power consumption is approximately 16 W, with the linear regulator being the major contributor. The regulator converts 12V DC down to 3.5V DC. 12V is the only voltage higher than 3.5V in FMC connector. We have tried a couple of switching regulator to save the power. Unfortunately, we removed them because of problems with ADC failure.

We continued using a manual tuning program developed in our previous 15 Gsps ADC project to tune the two parameters (gain and offset) through a serial peripheral interface bus. Data quality was optimized once the optimal gain and offset parameters are obtained, the parameters can be stored in an 1024-position digital potentiometer-analog device AD5235 nonvolatile memory. A block diagram of the PCBA is presented in Figure 3.

For protection and single-ended-to-differential transformation purposes, an analog-signal splitter, ANST6114, is placed in front of the ADC chip. A differential clock is required for high-speed operation such that a balun is formed, which consists of Mini-Circuit NCR2-183+ and a clock buffer (ANST5020, Adsantec).

Two symmetric coplaner waveguide traces were employed for the signal input. We duplicated this analog input trace design from our 10 Gsps ADC board (Jiang et al. 2016). To mitigate electromagnetic interference grounded via holes were placed along both sides of the traces.

3. Between Parallel and Serial Output

Most ADC output was in parallel in the old days. As the semiconductor technology evolved, the ADC is getting faster and faster and that perhaps motivates for the change from parallel input/output interface to high speed serializer/de-serializer (SERDES) interface. Nowadays, high speed ADC is at the order of giga sample per second. It challenges the layout to align many parallel data lanes and one clock signal. Similar with communication and removable disk media, SERDES ADC embeds clock signal and other necessary information in the data stream. Recover the clock signal and other useful information from the data stream eases the layout difficulty. Current SERDES ADCs almost complies with the JESD204 standard (JEDEC Standard JESD204B 2011). To simplify the chip design, ANST 7123 does not not totally follow that standard. A synchronized clock signal is provided by the chip to save the embedding clock signal circuit. The clock signal in JESD204 is embedded in 8/10 bit encoding mechanism. For DC balance, the chip used the PRBS to scramble the data, it

meets the JESD204 standard. Since ANST7123 only has 4 bits output, it employs 4 SERDES lanes with 1 bit word boundary, consequently no need for word alignment. The special characters for word alignment in JESD204 are termed commas. Since each SERDES data lane is independent of the other data lanes, alignment among those data lanes is critical for SERDES ADC, consequently a mechanism called channel bonding is devised in JESD204 and there are special characters embedded in the data stream for channel bonding purpose.

The ADC chip used in this study does not have 8/10 bit encoding in the data stream where the clock signal can be recovered. Thus, we divided the high-frequency clock output, 16 GHz, from the chip by 32. Consequently, a 500 MHz in-phase reference clock was used as the input FPGA. ADF5002 divides by 8, and HMC 905 divides by 4. Both are made by Analog Devices. The range of reference clock to the FPGA is limited under 900 MHz.

4. Channel Bonding

The main challenge of using ANST7123 family ADC was to align the 4 data lanes which might not arrive the FPGA at exact the same time. The misalignment is mainly because of the unequal length layout on the ADC and VCU118 boards or due to different delay time in the FPGA I/O. In this study, one inch, 25.4 millimeters (mm), trace layout difference will cause 145 pico-second (ps) signal difference. Running at 16 GHz, the clock period is 62.5 ps. If the signal can have 10%–20% delay tolerance, then it allows only about 1–2 mm trace layout difference. It will be even more challenging if includes the delay difference in each individual connector pin. ANST7123 does not embed the channel bonding characters in the serial data stream, thus an alignment mechanism is necessary to match the 4 data lanes. We devised a novel channel bonding method in our previous 15 Gsps ADC project (Jiang et al. 2019), we continued adopting that method.

The novel method we developed is that turn off the data input by de-asserting the ON_DATA signal, enable the PRBS code by asserting the ON_PRBS signal at the beginning. At that condition, the chip sends out PRBS code only to the FPGA. Checking_Raw, the Verilog program was developed, starts searching the leading PRBS code in first data lane. The leading PRBS code is 0x30004000. Once it is found it, the program memorizes the position in the buffer, then search the next 3 data lanes. The detail finite state machine is depicted in Figure 4.

The success of our channel bonding method is that Xilinx has a bit-slip function in the Y-series gigabit transceiver (GTY) of their FPGA chips. It allows users to shift individual serial data stream in the buffer at the unit of bit. With that function, the 4 data lanes of this study can be aligned. The parameter of bit-slip is called RXSLIDE. We converted the buffer from 128 bits to 4 bits by two first-in first-out buffer.

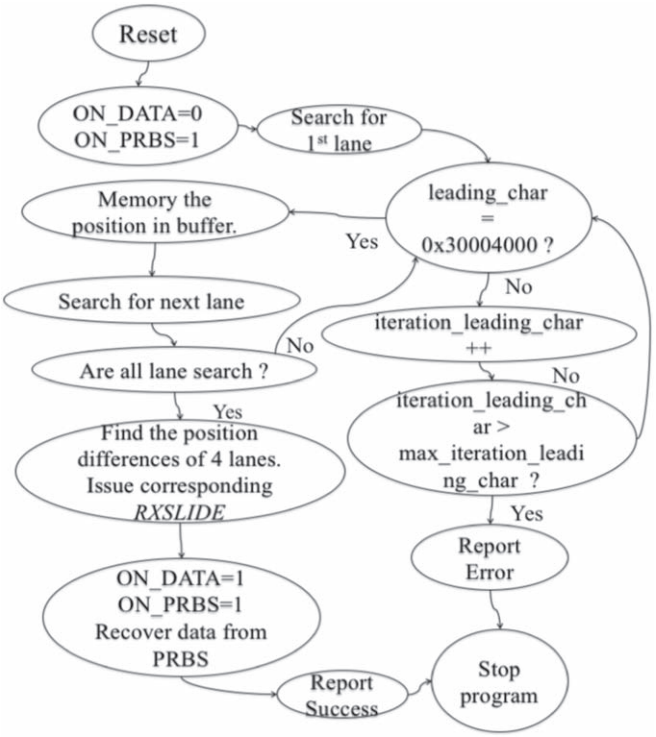

Figure 4. State machine of channel bonding. First of all, makes the ADC chip sends out PRBS code only by setting two control pins: ON_DATA = 0 and ON_PRBS = 1. Then the firmware starts searching for the leading PRBS code, 0x30004000 in the first data lane. Once found, the firmware memorizes the position in memory.

An interactive logic analyzer (ILA) outputs the 4 bit data stream to the computer for further characterization. The ILA is a component of Vivado.[4] Vivado is the development platform for Xilinx FPGA. Figure 5 is the block diagram of the data receiving firmware in FPGA.

5. Calibration and Performance

We used Xilinx VCU118 development board[5] as the testing platform which has a powerful XCVU09P FPGA. There are 120 multiple serial GTY available on the FPGA, and eight GTY pairs are attached to the FMC connector on the VCU118. The GTY can operate at up to 32.75 gigabits per second (Gb s^{-1}), that is enough to accommodate a 16 Gsps ADC output.

The test setup used for calibration and characterization is illustrated in Figure 6. The input to the ADC under test was stimulated as a variable frequency continuous wave (CW) tone at optimal input power. At this power level, the time domain sine wave occupied half the full range of this ADC device ($V_{pp} = 0.2377$ V).

[4] www.xilinx.com/products/design-tools/vivado.html
[5] www.xilinx.com/products/boards-and-kits/vcu118.html

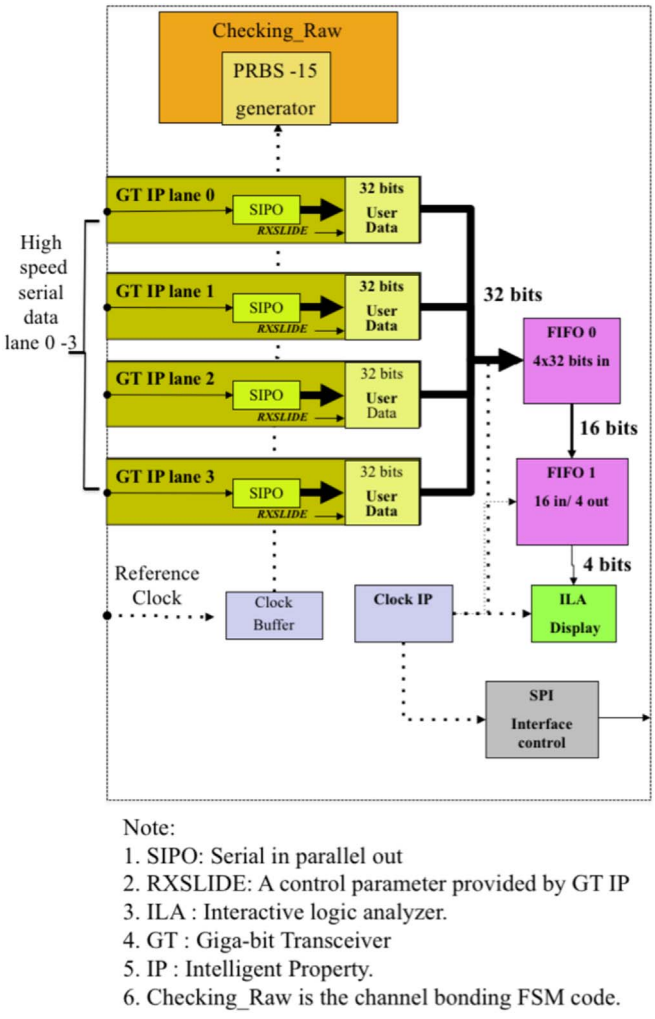

Figure 5. Data receiving interface inside the FPGA (www.adsantec.com).
(A color version of this figure is available in the online journal.)

We characterized the spurious-free dynamic range (SFDR) and effective number of bits (ENOB) for three boards. The frequency range covered the first and second Nyquist zones (i.e., 0–16 GHz).

Furthermore, we performed fast Fourier transform (FFT) on 4096 spectral channels for 8192 samples. We calculated and carefully tuned the CW signals such that they were concentrated on the center of the spectral bin, which helped us avoid leakage to the adjacent bins. We selected 16 discrete CWs per Nyquist zone, spaced at an interval of approximately 250 channels, for the characterization.

The SFDR is expressed in Equation (1) (IEEE 2017) (Section 8.8, IEEE 1057–2017):

$$\mathrm{SFDR(dB)} = 20\log_{10}\left(\frac{A_{\mathrm{inpit}}}{\max(f_h, f_s)}\right). \quad (1)$$

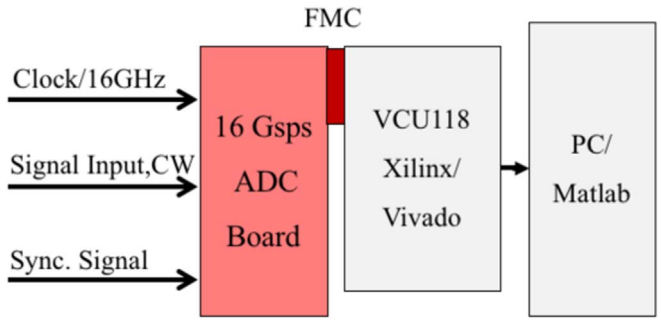

Figure 6. Calibration and test setup for the ADC. A CW source from an Agilent signal synthesizer, E8257D, was used to stimulate the ADC under test. VCU118 and a Linux PC are used to capture and process the digitized data from the ADC. The external 16 GHz clock was provided by the other Agilent signal synthesizer.
(A color version of this figure is available in the online journal.)

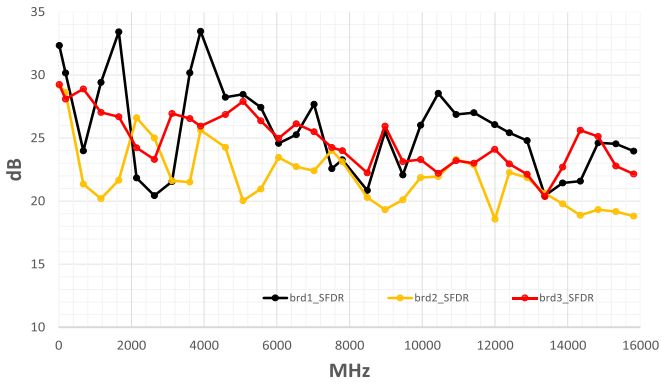

Figure 7. SFDR of 3 boards characterized from the first to the second Nyquist zone.
(A color version of this figure is available in the online journal.)

Where A_{input} is the amplitude of the input tone and the nominator is the maximum of either the harmonic or spurious signals appearing in the acquired spectrum.

The SFDR for the ADC board was characterized by inputting a single frequency tone into the ADC and measuring the ratio of the desired tone to the maximum undesired spur at the FFT output (IEEE 2017). The results are plotted in Figure 7. The SFDR measurement on Adsantec's datasheet at an input signal of 3.9/7.8 GHz is 30.13/28.78 dB. Our measured results at the same frequency is 28.3/23.5 dB on average.

To obtain the ENOB, the noise and distortion (NAD) must be determined in advance, for which we fitted a sine wave to record the signal at a chosen frequency. Next, we estimated the rms value of noise and distortion, as shown in Equation (2).

$$\mathrm{NAD} = \sqrt{\frac{1}{M}\sum_{n=1}^{M}(x(n) - x(n))^2} \quad (2)$$

where $x(n)$ is the sample data set
$x'(n)$ is the data set of the best-fit sine wave
M is the number of samples in the record.

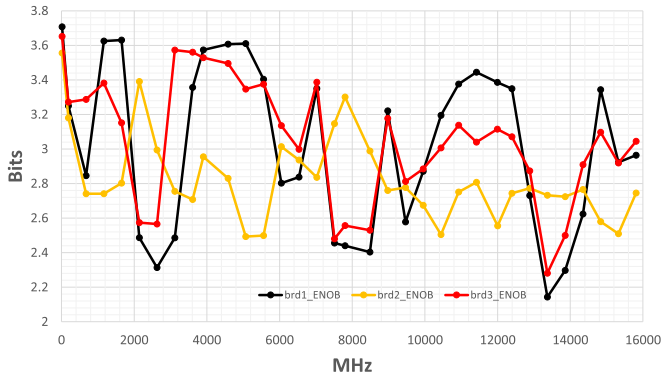

Figure 8. ENOB of 3 boards characterized from the first to the second Nyquist zone.
(A color version of this figure is available in the online journal.)

ENOB is defined by IEEE (IEEE 2017) (Section 8.5 of IEEE 1057–2017) as follows: for an input sine wave of specified frequency and amplitude, after correction for gain and offset, the ENOB is the number of bits of an ideal ADC for which the rms and distortion of the ADC are being tested. ENOB is expressed as follows:

$$\mathrm{ENOB} = \log_2\left(\frac{\mathrm{FSR}/G}{\mathrm{NAD}\sqrt{12}}\right) \approx N - \log_2\left(\frac{\mathrm{NAD}}{\epsilon_Q}\right) \qquad (3)$$

where

N is the specified number of bits in the ADC,
FSR is the specified full-scale range of the ADC,
G is the measured gain (nominally = 1),
NAD is the rms noise and distortion,
and ε is the rms ideal quantization error.

The ENOB measurement data on the Adsantec's datasheet at input signals of 3.9/12 GHz is 3.39/3.26 bits. Our results at the same frequencies is, on average, 3.36/3.02 bits, as depicted in Figure 8.

5.1. Optimal Input Noise Power

This ADC board can be used for astronomical applications where the input signal consists largely of Gaussian noise. The optimum input signal drive level relative to the $V_{\text{full-scale}}$ of the ADC device must be determined. Under-driving the ADC results in low ENOB, whereas overdriving leads to clipping and generation of undesired harmonics.

The IEEE method for determining optimal input drive is obtained by performing a noise-power ratio (NPR) test. This test involves using a broadband noise source with a notch filter to remove a portion of the noise prior to inputting it to the ADC under test. Our test setup for NPR is illustrated in Figure 9. First, a 16 GHz wideband noise source, NW10M16G-M by Noise Wave, was used to inject the noise signal into a 6 GHz LPF and then into a tunable notch filter, 3TNF-1500/3000-N/N,

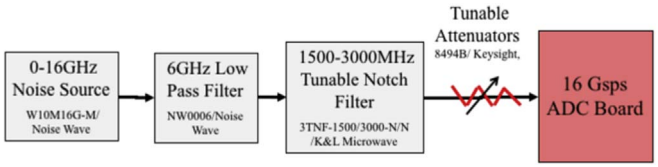

Figure 9. NPR test setup.
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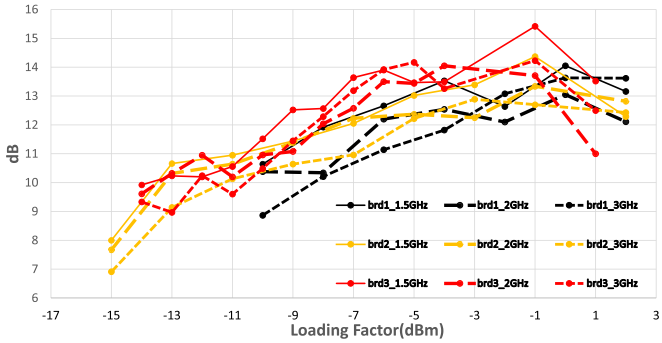

Figure 10. NPR test setup.
(A color version of this figure is available in the online journal.)

by using a K&L Microwave. The tuning range was 1.5–3.0 GHz. An adjustable attenuator, 8494B by Keysight, was used to attenuate the input power to determine the optimal value of the NPR. FFT was performed on the digitized ADC output and the NPR (Equation (4)). The ratio of desired noise to undesired residual noise in the notched portion of the spectrum was characterized at different input power levels.

$$\mathrm{NPR(dB)} = 10\log_{10}\left(\frac{P_{\mathrm{No}i}}{P_{N_i}}\right) \qquad (4)$$

where P_{No} and P_{Ni}, respectively, are the outside and inside notch power spectral densities (IEEE 2017) (Section 7.9 of IEEE 1057–2017).

The optimum drive occurred when the NPR was at its maximum. For an ideal 4 bit ADC, the maximum NPR is 19.4 dB and occurs at a loading factor of −8.6 dB, which is equivalent to an input drive of −9.1 dBm at the input point of the ADC chip. The loading factor is the ratio of the signal input level to the full-scale input range in decibels. The maximum NPR of three boards at 1.5, 2.0, and 3.0 GHz is, on average, 15 dB (see Figure 10). Because we placed an analog-signal splitter, ANST6114, in front of the ADC chip, power loss occurred. The loss offset the optimal input power to some extent. The optimal power occurred approximately at a loading factor of 0 dBm for No. 1 board, −1 dBm for No. 2 and No.3 board, The loading factor of this board to the real input power (dBm) is +0.5 dB. We conducted the

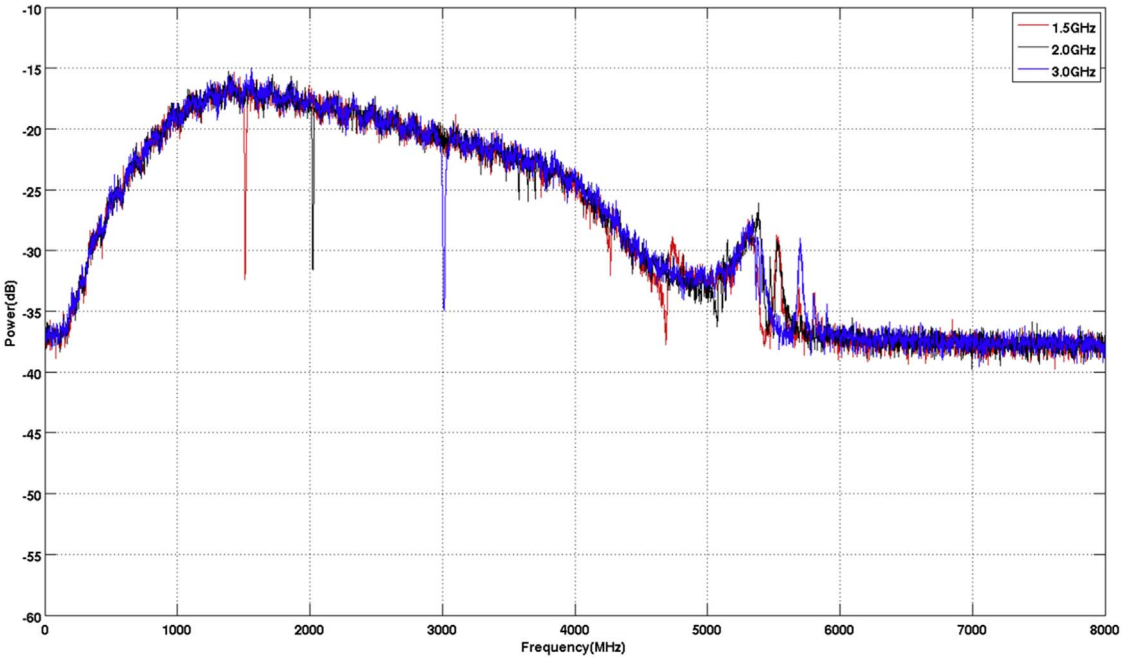

Figure 11. Overlapped spectra of No. 2 board with a notch filter at 1.5 GHz (red curve), 2.0 GHz (black curve), and 3.0 GHz (blue curve). One hundred spectra were averaged for each of the notch traces.
(A color version of this figure is available in the online journal.)

characterization of the ANST6114 evaluation board independently and confirmed power loss related to the chip. It is not an ideal gain buffer, as stated on its data sheet. Figure 11 depicts the spectra of board No. 2 the NPR tests at three frequencies. The roll-off at frequencies lower than 1 GHz and higher than 3 GHz is due to the notch filter response and spikes in the 5–6 GHz range.

6. Conclusion

In this study, we developed an ADC board that permits digitization of up to 16 Gsps with 4 bit quantization. Previously, we developed 5 and 10 Gsps ADCs for the CASPER community. The current study was focused on applications for enhancing EHT application and porting to the CASPER environment. Except EHT, those working with wide bandwidth radio telescopes such as the Greenland Telescope (Inoue et al. 2014), AMiBA (Ho et al. 2009), and Submillimeter Array can benefit by using the presented device. Their receivers output bandwidths at frequencies of 16, 16, and 18 GHz, respectively. The developed device can capture larger portions of the IF spectrum, which reduces the complexity and cost of using the IF distribution system.

The SFDR and ENOB of the ADC board were characterized over its operating bandwidth. The ADC board is functional for the first and second Nyquist samplings. For the first and second Nyquist zones (i.e., 0–16 GHz), the minimum to maximum range of SFDR and ENOB are 18–33 dB and 2.1–3.7 bits, respectively. Finally, for Gaussian noise-dominated applications, we recommend the optimal input power of −1 dBm at the entry of the board.

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References

Bardell, P. H., McAnney, W. H., & Savir, J. 1987, Built-In Test for VLSI: Pseudorandom Techniques (New York: Wiley)
Hickish, J., Abdurashidova, Z., Ali, Z., et al. 2016, JAI, 2016, 1641001
Ho, P. T. P., Altamirano, P., Chang, C. H., Chang, S. H., et al. 2009, ApJ, 694, 1
IEEE 2017, IEEE Standard for Digitizing Waveform Recorders, 1057–2017, Revision of IEEE 1057–2007
Inoue, M., Algaba-Marcos, J. C., Asada, K., et al. 2014, RaSc, 49, 564
JEDEC Standard JESD204B 2011, JEDEC Solid State Technology Association, www.jedec.org
Jiang, H., Guzzino, K., Kubo, D., Yu, C.-Y., & Chen, M.-T. 2016, PASP, 19, 128
Jiang, H., Li, C. T., Guzzino, K., et al. 2014, PASP, 126, 761
Jiang, H., Yu, C.-Y., Chen, M., & Liu, M. 2019, in The 28th Int. Symp. on Industrial Electronics (IEEE-ISIE 2019) (Piscataway, NJ: IEEE), 1345
The EHT Collaboration et al. 2019a, ApJL, 875, 1
The EHT Collaboration et al. 2019b, ApJL, 875, 2
Weintroub, J., et al. 2015, in 26th Int. Symp. on Space Terahertz Technology, 20 Gigasample per Second Analog-to-digital Conversion for Ultra-wideband Radio Astronomy, 41