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Structure of elastically strain-sharing silicon(110) nanomembranes

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Abstract. Nanomembranes composed of single-crystal, tensilely strained Si(110) and compressively strained SiGe(110) layers have been fabricated from silicon-on-insulator (SOI) substrates. Elastic strain sharing is demonstrated for a trilayer structure consisting of a 12 nm Si/80 nm $Si_{0.91}Ge_{0.09}$ film epitaxially grown on a 12 nm thick (110) oriented Si template layer that is subsequently released from its handle substrate. X-ray diffraction on the as-grown and released structures confirms a virtually dislocation-free membrane with a tensile strain of $0.23 \pm 0.02\%$ in the Si(110) layers after release. Lower growth temperatures in molecular beam epitaxy allow for smoother growth fronts than are possible using chemical vapour deposition.

Contents

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1. Introduction

It is well established that strain modifies the band structure of Si, thereby influencing the charge carrier mobility [1], among other effects. Tensile strain in Si(001) produces significant electron mobility enhancement, but degrades the hole mobility at low levels of strain [2]. Advanced CMOS (complementary metal-oxide-semiconductor) applications demand both high electron and high hole mobility. To achieve that goal with Si(001) would require the use of very highly strained Si(001), a difficult condition to achieve.

For high-mobility p-type devices, Si(110) is an attractive alternative, as its hole mobility is about twice that of Si(001), although it is still much lower than the Si(001) electron mobility [3]. However, when a (110) oriented Si lattice is under biaxial tensile strain, the hole mobility is dramatically enhanced even for relatively small values of strain, and the electron mobility can be improved to a value in excess of 80% of the electron mobility found in unstrained Si(001) [4]. Consequently, strained Si(110) is a good candidate for both high-speed pMOS (positive-channel metal-oxide-semiconductor), and for advanced CMOS applications, where reducing the current drive imbalance between n-type and p-type channels is a major concern. There is also considerable interest in using non-traditional crystal orientations to optimize carrier mobility, by fabricating mixed regions of Si(110) and Si(001) on a single wafer: so called hybrid-orientation technology (HOT). HOT architecture allows fabrication of p-channel devices on the high-hole-mobility Si(110) regions, and n-channel devices on the high-electron-mobility Si(001) regions [5]. The introduction of strain to HOT Si offers an even larger parameter space for tuning the mobility of both electrons and holes.

In order to strain Si tensilely over large areas (in particular the Si(001) orientation), traditionally one grows a Si layer epitaxially on a buffer composed of strain graded SiGe layers, where each layer in the buffer is grown beyond its kinetic critical thickness for relaxation by dislocation formation [6]. The use of thick buffer layers and low strain grading rates reduces the dislocation density by encouraging the propagation rather than the nucleation of dislocations [7]; however, each dislocation still has two threading arms that propagate through all layers and can degrade the carrier mobility [8]. The growth of SiGe(110) buffer layers is more problematic: for a given Ge concentration, the critical thickness for relaxation via dislocation generation is less than in the (001) orientation [9]. Strain grading results in a threading dislocation density that is more than 10 times higher than in Si(001) [10]. Consequently, techniques that produce tensile strain without the use of strain graded buffer layers and their associated dislocations are particularly desirable for the Si(110) orientation.

We have recently developed a method for tensilely straining Si that involves elastic strain sharing between the layers of a free-standing sandwich of heteroepitaxially grown Si/SiGe/Si nanomembranes [11, 12]. This method is based on the concept of compliancy, whereby a strained heterostructure system can elastically relax by moving freely on its substrate [13, 14]. This concept has not been very successful because solid substrates are not sufficiently compliant. In our nanomembrane approach, a compressively strained SiGe layer is grown (below its kinetic critical thickness for dislocation-driven relaxation) on the silicon template layer of a silicon-on-insulator (SOI) substrate, followed by a top Si capping layer. Selective chemical removal of the buried oxide (BOX) (insulator) layer releases the tri-layer system, creating a temporarily free membrane, and thus allowing compressive strain in the SiGe layer to be transferred to tensile strain in the Si layers as the system relaxes by laterally expanding [11]. In other words, the ‘compliant layer’ in this case is ‘nothing’: it can also be vapour or

Table 1. Dependence of SiGe and Si growth rates (CVD) on temperature for membranes with a 9 and a 20% Ge composition alloy layer.

Membrane	Material	Growth temperature (°C)	Growth rate (nm min^{-1})
1	$Si_{0.91}Ge_{0.09}$	660	1.2
	Si	720	1.7
2	$Si_{0.80}Ge_{0.20}$	720	1.3
	Si	720	2.1

fluid. An added significant benefit of our approach is that this elastically relaxed, very thin and dislocation-free multiple-layer membrane bonds readily to other hosts.

Eliminating the series of grown buffer layers containing dislocations makes our method particularly appealing for straining Si(110), because of the problems described above. We report here on elastically strain sharing Si(110) nanomembranes, and show high-quality, single-crystal, tensilely strained Si(110) sheets. Furthermore we also demonstrate the transfer of these membranes to foreign surfaces, opening the possibility for a large range of novel materials integration paradigms.

2. Experimental

Membrane fabrication begins with a SOI(110) substrate (Soitec) composed of a 190 nm thick Si(110) template layer, separated from a bulk Si(001) handle substrate by a 150 nm thick BOX layer. The template layer is thinned to 12 nm via thermal oxidation at 1050 °C and stripping of the thermal oxide in dilute hydrofluoric (HF) acid. This template layer becomes the bottom layer of what will become a Si/SiGe/Si(110) heterostructure with thickness and composition 12 nm Si/80 nm $Si_{0.91}Ge_{0.09}$/10 nm Si. We also fabricated a membrane stack with 20% Ge content in the alloy layer for structural comparison to the 9% alloy layer membranes (the alloy layer and Si capping layer were grown to a thickness of 80 and 38 nm, respectively).

The SiGe and top Si layers are epitaxially grown by either chemical vapour deposition (CVD) in a cold-wall ultra-high-vacuum (UHV) CVD reactor using silane and germane precursors, or by solid-source molecular-beam epitaxy (MBE). For CVD growth, the temperature dependence of the growth rate and the Ge fraction in the alloy layer are given in table 1 for membranes with a Ge content of 9 and 20%. For the membranes with a 9% Ge composition alloy, the alloy layer is grown at 660 °C, while for the 20% Ge composition sample the alloy growth temperature is 720 °C. The deposition temperature for the top Si layer is 720 °C in both cases. Precursor gas flow rates for the Si/$Si_{0.91}Ge_{0.09}$/Si membranes were set at 52 and 8 standard cubic centimeters per minute (SCCM) for SiH_4 (10% with balance H_2) and GeH_4(20% with balance H_2) respectively, yielding a total pressure of ∼26 m Torr. For the 20% Ge alloy, the GeH_4 flow rate is 14 SCCM. For a given temperature, the growth rate on Si(110) is much less than on Si(001), as will be discussed in section 3.3. Growth is monitored *in situ* using reflection high-energy electron diffraction (RHEED) to ensure a planar (rather than islanded [15, 16]) growth front. For MBE, we use a growth rate of 2.5 nm min^{-1} at 550 °C.

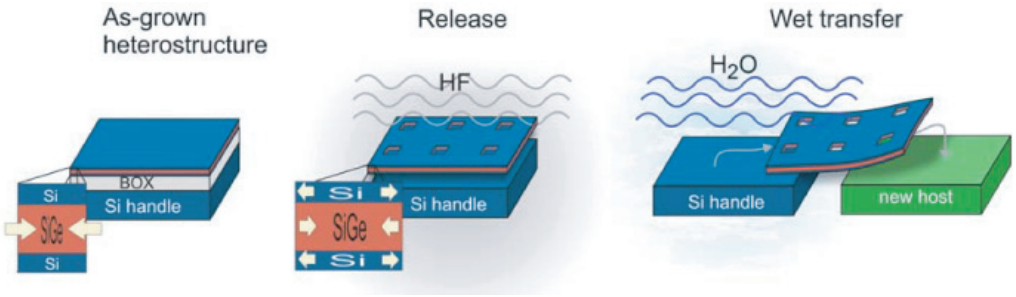

Figure 1. Schematic diagram of the release and transfer processes. The as-grown heterostructure is released from its handle substrate by chemical removal of the BOX. Strain sharing between the layers generates tensile strain in the Si layers. The membrane can then settle in place on its original substrate, or it can be transferred to a new host substrate via several methods, including floating off in water, shown here.

The as-grown (unreleased) heterostructure is composed of a compressively strained alloy layer and two Si layers that maintain their bulk lattice constant because the BOX/template interface pins the template layer at its original, relaxed, lattice constant during growth [10]. We characterize the as-grown membrane structure before release with high-resolution x-ray diffraction (XRD) to confirm the thickness and composition of the layers and to provide a reference for the strain state prior to release, and with intermittent-contact-mode atomic force microscopy (AFM) to investigate the growth front morphology.

We then release these tri-layer membranes (typical size $3 \times 3\,\mathrm{mm}^2$) by selective removal of the BOX layer [11], as depicted schematically in figure 1. To enhance etchant access to the BOX, we pattern and etch an array of access holes through the membrane via photolithography and reactive ion etching (RIE), to expose the BOX. Submersion in 49% HF for 60 min selectively removes the BOX, releases the membrane, and allows elastic strain sharing between the layers. The alloy layer now partially transfers some of its compressive strain to tensile strain in the Si layers as the system elastically relaxes (i.e., without forming dislocations). The magnitude of strain transfer depends on both the Ge content in the alloy layer and the thickness ratio of the layers [11], with the final strain in the Si layers given by

$$\varepsilon_{\mathrm{Si}} = -\varepsilon_{\mathrm{m}} \frac{t_{\mathrm{SiGe}} M_{\mathrm{SiGe}}}{t_{\mathrm{Si}} M_{\mathrm{Si}} + t_{\mathrm{SiGe}} M_{\mathrm{SiGe}}}, \tag{1}$$

where ε_{m} is the mismatch strain, and ε, M, and t are the layer strain, biaxial moduli, and thicknesses of the Si and SiGe layers [17]. The use of ultra-thin Si layers, relative to the thickness of the alloy layer, obviously maximizes the tensile strain in the two Si layers.

The membranes initially settle on the handle substrate, after which we again characterize with XRD and AFM. We also transfer some membranes to a new host by agitating the released membrane (which is only weakly bound to the original handle wafer on which it has settled) in deionized water. A floating membrane can be collected by bringing it into contact with the new host, which can be a variety of materials. For example, if the new host is a chemically cleaned Si substrate, the membrane can be bonded to this substrate on a hotplate at 100 °C for 10 min and then 500 °C for 10 min. This bond is extremely good. The (110) membrane release, transfer, and

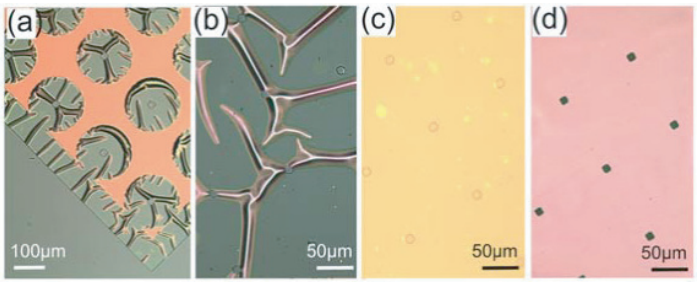

Figure 2. Optical-microscope images of Si(110)/$Si_{0.91}Ge_{0.09}$(110)/Si(110) nanomembranes. The arrays of holes in the membrane that are used to aid etchant access are visible in the images. (a) Snapshot of the release process. (b) Membrane released in place. (c) Wet transfer to new Si host. The ripples visible in (b) smooth out when the weak bonding to the handle substrate is eliminated. (d) Alternative dry transfer to paper.

bonding to a new host are quite similar to those for Si(001). As in Si(001), the strain condition is maintained during bonding [18, 19].

3. Properties of (110) oriented nanomembranes

3.1. Membrane release and transfer

The release and transfer sequence has been described above and shown schematically in figure 1. Optical-microscope images of (110) membranes with composition 12 nm Si/80 nm $Si_{0.91}Ge_{0.09}$/10 nm Si are shown in figure 2. Figure 2(a) shows a snapshot of an interim stage in the release, with the membrane taken prematurely out of HF, allowing observation of the etch front around the release holes and the edges of the membrane. The released parts are rippled because of their lateral expansion during strain sharing. Figure 2(b) shows a completely released membrane after it has settled in place on its original growth substrate (release-in-place). The rippled morphology is again obvious, and demonstrates the membranes' flexibility. The image in figure 2(c) was taken from a membrane after transfer to a new Si host; both the membrane and the new host were chemically cleaned and H terminated before transfer. The obvious absence of rippling in the transferred membrane is a consequence of the transfer process: the membrane is smoothed during the float-off and transfer in fluid. To demonstrate the versatility of transfer, we also transferred a membrane to a sheet of paper. In this case, the membrane was released in the usual manner and allowed to settle on its original handle substrate, the sample was then removed from the aqueous solution, and the membrane transferred by placing adhesive coated paper into contact with a release-in-place membrane.

As mentioned in the introduction, there is currently considerable interest in HOT, which allows fabrication of p-channel devices on the high-hole-mobility Si(110) regions, and n-channel devices on the high-electron-mobility Si(001) regions. When a membrane is transferred to a Si(001) host (e.g. figure 2(c)), the holes in the membrane provide ready access to a Si(001) substrate, while the surrounding membrane surface is strained Si(110). This architecture provides an opportunity to process the membranes further (for example, device isolation and selective epitaxy) in a manner similar to other forms of HOT fabrication [20]. The advantage

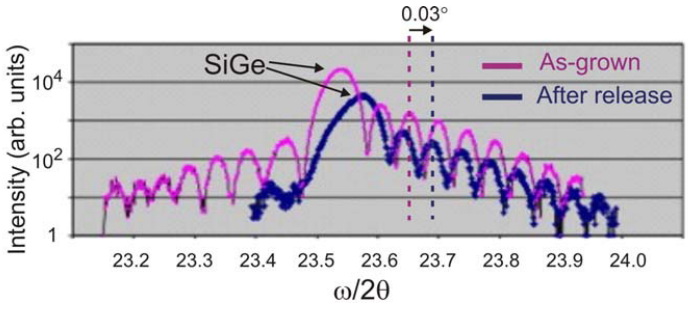

Figure 3. XRD $(\theta/2\theta)$ scans of the (220) reflection from an as-grown $Si(110)/Si_{0.91}Ge_{0.09}(110)/Si(110)$ heterostructure, and after release-in-place (see legend). The SiGe peak and the interference fringes all shift by 0.03° to higher diffraction angle after release (indicated by the dashed lines), confirming elastic strain relaxation.

here is that the use of membranes allows simple incorporation of dislocation-free *strained* Si(110) surfaces into HOT schemes, with the obvious benefit of significant carrier mobility enhancement over unstrained Si(110). The holes in the membrane that provide access to the host substrate can be made in any size and shape (within the limits of lithography). The fact that CVD growth on Si(001) is much faster than on Si(110) allows the fabrication, using conventional epitaxy techniques, of a planar surface that is effectively a quilt of (110) and (100) orientations. In addition to bonding, the membranes are capable of withstanding high-temperature device processing, as we have previously demonstrated for strained Si(001) membranes [11, 18, 19].

3.2. Elastic strain sharing

To confirm the crystal quality and to determine the strain state we performed XRD. XRD $(\theta/2\theta)$ scans were taken around the (220) reflection of a $Si/Si_{0.91}Ge_{0.09}/Si$ membrane (CVD grown) both before and after release, and the peak shifts evaluated [21]. In a $(\theta/2\theta)$ scan the peaks are associated with the out-of-plane lattice constants. Reference scans of the (004) reflection from the Si(001) handle substrate were also performed to ensure accurate calibration of the peak positions and shifts. Figure 3 shows the XRD scans. The single prominent peak visible in both of the scans originates from the alloy layer. A prominent Si peak is absent because the Si layers are so thin, however, the presence of the strong interference fringes indicates coherency at the interfaces [22]. After release, the thickness fringes are still present, and all peaks move by 0.03° to higher diffraction angle, corresponding to a uniform in-plane expansion of the lattice. The combination of the presence of interference fringes and uniform peak shifts confirms that the compressive strain relieved in the alloy layer has been transferred to tensile strain in the Si layers without inelastic relaxation, the extent of the transfer determined by the relative thicknesses of the Si and alloy layers [11].

For a (110) oriented film, the out-of-plane compressive strain, $\varepsilon_\perp$ in the Si layers after release is calculated from Bragg's law using the +0.03° peak shift. This compressive strain is converted to in-plane tensile strain, $\varepsilon_\parallel$, using the expression

$$\varepsilon_\parallel = -\left(\frac{c_{11} + 1/2C}{2c_{12} - 1/2C}\right)\varepsilon_\perp, \quad \text{with } C = 2c_{44} - c_{11} + c_{12},$$

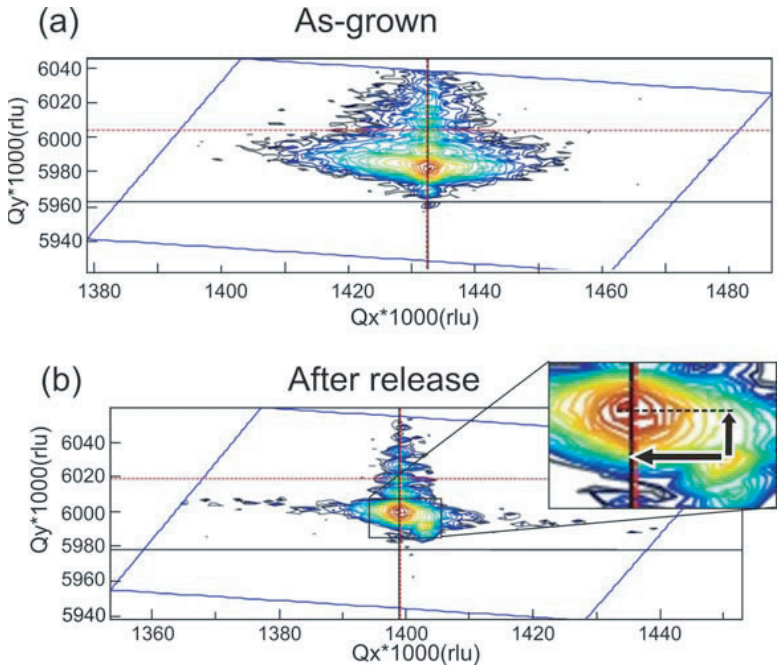

Figure 4. XRD reciprocal-space maps from the (331) reflection, where Qx is an in-plane component of the momentum transfer vector (i.e., parallel to the surface) and Qy is the out-of-plane component (i.e., normal to the surface): (a) before release (b) after release.

where c_{ij} are the elastic constants of Si [21, 23]. This equation yields the relation $\varepsilon_{\parallel} = -1.961\varepsilon_{\perp}$ and an in-plane biaxial tensile strain of $0.23 \pm 0.02\%$ in the Si layers. In contrast, in a (001) oriented film, $\varepsilon_{\parallel} = -1.299\varepsilon_{\perp}$.

To confirm elastic strain sharing in the $Si/Si_{0.91}Ge_{0.09}/Si$ membrane further, we also measured (331) (off-axis) reciprocal-space maps, which track the lattice constant changes both in-plane and out-of-plane. The map shown in figure 4(a) was taken before release, and clearly demonstrates that the intensity is conformal about a line parallel to the plane normal, i.e., the system is coherent (epitaxial relationship in all the layers). Figure 4(b), a map after the membrane was released, shows that the intensity remains conformal to a line parallel to the plane normal, indicating that the system is also coherent after release, a requirement for elastic strain sharing.

Figure 4(b) is an especially valuable map. For this particular membrane, a small section was not released from the handle substrate, leaving regions where the BOX is still intact, and hence a small portion of the membrane remains in its unrelaxed as-grown state. This as-grown region manifests itself in the scan as the smaller alloy peak located to the bottom right of the main alloy peak in figure 4(b) (highlighted in the inset), and allows comparison of the alloy peak before and after release in a single map. The inset in figure 4(b) shows that there is an increase in the in-plane lattice constant of the alloy layer (Q is in reciprocal-lattice units) and a decrease in the out-of-plane lattice constant going from the un-released to released peaks, which serves to confirm that the SiGe alloy relaxes via an in-plane expansion coupled with an out-of-plane lattice contraction, as strain is shared between the layers of the membrane.

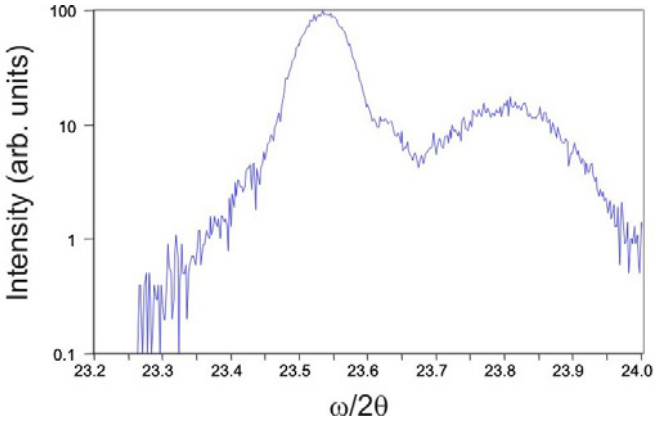

Figure 5. (220) XRD line scan from an as-grown high-Ge-content Si(110)/$Si_{0.80}Ge_{0.20}$(110)/Si(110) membrane.

An XRD scan taken from the as-grown Si(110)/$Si_{0.80}Ge_{0.20}$(110)/Si(110) membrane is shown in figure 5. Clearly this higher-Ge-concentration membrane does not display the thickness fringes that are indicative of a high-quality crystalline heterostructure with smooth interfaces. This observation suggests limits on the possibility of growing high-Ge-content (and hence highly strained) (110) membranes with CVD. This point will be elaborated on in section 3.3.

3.3. Surface roughness

Surface roughness plays an important role in charge scattering, and can seriously degrade mobility and hence device performance [24]. We measured the surface roughness of the Si/$Si_{0.91}Ge_{0.09}$/Si membranes grown with CVD with AFM, as shown in figure 6. The root mean square (RMS) roughness of an as-grown membrane, figure 6(a), is 1.7 ± 0.2 nm, determined from an average of 3 scans of size $5 \times 5 \mu m^2$. This value is significantly higher than typical values obtained for pseudomorphic growth of SiGe on Si(001) at similar growth conditions. Figure 6(b) shows an AFM image of the membrane after release, making it clear that the elastic strain relaxation has not altered the morphology. The measured RMS roughness after release is 1.8 ± 0.2 nm.

Growth front roughening during heteroepitaxy depends on both the Ge content in the alloy and the growth temperature [16]. Our CVD growth on the Si(110) surface proceeds at a much slower rate than on Si(001). As table 1 shows, typical Si(001) growth at 580 °C proceeds at 4 nm min^{-1}, while Si(110) growth proceeds at ∼2 nm min^{-1} at the much higher temperature of 720 °C. This slower growth is consistent with other reports of SiGe growth by CVD on Si(110) surfaces [10]. Most likely the lower growth rate arises from slower desorption, at the growth temperature, of the hydrogen that is the product of the decomposition of silane or germane at the surface, as is the case for a (111) oriented substrate [25]. A minimum practical (precursor decomposition limited) growth temperature of around 660 °C for CVD growth of SiGe(110) removes the possibility of smoothing the growth front via growth at a lower temperature. On the other hand, membrane growth by MBE is a viable option to obtain a smoother growth front. In MBE the minimum growth temperature is not dictated by precursor dissociation. Figure 6(c) shows an AFM image of a Si(110)/$Si_{0.91}Ge_{0.09}$(110)/Si(110) membrane grown with MBE at a temperature of 550 °C, with thicknesses identical to the CVD-grown membranes. The

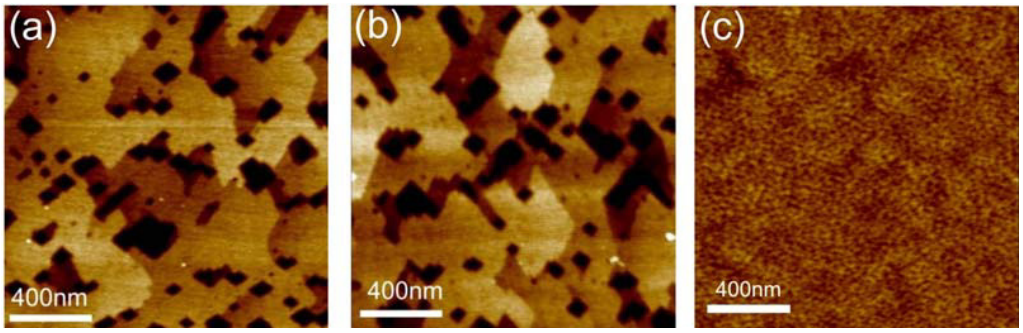

Figure 6. AFM images of Si(110)/$Si_{0.91}Ge_{0.09}$(110)/Si(110) membrane growth fronts. (a) As-grown with CVD and (b) after release (CVD). (c) As grown with MBE at 550 °C, thicknesses and composition identical to (a) and (b). All images have a color contrast (z-range) of 7 nm.

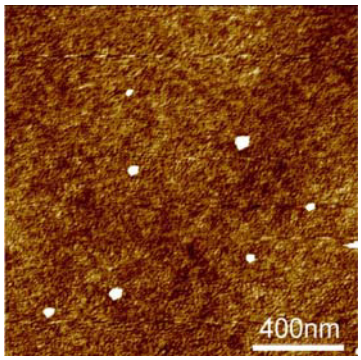

Figure 7. AFM image of CVD-grown Si(110)/$Si_{0.91}Ge_{0.09}$(110)/Si(110) after release, flip, and transfer to a new substrate. Color contrast (z-range) = 3 nm. The white spots are particulates that were not completely removed during rinsing.

RMS roughness was measured as 0.38 ± 0.03 nm and 0.42 ± 0.03 nm before and after release respectively, clearly a vast improvement over the CVD growth shown in figures 6(a) and (b), and comparable to the RMS roughness previously reported for (001) membranes grown with CVD [11].

Despite its rough growth front, the RMS outer-surface roughness of a CVD grown Si/$Si_{0.91}Ge_{0.09}$/Si membrane transferred to a new host substrate can be reduced by almost an order of magnitude by simply flipping the membrane during transfer. Figure 7 shows that this procedure works very well: flipping exposes the smooth Si(110) surface of the template layer that initially formed the BOX/template layer interface (RMS roughness = 0.20 ± 0.02 nm). Si device processing, e.g., in a HOT process, can proceed as it normally would. We have no evidence so far how this new interface, formed by a rough surface now in contact with the new substrate, will affect bonding or electronic transport. Clearly for MBE grown membranes these questions are irrelevant: we can use either side of the trilayer membrane as the outer surface and the bond is as good as for Si (001).

Development of roughness effectively prevents growth of higher-Ge-concentration membranes, because roughness increases with Ge content when membranes are grown by

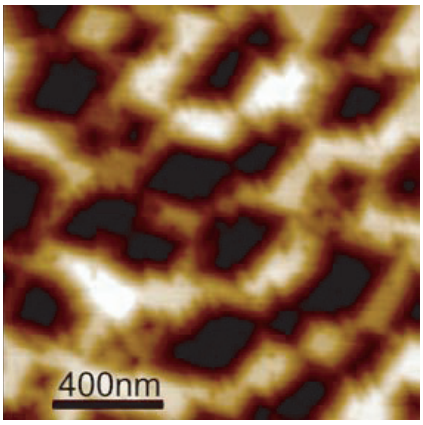

Figure 8. AFM image of the growth front of a CVD-grown Si(110)/$Si_{0.80}Ge_{0.20}$(110)/Si(110) membrane. Color contrast (z-range) = 30 nm.

CVD at accessible temperatures. Figure 8 shows an AFM scan of the higher-Ge-content (20%), as-grown (110) heterostructure, demonstrating extreme roughening (RMS roughness = 8 nm), consistent with the absence of thickness fringes in the XRD scan shown in figure 5. Membranes with this composition fractured during the release process, presumably because of the rough morphology. Again, MBE presents the opportunity for fabrication of tri-layer (110) membranes with significantly higher Ge content than is possible with CVD, and therefore the potential to obtain higher levels of tensile strain in the Si layers while keeping the surface roughness at an acceptable level. There also exists the option to build yet higher levels of strain by performing another growth sequence on an elastically strained membrane that has been transferred to an oxidized Si host, and subsequently releasing this new multi-layer membrane. The alloy layer in a second growth sequence is grown on an already tensilely strained Si surface, allowing growth of a higher-Ge-composition layer without dislocations (smaller lattice mismatch between the Si and alloy layers) [11].

We anticipate that strain sharing in Si(110) nanomembranes using just this single-release, CVD grown trilayer membrane will allow mobility enhancements of more than 20 and 35% for electrons and holes respectively [4]. For the strained-HOT geometry, the improvements should be even greater. The n-type devices can be fabricated on the high-electron-mobility (001) regions, while p-type devices formed on dislocation-free strained Si(110) could utilize hole mobility enhancements of up to 75% compared to the (001) universal mobility [4]. The ability to transfer the strained membranes also opens the possibility for optimizing channel direction in both types of devices via rotating the strained (110) membrane relative to its (001) host during transfer. The new (001) host could, of course, be a conventional SOI(001) substrate, which would enable a second release and transfer to almost any other surface, allowing the potential mobility enhancements in this novel combination membrane to be used in a vast array of emerging applications, such as flexible high-performance electronics.

4. Conclusions

We have demonstrated the formation, release, and transfer to a new host of elastically strain sharing Si nanomembranes with (110) orientation, starting from (110) oriented SOI. The elastic

strain sharing between the layers of a trilayer film generates defect-free tensilely strained Si(110) once the membrane is released by etching the oxide in SOI. High-resolution XRD is used to compare the strain state of the as-grown heterostructure (unrelaxed state) with that of the membrane after release from its growth substrate (which allows strain sharing between the layers), confirming elastic strain sharing. For layer thicknesses and compositions of 12 nm Si/80 nm $Si_{0.91}Ge_{0.09}$/10 nm Si, we obtain a tensile strain of $0.23 \pm 0.02\%$ in the Si layers. The XRD line scans reveal strong thickness fringes and uniform peak shifts after release, indicating coherency at the interfaces and elastic strain sharing without the generation of dislocations.

Higher Ge content in the alloy layer increases roughness using CVD and hence limits the magnitude of strain that can be obtained in the Si layers. A high level of roughness affects the release and transfer of membranes. MBE growth does not suffer from this limitation. Using a temperature for obtaining a smooth growth front allows the growth of higher-Ge-content membranes, and consequently, higher levels of defect-free tensile strain in the Si layers.

The membrane approach to straining Si(110) couples the use of elastic strain sharing with the versatility of a freestanding and very flexible membrane that may be transferred to a range of foreign surfaces and bonded readily. The potential for integration of a material with enhanced electronic properties on non-traditional surfaces (e.g., flexible substrates, diamond films), or on other orientations of Si (e.g., Si(001) in order to maximize both electron and hole mobility on a single wafer) seems considerable and deserving of further exploration.

Acknowledgments

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