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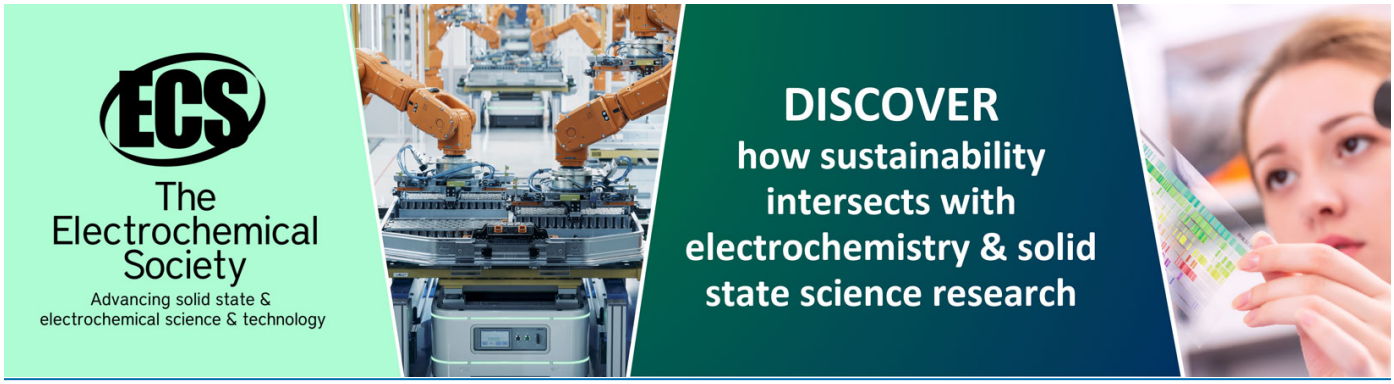

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The influence of AlN nucleation layer on RF transmission loss of GaN buffer on high resistivity Si (111) substrate

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Abstract

A sufficiently low transmission loss in radio frequency (RF) is one of the critical requirements for GaN-on-Si RF devices to achieve high performance. We have systematically studied the mechanism and effect of the AlN nucleation layer on the RF loss of the GaN-on-Si device buffer stack. Our results show that the RF loss is strongly influenced by the growth parameters of the AlN nucleation layer during epitaxial process. It is observed that the AlN nucleation layer grown at a low thermal budget with a low density of deep surface pits can efficiently reduce the AlN/Si interface loss by suppressing the conductive channel at AlN/Si interface which is governed largely by the thermal diffusion of Al and Ga into the Si substrate. By optimizing the growth process of the AlN nucleation layer, the RF loss of the GaN-on-Si device buffer can be dramatically reduced by up to ~40%.

Keywords: AlN nucleation layer, coplanar waveguides, GaN on Si, high frequency, RF loss, metalorganic chemical vapor deposition

(Some figures may appear in colour only in the online journal)

1. Introduction

GaN-based devices are attractive for high power and high frequency applications due to the high breakdown and high mobility characteristics of the GaN material [1, 2]. At present, SiC is commonly chosen as the substrate material for epitaxial growth of GaN devices for high frequency applications due to its low lattice mismatch towards GaN, high electric resistivity and high thermal conductivity [3]. However, GaN-on-Si RF devices are even more appealing due to the much lower cost and larger size of Si substrate compared to SiC substrate.

Having a good control during the epitaxial growth to obtain a low RF loss for GaN-on-Si devices is one of the challenges to achieve the desired RF performance. It is known that the total RF loss consists of 4 major elements: conductor loss, interface loss, dielectric loss and substrate loss [4]. For GaN-on-Si RF devices, the reduction of substrate loss is commonly achieved by using high resistive (HR) Si substrates [4, 5]. However, there have been very few dedicated studies regarding the sensitivity of RF loss performance of the GaN-on-Si structures on the Si substrate resistivity [6]. The choice of the optimum Si substrate resistivity is not straightforward either. It has to be made by taking into account of specific epitaxial and following device fabrication process; substrate cost (the higher the substrate resistivity usually the higher the substrate cost) and mechanical strength of the epi-wafers, etc.

Typical GaN-on-Si epitaxial process usually requires growing an AlN nucleation layer directly on Si substrate in order to prevent the melt-back etching [7]. This AlN nucleation layer is extremely critical because it largely determines the quality of the following epi layers grown on the top. The physical, chemical and electric nature of the AlN/Si interface are very complicated which may vary significantly depending on the specific epitaxial growth process.

As a result, the interface loss at the AlN/Si interface in the case of GaN-on-Si RF devices is much less well understood and is very difficult to control. When other RF loss mechanisms are sufficiently suppressed, a high interface loss may become the dominating factor to the total RF loss and consequently becomes the bottleneck of the RF performance of the device [3, 8]. The free carriers generated at the AlN/Si interface increase the interface conductivity and consequently increase the interface loss [9]. It is widely believed that the interface loss due to a high interface conductivity is induced by the Al and Ga diffusion into the Si substrate during the epitaxial growth, which forms a p-type parasitic conducting layer. Although there has been a report demonstrating the benefit of combining metalorganic chemical vapor deposition (MOCVD) process with low thermal budget on the AlN-on-Si template prepared by using Molecular Beam Epitaxy (MBE), the exact mechanism for the reduction of the RF loss is not fully understood [10]. On the other hand, a n-type inversion layer at the AlN/p-Si interface which is induced by the polarization field of the AlN layer has also been reported in recent years [6]. This inversion layer might not only enhance the leakage of the GaN buffer but also result in a high interface loss at equilibrium state [6, 11, 12]. Furthermore, the inversion layer at the AlN/Si interface induced by the applied bias may also affect the RF loss [13, 14]. Therefore, it is important to understand the electric characteristics at the AlN/Si interface under different bias conditions.

Despite that there were reports studying the effect of AlN/Si interface on the RF loss in recent years as previously mentioned, there have been lack of consistency in conclusions in literature due to the different characterization and growth techniques used. In order to have a deeper understanding on the RF loss mechanism in GaN-on-Si structure despite of diverse reports in literature, we have systematically investigated the RF loss mechanism for GaN-on-Si epi stacks by studying the key building blocks of the structure, including the Si substrate, AlN/Si template and the complete GaN-on-Si device buffer stack, with the main focus on the AlN nucleation layer.

2. Experimental

In the present study, all the samples were grown using a Veeco Turbodisc Maxbright MOCVD system with trimethylgallium (TMGa), trimethylaluminum (TMAl), and ammonia (NH_3) as precursors and N_2 as carrier gas. All samples were grown on 8 inch Si (111) substrates except those specified in table 1.

For the substrate loss study, an AlN nucleation layer with nominal thickness of 200 nm was grown at 1050 °C on p-type Si (111) substrates with different resistivity. The resistivity and diameter of the p-Si substrates are summarized in table 1.

In order to investigate the correlation between the thermal budget of epitaxial growth process and the RF loss, single AlN nucleation layers of different layer thicknesses, TH_{AlN}, were grown at different growth temperatures, GT_{AlN}, on Si substrate with resistivity of 3k–6k Ω cm. The variation of

Table 1. Summary of XRC FWHM of the AlN nucleation layer grown on different Si substrates, and the RF loss at 10 GHz obtained from different Si substrates with and without AlN nucleation layer.

		Loss at 10 GHz (dB mm^{-1})	
Si substrate Resistivity (Ω cm)	AlN (002) XRC FWHM (arcsec)	AlN/Si template	Bare Si substrate
1–3 (8 inch)	1580	7.6	
2–10 (6 inch)	1540	5.2	
1–150 (6 inch)	1550	2.4	4.6
0.5k–2k (8 inch)	1560	0.21	0.15
3k–6k (8 inch)	1520	0.24	0.14
3k–20k (6 inch)	1545	0.25	

TH_{AlN} was realized by changing the growth time, while all other growth parameters were kept constant expect the GT_{AlN}. Samples with a nominal TH_{AlN} of 200 nm grown at temperature of 930 °C, 970 °C, 1010 °C and 1050 °C are labeled as Samples A, B, C and D, respectively. Samples with a nominal TH_{AlN} of 175 and 250 nm grown at 1010 °C are labeled as Samples E and F, respectively. Figure 1(a) shows the schematic structure of Samples A–F. A rather constant growth rate of ~2.63 nm min^{-1} was obtained for the AlN nucleation layer within the entire growth temperature range studied. Finally, device buffer stacks with a total thickness of 2.5 μm were grown. Figure 1(b) shows the schematic structure of Samples A_1–F_1, which are the device buffer stacks with the AlN nucleation layer grown under the growth conditions corresponding to that for Samples A–F, respectively. This is to study the influence of AlN nucleation layer growth parameters on the RF loss of the device buffer stacks. Along the growth direction, the device buffer stack includes: an AlN nucleation layer, an AlGaN transition layer, an AlN/AlGaN superlattice, a C doped GaN layer and an unintentionally doped (uid)-GaN channel layer. Among the different samples, the growth process of the buffer stack was identical except that of the AlN nucleation layer.

Surface morphologies of all samples were examined by atomic force microscopy (AFM) with a Bruker Dimension ICON-PT system. All the AFM images are with a scan size of 5 × 5 μm^2. X-ray rocking curves (XRC) around AlN (002), GaN (002) and GaN (102) diffraction peaks were recorded by using a Bruker QC3 diffractometer system (CuKα1 radiation). 9 locations were measured on each sample and the average value was reported. Etched samples were all processed by inductively coupled plasma (ICP) etching technique using an Oxford Plasmalab100 system. Chemical profiling of elements of interest was performed by time-of-flight secondary ion mass spectrometry (ToF-SIMS) with a ToF-SIMS/scanning probe microscopy (SPM) instrument (ION-TOF GmbH, Germany). ToF-SIMS specimens were prepared by thinning the AlN layer down to ~40 nm by ICP dry etching. The surface root mean square (RMS) roughness of the starting surface of etched samples and the surface RMS roughness near the AlN/Si interface during ToF-SIMS measurement SPM were measured as ~1 nm (in 5 × 5 μm^2 scan

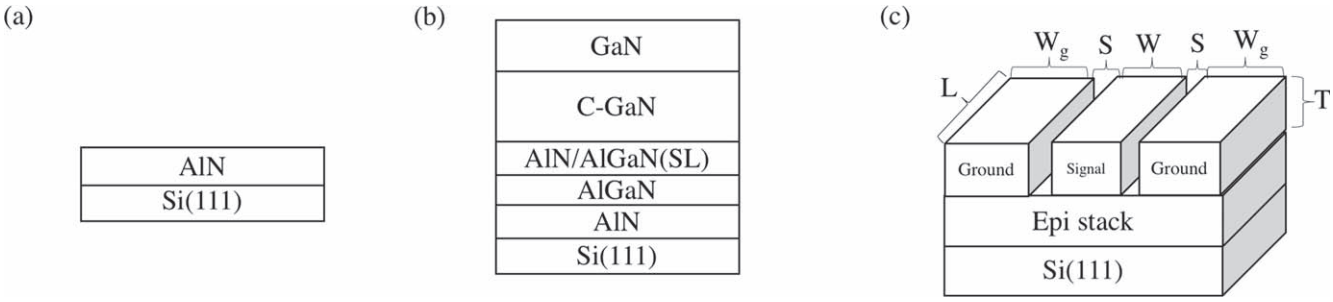

Figure 1. Schematic of different structures studied in this work. (a) Single AlN nucleation layer grown on Si substrate with different growth parameters for Samples A–F. (b) Device buffer stack for Samples A_1–F_1. (c) CPW structure.

area) by *in situ* AFM which is sufficiently low such that no influence was expected to the ToF-SIMS results. For the ToF-SIMS measurements (dual beam experiments using Bi_1^+ 15 kV and O_2^+ 500 eV), the influence of the push-in effect near the interface has to be considered. However, the density of the AlN near the AlN/Si interface was not expected to be dramatically different, consequently the amount of Al which was pushed into Si substrate by the push-in effect should be similar in all samples. The Al intensity was quantified in the Si substrate using Al in Si reference sample with known Al concentration. However, the Si in the AlN is not quantified due to the lack of proper reference samples.

Coplanar waveguide (CPW) structures as depicted in figure 1(c) were fabricated on all the samples for RF loss measurement. The signal line and ground plane consist of a bi-metal layer of 10 nm Ti/500 nm Au. The width of ground plane, W_g, is 400 μm. The width of the signal line, W, is 75 μm. The spacing, S, and length of the transmission line, L, are 50 μm and 2 mm, respectively. The RF loss were measured at room temperature by using an AGT E8363B Network Analyzer with the substrate grounded. The measured S-parameters were transferred to the RF loss (equivalent to attenuation constant) by using the formulation in [15]. The presented RF loss values at 10 GHz are averaged from measurements of 4 random CPW devices on one sample except for the bias-dependent RF loss measurements where 1 device was measured to avoid unaffordable long measurement time.

3. Results and discussion

3.1. The effect of Si substrate resistivity

Table 1 summarizes the full width at half maximum (FWHM) of XRCs around the AlN (002) diffraction peak and the RF loss of AlN/Si templates prepared on various p-Si substrates. All AlN layers showed similar FWHM values around 1500 arcsec, indicating an essentially identical crystalline quality among all the samples. However, figure 2 shows that the RF loss of AlN/Si templates monotonically reduces as the Si substrate resistivity increases from 1–3 Ω cm to 0.5k–2k Ω cm, and then stays rather constant as the Si substrate resistivity further increases. This suggests that the substrate loss very likely dominates the total RF loss for the Si resistivity below 0.5k–2k Ω cm. As the Si substrate resistivity is

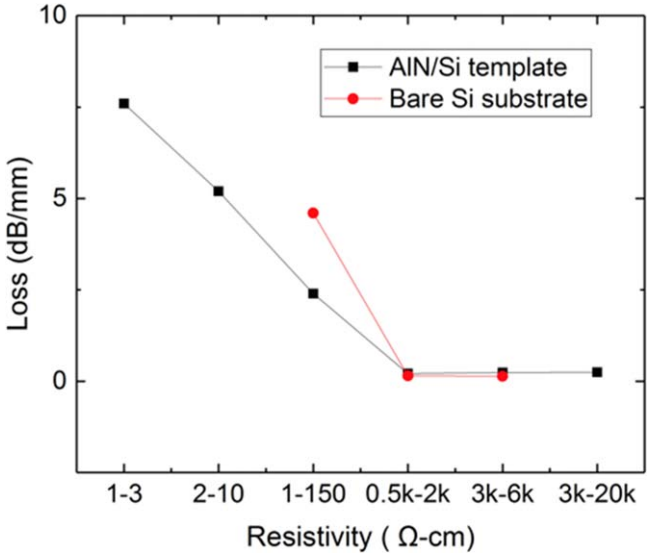

Figure 2. The RF loss at 10 GHz from AlN/Si templates and bare Si substrates with various Si substrate resistivity.

higher than 0.5k–2k Ω cm, the contribution of the substrate loss to the total RF loss becomes significantly small so that the total RF loss is no longer sensitive towards the change of Si substrate resistivity. In order to further verify and understand the observation above, the RF loss measurement was also carried out on 3 bare Si substrates with resistivities around 0.5k–2k Ω cm. As shown in figure 2, the trend of RF loss of the bare Si substrate is similar to that of the AlN/Si template when the Si substrate resistivity increases and cross 0.5k–2k Ω cm range. This leads to the conclusion that the substrate loss component becomes clearly insignificant when the Si substrate resistivity is within or above the range of 0.5k–2k Ω cm.

It is a common method to reduce the substrate loss by introducing a dielectric layer between the substrate and the coplanar lines to reduce the propagation of the electric field into the substrate [16–18]. This explains the observation that the RF loss of AlN/Si template is lower than the RF loss of bare Si at Si substrate resistivity of 1–150 Ω cm. However, in the case where the Si substrate resistivity is ⩾0.5k–2k Ω cm, the RF loss of the AlN/Si template is slightly higher than that of the counterpart bare Si substrate as shown in table 1 and figure 2. This additional RF loss can be explained by the other components of RF loss. The conductor loss should be

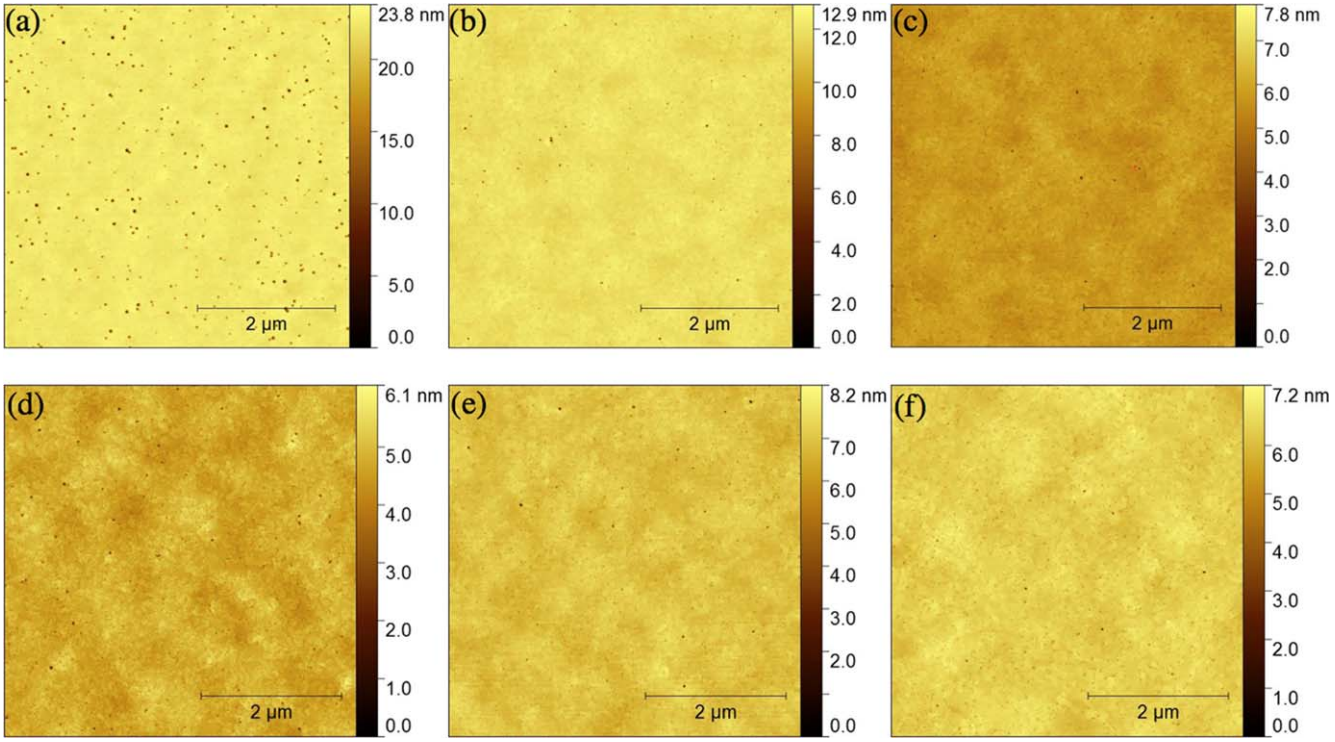

Figure 3. AFM images (5×5 μm^2 scan area) of Samples A–F, respectively.

identical for every sample due to the same metallization process of the transmission line. However, the contribution of interface loss and dielectric loss components introduced by the epitaxial process and the AlN nucleation layer may be higher than the reduction of the substrate loss after growing an AlN nucleation layer on the Si substrate. As a result, the RF loss of the AlN/Si template is likely dominated by interface loss and dielectric loss at Si substrate resistivity of $\geqslant$0.5k–2k Ω cm. Therefore, it is very important to be able to control and minimize not only the dielectric loss from the AlN nucleation layer but also the interface loss at AlN/Si interface.

3.2. AlN/Si template

The growth parameters and the physical characterization results of Samples A–F are summarized in table 2. The AFM images of all samples are shown in figure 3. For Samples A–D, the TH_{AlN} was kept constant at 200 nm and only the GT_{AlN} increases from 930 °C to 1050 °C. One can see from these 4 samples that the AlN (002) XRC FWHM first decreases and then increase as the GT_{AlN} increases, with the lower values (namely a better crystalline quality) obtained in 970 °C–1010 °C range. A somewhat similar trend also appears in the surface RMS roughness and the deep pit density. However, the initial decrease in value is much more significant once the GT_{AlN} increases to 970 °C–1010 °C range. Table 2 also shows that the surface peak-to-valley (PV) value decreases monotonically as increasing the GT_{AlN}. The worst crystalline and morphological quality of the AlN nucleation layer grown at 930 °C can be easily understood because this temperature is clearly too low. The low atom mobility at this low temperature hinders coalescence of the grains concomitant with a higher density of defects [19–21]. On the other hand, the serious Si out-diffusion in AlN nucleation layer and the nanoparticles generated via parasitic gas phase reaction between TMAl and NH_3 at the unfavorably high GT_{AlN} of 1050 °C explains the deteriorated crystalline quality [20, 22]. Considering all the characterization results, 1010 °C is identified as the optimum GT_{AlN} for a 200 nm AlN nucleation layer in the current study.

The effect of the TH_{AlN} was studied via Samples C, E and F where the GT_{AlN} was fixed at 1010 °C. The AlN (002) XRC FWHM of those samples clearly decreased with increasing TH_{AlN}. The threading dislocation recombination and annihilation can be enhanced with increasing the layer thickness, resulting in the reduction of the total number of threading dislocations [23]. However, surface RMS roughness and deep pit density are insensitive on the layer thickness of AlN layer in 175–250 nm range because the growth mode of the AlN nucleation layer is already stabilized [24].

The RF loss values at 10 GHz for Samples A–D are shown in figure 4(a). There is a general trend that the RF loss increases with increasing the GT_{AlN} from 930 °C to 1050 °C. However, this trend does not show any correlation with either the crystalline or morphological quality of these 4 samples as summarized in table 2. This increase of RF loss may be attributed to the change in interface loss at AlN/Si interface and the dielectric loss from the AlN nucleation layer, respectively. It is known that the dielectric loss of the insulator is always very low due to its extremely high resistivity [4, 25, 26]. Although the resistivity of the insulator cannot be obtained by using common measurement techniques, an extremely high resistivity of $\sim 10^{13}$ Ω cm was extracted for

Table 2. Growth parameters and physical characterization results of Samples A–F.

	Sample A	Sample B	Sample C	Sample D	Sample E	Sample F
AlN layer growth temperature, GT_{AlN} (°C)	930	970	1010	1050	1010	1010
AlN layer thickness, TH_{AlN} (nm)	200	200	200	200	175	250
AlN (002) XRC FWHM (arcsec)	1570	1340	1345	1520	1435	1200
AFM surface RMS (nm)	0.88	0.25	0.23	0.27	0.25	0.23
AFM PV (nm)	24	13	8	6	8	7
Deep pit density (pit depth >3 nm) ($\#/cm^2$)	9×10^8	1.5×10^8	3×10^7	4.5×10^7	5.5×10^7	2×10^7

AlN by Francis *et al* [27]. This suggests that the dielectric loss component must be very low and cannot be the main contributor to the change of the RF loss in all samples. As a result, the increase of RF loss in figure 4(a) is mostly attributed to the interface loss which is at least associated with a temperature-driven process. Therefore, the thermal diffusion of Al into Si substrate during the growth could be one of the candidates according to [3].

The RF loss values for Samples C, E and F with TH_{AlN} from 175 to 250 nm grown at 1010 °C are shown in figure 4(b). The RF loss increases with increasing the TH_{AlN} and this trend is not in correlation with either the crystalline or morphological quality of these 3 samples as summarized in table 2. In order to fully understand the effect of TH_{AlN} on RF loss, the contributions of both the thickness effect and the thermal effect have to be taken into account because of the following considerations. Increasing the TH_{AlN} may decrease the substrate loss because the capacitance of AlN, C_{AlN}, which reduces as the thickness increases ($C \propto 1/\text{thickness}$) can consequently reduce the propagation of the electric field into the substrate [6, 18]. Besides, it is reported in [12] by Luong *et al* that the n-type inversion layer at the AlN/p-Si interface may increase with increasing TH_{AlN} due to the increase of the polarization field at AlN/p-Si interface. This consequently results in a higher interface loss [6]. In the present study, a larger TH_{AlN} also led to a higher total thermal budget in the epitaxial growth. The amount of Al diffusion into the Si substrate might hence increase during the epitaxial growth and consequently increase the interface loss by enhancing the p-type conductive channel near the AlN/Si interface.

In order to decouple the thickness effect and thermal effect on the RF loss as described above, 2 additional samples were prepared. The 200 nm AlN nucleation layer in Sample C was etched down to 150 and 100 nm, so that all these 3 samples experienced exactly the same thermal budget during the epitaxial growth process. The surface RMS roughness of the etched samples is ~0.35 nm which is sufficiently low for the RF loss measurement. Figure 4(c) shows that the RF loss increases as thinning the AlN layer. This observation indicates that the impact of C_{AlN} change is more significant than the change of the polarization field as varying TH_{AlN}. Therefore, the trend of the RF loss for the as-grown samples shown in figure 4(b) is considered mainly attributed to the associated thermal effect.

To further study in detail the thermal effect on the RF loss, ToF-SIMS measurements were performed on Samples A, C and D, which were grown in different GT_{AlN} with same nominal thickness of 200 nm. Figure 5 summarizes the chemical profiles of Al and Si near the AlN/Si interface from these 3 samples. The profiles are aligned at the AlN/Si interface where the Si intensity is 50% of that of the bulk Si substrate. As GT_{AlN} increases, the inter-diffusion of Al and Si are clearly stronger across the AlN/Si interface. Because Al is a p-type dopant in Si, the region of the Si substrate affected by the Al in-diffusion very likely forms a p-type conductive channel underneath the AlN/Si interface. As a natural consequence, the sample with a stronger thermal diffusion of Al into Si will have a channel with a higher conductivity and results in a higher interface loss. Besides the Al diffusion into Si, one can also see that there is a clear diffusion of Si cross the interface into the AlN layer. Si is a well-known n-type dopant in III-N materials, while it has been reported that the Si may undergo a shallow-deep transition to become a deep donor in $Al_xGa_{1-x}N$ when $x \geqslant 40$ at% [28, 29]. This suggests that Si dopants are very likely not electrically active in the AlN nucleation layer and have no influence to the observed interface loss. By taking the RF loss plot in figure 4(a) and the diffusion profiles in figure 5 into account, we conclude that a weaker thermal diffusion of Al into Si substrate at a lower GT_{AlN} reduced the interface loss by mitigating the conductive p-type channel underneath the AlN/Si interface. Therefore, the thermal diffusion of Al into Si substrate is identified as the main contributor to the interface loss at the AlN/Si interface.

Moreover, it has been reported by Chandrasekar *et al* that the S–O–N complexes can act as thermal acceptors and possibly form at the top surface of the Si near the AlN/p-Si interface during the high temperature growth [30]. The density of such S–O–N complexes may increase with increasing the growth thermal budget of the AlN nucleation layer [30]. However, in Samples A, C and D, we observed a nearly identical diffusion profiles of O and N into the Si substrate from ToF-SIMS measurement (not shown). This largely rules out an appreciable effect of the possible S–O–N complexes in our work.

Capacitance–voltage (*CV*) measurement has been widely used to investigate the electric characteristics of the AlN/Si interface. Accumulation, depletion and inversion conditions can be observed when the bias applied on AlN/p-Si template changes from negative voltage to positive voltage [13, 31]. However, the HR Si substrate makes *CV* measurements very difficult due to the additional contribution from the substrate capacitance. As an alternative, bias can be applied on the signal line during the RF loss measurements in order to study

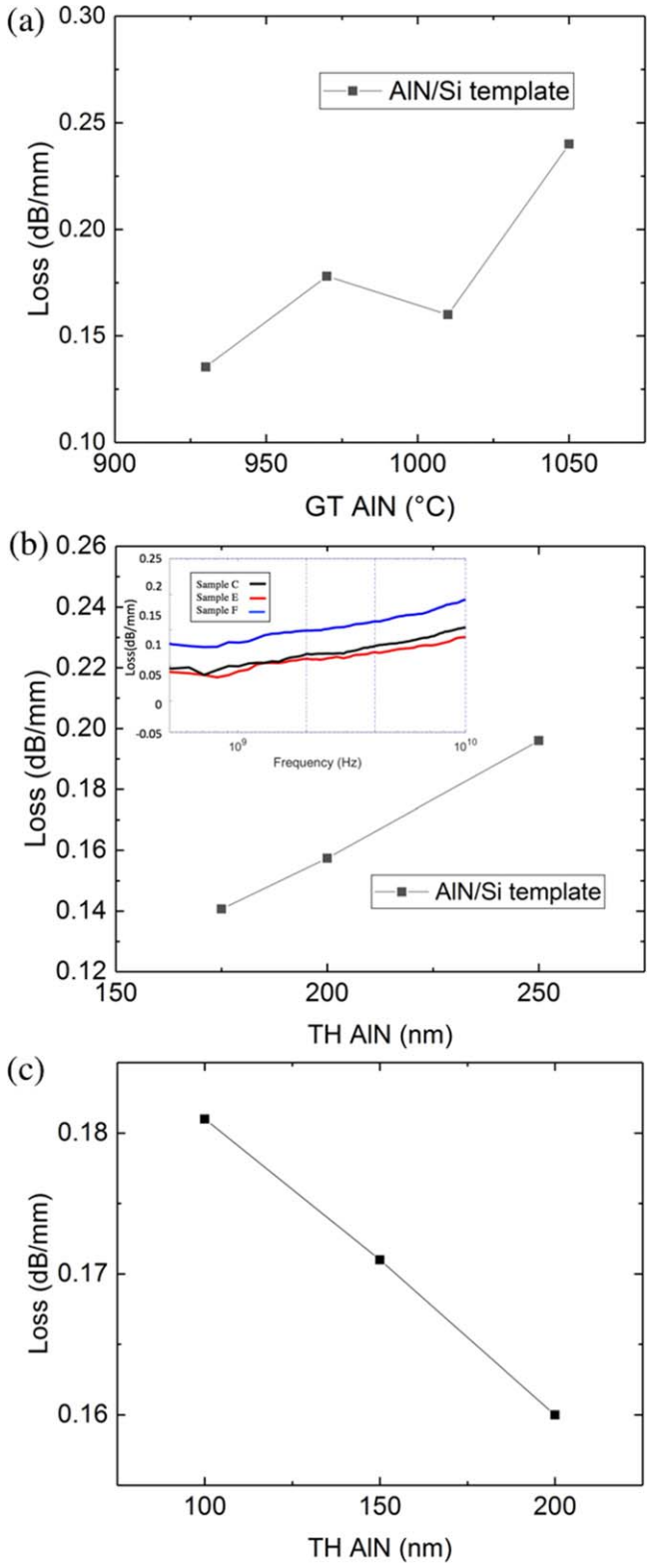

Figure 4. (a) RF loss of AlN/Si template with TH_{AlN} of 200 nm versus the GT_{AlN}. (b) RF loss of AlN/Si template grown at 1010 °C versus the TH_{AlN}. The inset of figure 4(b) is the frequency dependency RF loss profiles for Samples C, E and F in one measured device. (c) RF loss versus the AlN thickness for the samples etched from Sample C by ICP.

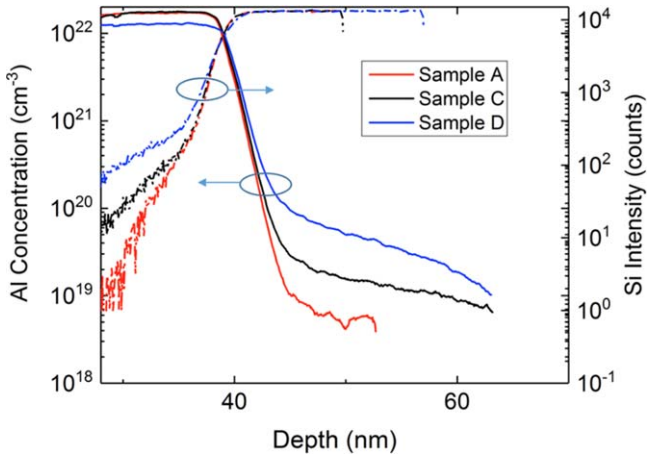

Figure 5. ToF-SIMS chemical profiles of Al and Si as a function of depth for Samples A, C, and D. Al quantified in Si substrate and Si not quantified in AlN.

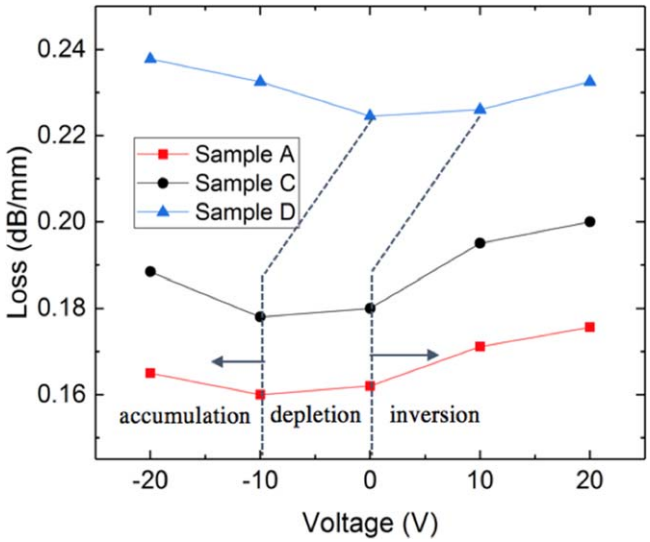

Figure 6. Bias-dependent loss of Samples A, C and D at 10 GHz.

the electric nature of the Si substrate near the AlN/Si interface [4, 32].

Such bias-dependent RF loss measurements were carried out on Samples A, C and D and results are summarized in figure 6. There are several observations can be made from figure 6. One can see in figure 6 that the RF loss of AlN/Si template decreases overall with decreasing GT_{AlN} in the full range of applied bias. This is due to the lower conductivity at AlN/Si interface associated with the lower concentration of the diffused Al into the Si substrate (figure 5).

In addition, the bias-dependent RF loss curves of all samples in general exhibit a 'U' shape in the applied bias range from −20 to 20 V. The similar U-shape bias-dependent RF loss curve has also been reported on metal–oxide semiconductor (MOS) varactors in [4]. The RF loss is higher at both accumulation and inversion conditions due to the increase of interface loss by the bias-induced carrier concentration enhancement near the interface. The interface loss reaches the minimum under the depletion condition where the

Table 3. Summary of growth parameters and physical characterization results of Samples A_1–F_1.

	Sample A_1	Sample B_1	Sample C_1	Sample D_1	Sample E_1	Sample F_1
AlN nucleation layer growth temperature, GT_{AlN} (°C)	930	970	1010	1050	1010	1010
AlN nucleation layer thickness, TH_{AlN} (nm)	200	200	200	200	175	250
GaN(002) XRC FWHM (arcsec)	680	690	685	700	720	675
GaN(102) XRC FWHM (arcsec)	1445	1470	1320	1360	1465	1305
AFM RMS (nm)	0.4	0.35	0.60	0.55	0.5	0.5
AFM PV (nm)	6.5	5	5	6	5.5	4

free carriers are pushed away far from the interface. Following the same analysis, the regions corresponding to accumulation, depletion and inversion conditions can be identified and are indicated in figure 6. Although the interval of the applied bias is relatively large to identify more precisely the depletion condition, it is still sufficient for investigating the behavior of carriers at AlN/Si interface.

The depletion region (around turning point of the curves) for Samples A and C is located approximately in the bias range from −10 to 0 V, but it clearly shifts along the positive bias direction to the range from 0 to 10 V for Sample D. For Samples A and C, the fact that the location of the depletion region is near the negative bias range suggests a weak n-type conductivity at equilibrium near the interface. In contrast, the depletion for Sample D occurs in the positive bias range, which indicates a switch of the conductive channel to slight p-type at equilibrium near the interface compared with the other 2 samples. In figure 5, the Al thermal diffusion into Si substrate is observed in all samples. However, the Al diffusion for Samples A and C is much weaker compared with Sample D. Several groups have reported the existence of polarization-introduced n-type inversion layer in AlN/p-Si templates [6, 13]. We speculate this n-type inversion layer is induced in Samples A and C (with lower Al diffusion) by polarization field at AlN/Si interface. Thus, conductive channel near the interface consequently exhibits a weak n-type. However, as the Al thermal diffusion became much stronger when GT_{AlN} was increased to 1050 °C for Sample D, the resultant hole concentration surpassed the concentration of polarization introduced electrons. The interface conductive channel thus exhibits a weak p-type conductivity.

According to the bias-dependent RF loss and the ToF-SIMS results, the thermal diffusion of Al into the Si substrate which can increase the conductivity at AlN/Si interface is indeed a main contributor to the RF loss for AlN/Si template. However, it is observed when the p-type background near the AlN/Si interface, which is determined by the thermal diffusion of Al into Si substrate is low enough, the n-type inversion channel can play an important role in RF loss. Therefore, it is also important to study the n-type inversion layer induced by the polarization filed at AlN/Si interface to further improve the RF loss in AlN/Si template.

3.3. Device buffer stack

At last, Samples A_1–F_1 which contain identical device buffer stack up to the GaN channel layer (without the active layers) were grown with the same AlN nucleation layer growth condition (namely, thickness and growth temperature) as that for Samples A–F. The growth parameters and the physical characterization results of Samples A_1–F_1 are summarized in table 3.

In table 3, one can see that although the FWHM values of GaN (002) XRC for Samples A_1–D_1, are all very similar and are around 700 arcsec, FWHM of GaN (102) XRC decreases from ∼1450 to ∼1350 arcsec as GT_{AlN} increases from 930 °C–970 °C to 1010 °C–1050 °C. The broadening of the symmetric GaN (002) XRC is associated with the density of screw type of dislocations and asymmetric GaN (102) XRC with the density of mixed and pure edge types of dislocations [33]. A similar density of screw type dislocations can be expected for the above 4 samples but the density of mixed and pure edge type of dislocations is obviously lower for Samples C_1 and D_1. This indicates that a higher GT_{AlN} in 1010 °C–1050 °C range is beneficial to the crystalline qualify of the device buffer stack. Despite the clear difference in crystalline quality, the surface morphology of all the samples looks very similar without appreciable abnormalities. The AFM image of Sample D_1 is shown in figure 7(a) as a typical example. There is no systematic difference observed among these 4 samples either in terms of the surface RMS roughness and PV value. This suggests that the growth process of the device buffer is properly tuned such that the surface morphology can be effectively recovered from the initially unfavorable condition after the AlN nucleation layer as shown in the case of Sample A.

For Samples C_1, E_1 and F_1 which grown with TH_{AlN} varied from 175 to 250 nm, it is observed that the FWHM of both GaN (002) and GaN (102) XRCs slightly decreases with increasing TH_{AlN}. The difference in terms of surface RMS roughness and PV are negligible among these 3 samples, which is similar to the case of AlN/Si templates as well (i.e. Samples C, E and F). This indicates that TH_{AlN} has a strong influence on the crystalline quality but not on the surface morphology.

Figure 7(b) shows the RF loss of device buffer stacks (namely, Samples A_1–D_1) and AlN/Si templates (namely, Samples A–D) as a function of GT_{AlN}. The RF loss of the device buffer stacks is overall higher than that of the corresponding AlN/Si templates and the increase of the RF loss within the corresponding sample pairs is defined as 'Δ loss'. As shown in figure 7(b), the RF loss values of device buffer stacks are almost the same when the GT_{AlN} is in 930 °C–970 °C range. With further increase of GT_{AlN}, the RF

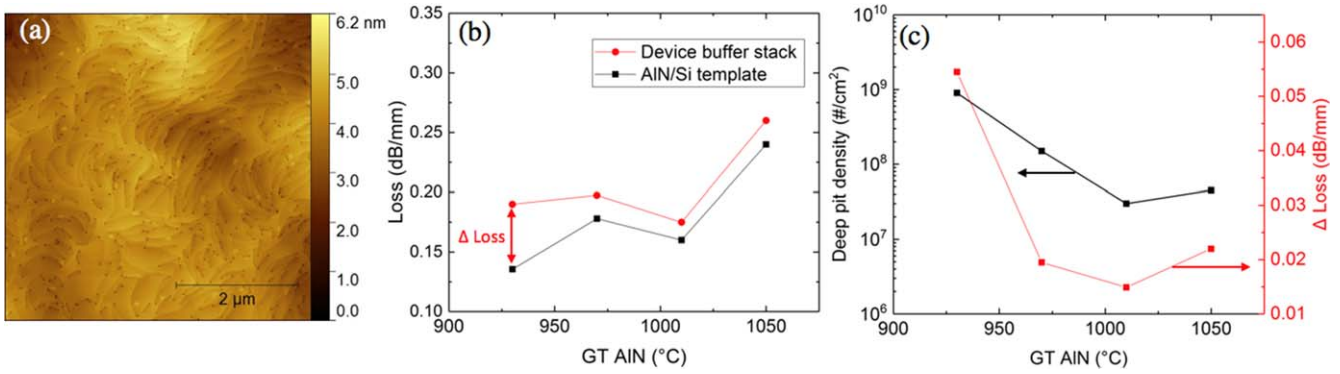

Figure 7. (a) AFM surface image ($5 \times 5\ \mu m^2$ scan area) of Sample D_1. (b) RF loss of device buffer stack and AlN/Si template versus GT_{AlN} (TH_{AlN} is 200 nm). (c) The density of deep pit on AlN nucleation layer surface and the Δ loss versus GT_{AlN} (TH_{AlN} is 200 nm).

loss first slightly decreases at $GT_{AlN} = 1010\,^{\circ}C$ and then dramatic increases as GT_{AlN} reaches 1050 °C. On the other hand, this trend in RF loss does not show any correlation with either the crystalline or morphological quality of these 4 samples as summarized in table 3.

Because the only difference between Samples A–D series and Samples A_1–D_1 series is the structure of epi stack, we therefore consider 2 possible causes that might contribute to the Δ loss in Samples A_1–D_1 series. First, there may be one or more additional conductive channels introduced within the device buffer stack leading to a higher dielectric loss. Second, there could also be extra Al and Ga diffusion into Si substrate after the growth, enhancing the interface loss at the AlN/Si interface [3, 8]. Since the identical buffer stack was grown after the AlN nucleation layer in Samples A_1–D_1 series, the first factor cannot explain the relative difference in Δ loss at different GT_{AlN}. To investigate the RF loss mechanism, the Δ loss and the deep pit density on the AlN/Si template is plotted as a function of GT_{AlN} in figure 7(c). It is found in figure 7(c) that the evolution in the density of deep pit as listed in table 2 matches fairly well with the trend of Δ loss as GT_{AlN} increases. It has been reported that the threading dislocations can act as diffusion paths for atoms during both epitaxial growth and annealing processes at high temperature [34, 35]. We speculate that the deep pits and the associated dislocations of the AlN nucleation layer facilitate the diffusion of Al and Ga into the Si substrate during the following epitaxial layer in the device buffer stack and consequently increase the Δ loss by increasing the conductivity at the AlN/Si interface.

The RF loss of device buffer stacks and AlN/Si templates with various TH_{AlN} grown at 1010 °C are presented in figure 8. The RF loss of both structures increase as TH_{AlN} increases from 175 to 250 nm. However, this trend of RF loss does not show any correlation with either the crystalline or morphological quality of these 3 samples as summarized in table 3. Although the thinner AlN nucleation layer in device buffer stack may lead to a shorter path for the following Al and Ga diffusion into the Si substrate and potentially increase the Δ loss, a nearly constant Δ loss value can be observed in figure 8, suggesting a rather low sensitivity of Δ loss towards the TH_{AlN}. Therefore, the nearly constant Δ loss value is mainly attributed to the similar density of deep pit on the surface of AlN/Si templates as listed in table 2, upon the same Al and Ga diffusion mechanism through the deep pits as explained above.

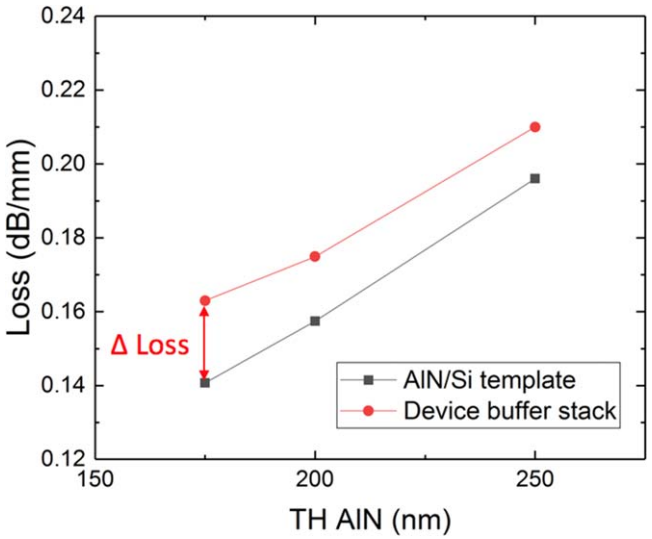

Figure 8. RF loss of device buffer stack and AlN/Si template versus the TH_{AlN} grown at the same temperature of 1010 °C.

4. Conclusions

The influence of AlN nucleation layer on RF loss of GaN-on-Si device buffer stacks was systematically investigated in this work. In our study, we found that the contribution of the substrate loss to the total RF loss was no longer the dominant factor when the Si substrate resistivity was within or above the range of 0.5k–2k Ω cm. In additional, by using various characterization techniques on both AlN/Si template and device buffer stack, we found that the interface loss became the main contributor to the total RF loss in device buffer stack. This interface loss is mainly attributed to the parasitic conductive channel due to the thermal diffusion of Al and Ga into Si substrate which is strongly determined by the growth thermal budget of the AlN nucleation layer. Although reducing the growth thermal budget of AlN nucleation layer can mitigate the thermal diffusion of Al into Si substrate, an

unfavorably GT_{AlN} can also lead to a higher density of surface deep pits on the AlN nucleation layer and consequently induces a higher interface loss at AlN/Si interface by facilitating extra thermal diffusion of Al and Ga into the Si substrate during the following epitaxial growth. Therefore, it is crucial to minimize the growth thermal budget and ensure the morphological quality of the AlN nucleation layer at the same time to suppress the RF loss in device buffer stack. We demonstrated that the RF loss of ~0.16 dB mm^{-1} at 10 GHz from a full RF device buffer stack with an optimized AlN nucleation layer with a thickness of 175 nm grown at 1010 °C. This is ~40% lower than that of a device buffer stack with a 200 nm thick AlN nucleation layer grown at 1050 °C.

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References

[1] Mishra U K, Parikh P and Yi-Feng W 2002 AlGaN/GaN HEMTs-an overview of device operation and applications *Proc. IEEE* **90** 1022–31
[2] Kato S, Satoh Y, Sasaki H, Masayuki I and Yoshida S 2007 C-doped GaN buffer layers with high breakdown voltages for high-power operation AlGaN/GaN HFETs on 4-in Si substrates by MOVPE *J. Cryst. Growth* **298** 831–4
[3] Shinichi H, Masanori I, Toshiharu M, Hideyuki O, Yoshiaki M, Isao T, Fumihiko T, Shohei S and Takashi E 2009 12.88 W/mm GaN high electron mobility transistor on silicon substrate for high voltage operation *Appl. Phys. Express* **2** 061001
[4] Schollhorn C, Weiwei Z, Morschbach M and Kasper E 2003 Attenuation mechanisms of aluminum millimeter-wave coplanar waveguides on silicon *IEEE Trans. Electron Devices* **50** 740–6
[5] Reyes A C, El-Ghazaly S M, Dorn S J, Dydyk M, Schroder D K and Patterson H 1995 Coplanar waveguides and microwave inductors on silicon substrates *IEEE Trans. Microwave Theory Tech.* **43** 2016–22
[6] Luong Tien T, Lumbantoruan F, Chen Y-Y, Ho Y-T, Weng Y-C, Lin Y-C, Chang S and Chang E-Y 2017 RF loss mechanisms in GaN-based high-electron-mobility-transistor on silicon: role of an inversion channel at the AlN/Si interface *Phys. Status Solidi* a **214** 1600944
[7] Zhu D, Wallis D J and Humphreys C J 2013 Prospects of III-nitride optoelectronics grown on Si *Rep. Prog. Phys.* **76** 106501
[8] Rajagopal P, Roberts J C, Cook J W, Brown J D, Piner E L and Linthicum K J 2011 Symposium Y: Gan and related alloys MOCVD AlGaN/GaN HFETs on Si: challenges and issues *MRS Proc.* **798** Y7.2
[9] Yamaguchi Y, Kamioka J, Shinjo S, Yamanaka K and Oishi T 2016 Physical model of RF leakage in GaN HEMTs on Si substrates based on atomic diffusion analysis at buffer/substrate interface *2016 IEEE Compound Semiconductor Integrated Circuit Symp. (CSICS)* pp 1–4
[10] Cordier Y, Comyn R, Frayssinet E, Khoury M, Lesecq M, Defrance N and De Jaeger J-C 2017 Influence of AlN growth temperature on the electrical properties of buffer layers for GaN HEMTs on silicon *Phys. Status Solidi* a **215** 1700637
[11] Zhiyuan H *et al* Investigations of leakage current properties in semi-insulating GaN grown on Si(111) substrate with low-temperature AlN interlayers *J. Phys. D: Appl. Phys.* **47** 2014045103
[12] Zhou C, Jiang Q, Huang S and Chen K J 2012 Vertical leakage/breakdown mechanisms in AlGaN/GaN-on-Si devices *IEEE Electron Device Lett.* **33** 1132–4
[13] Yacoub H, Eickelkamp M, Fahle D, Mauder C, Alam A, Heuken M, Kalisch H and Vescan A 2015 The effect of AlN nucleation growth conditions on the inversion channel formation at the AlN/silicon interface *2015 73rd Annual Device Research Conf. (DRC)* pp 175–6
[14] Freedsman J J, Watanabe A, Yamaoka Y, Kubo T and Egawa T 2015 Influence of AlN nucleation layer on vertical breakdown characteristics for GaN-on-Si *Phys. Status Solidi* a **213** 424–8
[15] Eisenstadt W R and Eo Y 1992 S-parameter-based IC interconnect transmission line characterization *IEEE Trans. Compon. Hybrids Manuf. Technol.* **15** 483–90
[16] Jin-Su K, Bon-Kee K and Kwyro L 1997 Simple modeling of coplanar waveguide on thick dielectric over lossy substrate *IEEE Trans. Electron Devices* **44** 856–61
[17] Henri H, Gonzague S, Matthieu V, Alain C and Gilles D 2000 Ultra low loss transmission lines on low resistivity silicon substrate *2000 IEEE MTT-S Int. Microwave Symp. Digest (Cat. No.00CH37017)* vol 1803, pp 1809–12
[18] Reyes A C, El-Ghazaly S M, Dorn S, Dydyk M and Schroder D K 1994 Silicon as a microwave substrate *1994 IEEE MTT-S Int. Microwave Symp. Digest (Cat. No.94CH3389-4)* vol 1753, pp 1759–62
[19] Chernykh M Y, Ezubchenko I S, Mayboroda I O and Zanaveskin M L 2019 Influence of the growth conditions of LT-AlN on quality of HT-AlN growth on Si (1 1 1) by metalorganic chemical vapor deposition *J. Cryst. Growth* **507** 200–4
[20] Lu Y, Liu X, Wang X, Lu D-C, Li D, Han X, Cong G and Wang Z 2004 Influence of the growth temperature of the high-temperature AlN buffer on the properties of GaN grown on Si(111) substrate *J. Cryst. Growth* **263** 4–11
[21] Wang H, Li S L, Xiong H, Wu Z H, Dai J N, Tian Y, Fang Y Y and Chen C Q 2012 The effect of AlN nucleation temperature on the growth of AlN films via metalorganic chemical vapor deposition *J. Electron. Mater.* **41** 466–70
[22] Gaubas E *et al* 2017 Study of recombination characteristics in MOCVD grown GaN epi-layers on Si *Semicond. Sci. Technol.* **32** 125014
[23] Mathis S K, Romanov A E, Chen L F, Beltz G E, Pompe W and Speck J S 2001 Modeling of threading dislocation reduction in growing GaN layers *J. Cryst. Growth* **231** 371–90

[24] Wei M, Wang X, Pan X, Xiao H, Wang C, Hou Q and Wang Z 2011 Effect of AlN buffer thickness on GaN epilayer grown on Si(111) *Mater. Sci. Semicond. Process.* **14** 97–100
[25] Simons R N 2001 *Coplanar Waveguide Circuits, Components, and Systems* (New York: Wiley)
[26] Tataroğlu A, Altındal Ş and Bülbül M M 2005 Temperature and frequency dependent electrical and dielectric properties of $Al/SiO_2/p$-Si (MOS) structure *Microelectron. Eng.* **81** 140–9
[27] Francis R W and Worrell W L 1976 High temperature electrical conductivity of aluminum nitride *J. Electrochem. Soc.* **123** 430–3
[28] Van de Walle C G and Neugebauer J 2004 First-principles calculations for defects and impurities: applications to III-nitrides *J. Appl. Phys.* **95** 3851–79
[29] Taniyasu Y, Kasu M and Kobayashi N 2002 Intentional control of n-type conduction for Si-doped AlN and $Al_xGa_{1-x}N$ ($0.42 \leqslant x < 1$) *Appl. Phys. Lett.* **81** 1255–7
[30] Chandrasekar H, Bhat K N, Rangarajan M, Raghavan S and Bhat N 2017 Thickness dependent parasitic channel formation at AlN/Si interfaces *Sci. Rep.* **7** 15749
[31] Yacoub H, Fahle D, Finken M, Hahn H, Blumberg C, Prost W, Kalisch H, Heuken M and Vescan A 2014 The effect of the inversion channel at the AlN/Si interface on the vertical breakdown characteristics of GaN-based devices *Semicond. Sci. Technol.* **29** 115012
[32] Lederer D and Raskin J-P 2003 Substrate loss mechanisms for microstrip and CPW transmission lines on lossy silicon wafers *Solid-State Electron.* **47** 1927–36
[33] Moram M A and Vickers M E 2009 X-ray diffraction of III-nitrides *Rep. Prog. Phys.* **72** 036502
[34] Matthews J W and Blakeslee A E 1975 Defects in epitaxial multilayers: II. Dislocation pile-ups, threading dislocations, slip lines and cracks *J. Cryst. Growth* **29** 273–80
[35] Garbrecht M, Saha B, Schroeder J L, Hultman L and Sands T D 2017 Dislocation-pipe diffusion in nitride superlattices observed in direct atomic resolution *Sci. Rep.* **7** 46092