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Non-volatile multi-level cell storage via sequential phase transition in Sb₇Te₃/GeSb₆Te multilayer thin film

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Abstract

For high-performance data centers, huge data transfer, reliable data storage and emerging inmemory computing require memory technology with the combination of accelerated access, large capacity and persistence. As for phase-change memory, the Sb-rich compounds Sb_7Te_3 and GeSb₆Te have demonstrated fast switching speed and considerable difference of phase transition temperature. A multilayer structure is built up with the two compounds to reach three nonvolatile resistance states. Sequential phase transition in a relationship with the temperature is confirmed to contribute to different resistance states with sufficient thermal stability. With the verification of nanoscale confinement for the integration of $Sb_7Te_3/GeSb_6Te$ multilayer thin film, T-shape PCM cells are fabricated and two SET operations are executed with 40 ns-width pulses, exhibiting good potential for the multi-level PCM candidate.

Keywords: multi-level cell, phase-change memory, multilayer thin film, non-volatile storage

(Some figures may appear in colour only in the online journal)

1. Introduction

With the growing demand for high-performance cloud computing and large-scale databases, modern data centers are facing challenges of processing huge data transfer between the traditional von-Neumann model-based memory and storage, which may cause unbearable latency for response. As an emerging solution, phase-change memory (PCM) is a promising alternative technology that can break the bottleneck of storage capacity without compromising fast access speed. The prototype PCM utilizes chalcogenide materials with the capability of reversible amorphous-crystalline phase transition to save 1-bit information by identifying the high-resistance state (HRS) and low-resistance state (LRS) of the amorphous and crystalline structures [1]. Moreover, the concept of inmemory computing is recently promoted in favor with PCM devices as an exploration of non-von Neumann architecture [2]. Among the chalcogenides, Ge-Sb-Te ternary system attracts major attention for the development of PCM, and the stoichiometric Ge₂Sb₂Te₅ (GST) alloy derived from GeTe-Sb₂Te₃ pseudo-binary line is the mostly studied chalcogenide materials with considerable optical reflectivity and electrical resistivity contrast upon rapid and reversible phase transition [3, 4]. However, GST suffers from poor thermal stability (85 °C endurance for 10 years), relatively slow SET (HRS to LRS) speed (>100 ns) and high RESET (LRS to HRS) current (>200 μ A), limiting its application for reliable PCM devices [5]. In order to optimize these critical properties, pure GST needs to be modified via material engineering. For example, carbon doping and nitrogen doping of GST have shown good potential for PCM integration with enhanced thermal stability [6, 7]. As for the alloys belonging

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to the Ge-Sb-Te system, Ge-rich orientation targets sufficient thermal endurance for high-temperature storage application, while Sb-rich adjustment enables ultra-fast switching speed to satisfy the requirement of storage-class memory [8–10]. Non-stoichiometric alloys with the balanced reliability and access time are pursued for the alternation of traditional GST.

Increasing the capacity of PCM is another challenging subject towards the consumer market. Since the large range of resistance contrast between HRS and LRS leaves space for intermediate states in PCM, multi-level cell (MLC) is successfully implemented by two methods: (1) Programming current with iterative amplitudes to obtain the partly-amorphous or partly-crystalline states with stable resistance [11, 12]. Although this strategy can reach multiple programmable states in a single compound and realize two or more bits per cell for high density storage, resistance drift and cell variability limit the reliability of the obtained programmable states and the algorism requires further optimization [13]. (2) Sequential phase transition in the multilayer structure. This method is feasible when each layer crystallizes at different temperature and the crystalline resistance can be adjusted by controlling the thickness of active layers. Through the selection of layers with fast crystallization or sustainable thermal stability, three non-volatile resistance states with competitive switching speed have been achieved in the Ge₂Sb₂Te₅/ZnSb [14] and SbSe/ZnSb [15] multilayer thin films. Plus, the superlattice like $GaSb/Sb_4Te$ [16] and Ge₅₀Te₅₀/Ge₈Sb₉₂ [17] structures were also proposed for high-density PCM applications. From the perspective, it is predictable that multi-level storage of the multilayer structure depends on the phase change behavior of each layer.

Materials screening in the Sb-rich area of Ge-Sb-Te system reveals two effective non-stoichiometric candidates Sb₇Te₃ and GeSb₆Te. With the similar growth-dominated crystallization mechanism, both compounds feature ultra-fast switching speed under 30 ns pulse, while the thermal stability and power consumption during memory operations are not compromised with distinct crystallization temperature difference (~170 °C and ~240 °C) [18-20]. A combination of Sb₇Te₃ and GeSb₆Te layers is expected to possess the mentioned advantages simultaneously, while the intermediate state can be optimized by utilizing scaling-down effect. With the investigation of phase-change behavior, structural evolution, physical properties and electrical performance in the PCM cell, $Sb_7Te_3/GeSb_6Te$ multilayer thin film with sequential phase transition during SET process is favorable for reliable MLC storage.

2. Experimental details

Sb₇Te₃/GeSb₆Te multilayer thin films were deposited on the SiO₂/Si(100) substrate by radio frequency magnetron sputtering from GeSb₆Te (99.99%) and Sb₇Te₃ (99.99%) alloy targets. The base pressure was below 2.0×10^{-4} Pa, and the working pressure was adjusted to 0.2 Pa with 30 sccm Ar gas flow. The thickness of each layer was controlled by adjusting

the deposition time and the sputtering power, which was verified by cross-sectional scanning electron micro-scope (SEM).

In situ sheet resistance measurement related to the temperature was performed for Sb₇Te₃/GeSb₆Te film with the total thickness of 50 nm in a Linkam HFS600E-PB2 hot stage. Each sample was heated at the rate ranging from 10 to 40 °C min⁻¹ to trigger phase transition and estimate crystallization activation energy. Isothermal Arrhenius curve was measured for samples held at the specific temperature to evaluate the data retention. For the investigation of phase change behavior, amorphous samples were annealed at 200 °C and 300 °C for 10 min in an Ar atmosphere, respectively. The amorphous and crystalline structures of the as-deposited and annealed films were examined by x-ray diffraction (XRD) and Raman spectra. Transmission electron microscope (TEM) was utilized to execute selected area electron diffraction (SAED) of the different states for micro structure details. The thickness changes and surface roughness of the samples were monitored by x-ray reflection (XRR) and atomic force microscope (AFM). T-shape PCM cells based on Sb₇Te₃/GeSb₆Te multilayer thin films were fabricated by 0.13 μm CMOS technology for the linear current sweep and pulse sweep tests with a Keithley 2400C source meter and a Tektronix AWG5002B arbitrary waveform generator.

3. Result and discussion

The relationship between the sheet resistance of Sb₇Te₃/GeSb₆Te thin film and temperature during the heating process at the rate of 10 $^{\circ}$ C min⁻¹ is shown in figure 1(a). Since GeSb₆Te and Sb₇Te₃ crystallize at different temperatures, a combination of the two layers with the same thickness of 50 nm displays two steps of rapid resistance drop, which reveals the potential of multi-level cell storage for higher capacity. Here, the high-resistance state, intermediate-resistance state and low-resistance state are defined as the '0' state, '1' state and '2' state. While the resistance contrast between the two states may not be distinct enough for read operations in the device, scaling down Sb₇Te₃ layer with lower crystallization temperature (T_c) will help to increase the intermediate resistance and improve the thermal stability of the amorphous state [21]. As the total thickness is maintained at 50 nm, Sb₇Te₃(10 $nm)/GeSb_6Te(40 nm)$ thin film exhibits one to three orders of the magnitude of resistance contrast for each level and slight increase of the first crystallization temperature from 172.3 °C to 187.8 °C (see figure 1(b)), which is favorable for further investigation of the multi-level storage.

Crystallization kinetics of the two-step phase transition can be estimated by the Kissinger method when the heating rate for $Sb_7Te_3(10 \text{ nm})/GeSb_6Te(40 \text{ nm})$ samples varies from 10 to 40 °C min⁻¹. Based on the Kissinger equation:

$$\ln\left(({\rm d}T/{\rm d}t)/T_c^2\right) = E_a/k_BT_c + C, \tag{1}$$



Figure 1. Temperature dependence of sheet resistance for the $Sb_7Te_3/GeSb_6Te$ thin film with different thickness of each layer at the heating rate of 10 °C min⁻¹. (a) each layer was initially controlled by 50 nm and then the thickness was suppressed for optimization. (b) $Sb_7Te_3(10 \text{ nm})/GeSb_6Te(40 \text{ nm})$ film compared with Sb_7Te_3 and $GeSb_6Te$ monolayers. Two kinetic models were utilized to investigate two resistance drops of $Sb_7Te_3(10 \text{ nm})/GeSb_6Te(40 \text{ nm})$ film. (c) Kissinger plots obtained at the heating rate of 10, 20, 30 and 40 °C min⁻¹. (d) Arrhenius plots of failure time with regard to the annealing temperature.

where dT/dt, T_c , k_B represent the heating rate, crystallization temperature and Boltzmann's constant respectively, crystallization activation energy (E_a) can be derived from the slope of the fitting line for Kissinger plots. As shown in figure 1(c), the activation energy of the first transition (E_{a1}) and the second transition (E_{a2}) is 2.16 eV and 2.18 eV respectively, suggesting sufficient amorphous stability against unintentional crystallization. Besides the higher activation energy, non-volatile phase change memory requires maintaining the metastable amorphous state beyond the working temperature for ten more years, which is called the data retention. Figure 1(d) demonstrates the failure time related to the isothermal annealing temperature when the resistance drops to half of its initial value. Assuming the phase transition is similar to the temperature dependence of reaction rates, these plots can be fitted by Arrhenius equation: $t = \tau_0 \exp\left(-E_a/k_BT\right)$, where t is the failure time and τ_0 is a pre-exponential factor for the specific transition. The ten-year data retention for the '0' state is 103 °C and it can reach 183 °C for the '1' state, significantly beyond the requirement for embedded automobile applications (120 °C) [22]. From the sight of thermal stability, $Sb_7Te_3/GeSb_6Te$ multilayer thin film shows superiority over the typical $Ge_2Sb_2Te_5$ thin film and reach the goal of three non-volatile states in phase change memory.

For phase change materials, HRS is commonly attributed to the amorphous structure while LRS suggests the amorphous thin film is partly or fully crystallized. As Sb₇Te₃ and GeSb₆Te are non-stoichiometric Sb-rich compounds, XRD is utilized to examine the phase structural evolution of the multilayer thin film at the speed of 2° \min^{-1} in figure 2(a). A large and wide bump distributed near $2\theta = 29^{\circ}$ is observed in the as-deposited thin film without diffraction peaks, which can be identified as the amorphous state. When the film is annealed at 200 °C to reach the '1' state, the amorphous bump remains the initial range while three diffraction peaks emerge at $2\theta = 40.08^{\circ}$, 42.20° and 46.90° , which match the characteristic of (104) (110) and (015) planes derived from rhombohedral Sb phase [18]. It can be deduced that only Sb_7Te_3 layer crystallizes in the '1' state and GeSb₆Te layer maintains the amorphous structure. The diffraction pattern of the '2' state



Figure 2. Phase structural evolution of $Sb_7Te_3/GeSb_6Te$ multilayer thin film. (a) XRD patterns of the thin film after the deposition, annealed at 200 °C and 300 °C. (b)–(d) are SAED patterns of thin film correspond to the three resistance states. (e) Cross-sectional TEM image of the thin film in the '2' state.

annealed at 300 °C shows a little shift towards higher angle compared with pure rhombohedral Sb phase, and two split peaks at $2\theta = 28.54^{\circ}$ and 28.98° appear instead of the bump, indicating two different crystalline phases are formed. From the Ge-Sb-Te ternary phase diagram determined by Bordas et al [23], GeSb₆Te locates in the threephase area ($\langle Sb \rangle + \delta + \langle Ge \rangle$) close to the Sb-rich position, and Cheng et al [19] confirmed GeSb₆Te crystallized in a rhombohedral structure similar to pure Sb using temperature resolved in situ XRD. Therefore, it is reasonable that the '2' crystalline state is a combination of two different rhombohedral phase with different T_c . Figures 2 (b)-(d) show SAED patterns of the three states. Multiple diffused rings represent the amorphous state in the as-deposited thin film, while the diffraction spots of Sb single crystal and a fuzzy diffused ring coexist in the '1' state. Then amorphous rings disappear and the characteristic of rhombohedral structure is highlighted in the '2' state. The structural evolution deduced from XRD results is valid in the micro structure of Sb₇Te₃/GeSb₆Te multilayer thin film.

To further analyze the structural details of Sb₇Te₃/GeSb₆Te thin film, Raman spectra is performed in the range from 100 to 250 cm⁻¹ for the samples characterized by XRD. As shown in figure 3, the spectrum of amorphous Sb₇Te₃/GeSb₆Te film at ambient temperature is fitted with two Gaussian amplitudes around 138 and 155 cm⁻¹. These can be ascribed to A1 vibration mode of corner-sharing tetrahedral units GeTe_{4-n}Ge_n (n = 3) [24] and the Sb-Te vibrations in the defective octahedral configurations of Sb atoms and SbTe₃ pyramidal units [25]. Partly crystallized thin film annealed at 200 °C demonstrates two individual peaks with higher intensity at 123 and 152 cm⁻¹, apparently distinguished from the amorphous state. The two peaks are assigned to the A1 mode of GeTe_{4-n}Ge_n when n = 2 and the similar Sb-Te vibrations referred above. A blue shift of



Figure 3. Raman spectra of $\text{Sb}_7\text{Te}_3/\text{GeSb}_6\text{Te}$ multilayer thin film processed under the room temperature, 200 °C and 300 °C, respectively. Inset figure shows the spectrum of amorphous thin film and the Gaussian peak fit result.

the Raman peak from 152 to 155 cm⁻¹ is observed in the sample annealed at 300 °C, which would be attributed to the change of internal stress or cluster size upon fully crystallization of two layers [26]. In conclusion, the phase transition mechanism of Sb₇Te₃/GeSb₆Te thin film can be described as follows: amorphous \rightarrow crystalline Sb₇Te₃ and amorphous GeSb₆Te \rightarrow crystalline Sb₇Te₃ and GeSb₆Te.

Before integrated in the PCM cells, the selected $Sb_7Te_3(10 \text{ nm})/GeSb_6Te(40 \text{ nm})$ thin film should satisfy the nanoscale confinement between the two electrodes for SET-RESET operations. The interface between phase change materials and electrodes plays an essential role in the memory cell. Shindo *et al* [27] reported that the total



Figure 4. Measured XRR plots and the fitting curves of (a) amorphous and (b) crystalline $Sb_7Te_3(10 \text{ nm})/GeSb_6Te(40 \text{ nm})$ thin film. (c) and (d) demonstrate the surface morphology of the samples correspond to the two states measured by AFM.

resistance of PCM devices is determined by contact resistance related to the interface. In addition, the thickness and surface roughness of the thin film will vary upon the phase transition due to the inherent strain, lattice mismatch or atomic rearrangement. Voids formed at the electrode interface because of excessive volume change will break the contact and cause memory failure [28]. As refractive index varies in different materials, XRR is implemented to measure the total thickness and surface roughness of amorphous and full crystallized Sb₇Te₃/GeSb₆Te thin film deposited on the Si substrates. As shown in figures 4(a) and (b), the period of oscillation and the intensity decay rate at higher angle are associated with the thin film thickness and roughness respectively. Based on the theoretical calculation model for x-ray reflection of multilayer thin film [29], the obtained XRR plots can be fitted to determine the exact data of the two parameters (see table 1). The variation rate of thickness upon fully crystallization is 3.0%, which is competitive compared with other reported multilayer thin film systems [17, 30] and significantly better than the thickness reduction in GST (6.5%)[31]. This optimized thickness change will avoid stripping the phase change materials off the electrodes when the memory is switching between different states. As regards the surface average roughness, Sb₇Te₃/GeSb₆Te thin film possesses extreme smooth surface before and after crystallization. The surface morphology and root-mean-square (RMS) roughness are also validated by AFM with a height sensor in figures 4(c),

Table 1. The total thickness, average roughness and RMS roughness of amorphous and fully-crystallized $Sb_7Te_3(10 \text{ nm})/GeSb_6Te(40 \text{ nm})$ film.

Film state	Total thickness (nm)	Average roughness (nm)	RMS roughness (nm)
Amorphous	49.6	0.497	0.263
Crystalline	48.1	0.358	0.376

(d). Compared with crystalline GST, $Sb_7Te_3/GeSb_6Te$ with smaller grain size inferred from XRD peaks may contribute to less surface roughness in crystalline state [32]. Smooth surface is able to ensure better contact between the active layers and electrodes, thus improving the reliability of $Sb_7Te_3/GeSb_6Te$ thin film during reversible phase transition for PCM devices.

The experimental PCM cell illustrated in figure 5(a) is then fabricated with $Sb_7Te_3(10 \text{ nm})/GeSb_6Te(40 \text{ nm})$ thin film as the active layer for electrical performance test. For the details, aluminum (~200 nm in thickness) and TiN (~10 nm in thickness) are combined as the top electrodes (TE), while tungsten is used for bottom electrodes (BE, ~190 nm in diameter). Phase change materials (PCMs) is deposited and confined in the cell. Figure 5(b) presents *I–V* characteristic in the linear current sweep test. In PCM, memory switching is represented by threshold switching proposed by Ovshinsky [33]. Generally, in a single switching system, non-linear curve corresponds to the amorphous state due to the semiconductorlike resistance behavior. When the current increases linearly to a critical value, threshold switching happens and the



Figure 5. (a) Schematic diagram of the experimental T-shape PCM cell. (b) I-V and (c) R-V curves of the Sb₇Te₃(10 nm)/GeSb₆Te(40 nm)-based PCM cell. (d) Resistance drift of the three resistance states.

measured voltage will snap back to a smaller value immediately. After the switching, the I-V curve will show linear characteristic related to the crystalline state. In the Sb₇Te₃(10 nm)/GeSb₆Te(40 nm)-based PCM cell, two voltage snapbacks are observed in the current sweep, validating the three resistance states obtained from the temperature-dependent sheet resistance measurement. As shown in figure 5(c), SET-RESET operations are implemented by electric pulses with linear ascending amplitudes. Joule effect of pulses triggers phase transition at certain temperatures. The cell resistance is recorded after each pulse by a 0.1 V bias. The width of pulses reflects access speed of PCM cell, which is critical for the performance of storage-class memory. The switching speed of Sb₇Te₃(10 nm)/GeSb₆Te(40 nm) cell can reach 40 ns with distinct resistance contrast of the three states.

Another factor that extremely affects the accuracy of read operation is resistance drift. Owing to the metastable amorphous phase of phase change materials, the cell resistance of the high-resistance and intermediate-resistance states will experience a slow and time-dependent increment and eventually cause read errors for the preset range. This relationship can be described by the following equation:

$$R(t) = R(t_0)(t/t_0)^{\nu},$$
(2)

where ν is the drift exponent [34]. From the results of time-dependent cell resistance in figure 5(d), resistance drift is suppressed in Sb₇Te₃/GeSb₆Te multilayer thin film, which shows advantages over traditional GST ($\nu = 0.1$ in a-GST) [35]. The accuracy of long-term read operation is ensured for MLC storage.

4. Conclusions

Non-volatile multi-level cell storage is investigated and executed in the Sb₇Te₃/GeSb₆Te multilayer thin film. Different crystallization temperatures and crystalline structures of Sb₇Te₃ and GeSb₆Te provide the possibility of the combination for multi-level cell storage with the adjustment of thin film thickness. Although the two compounds locate in the Sbrich area, the thermal stability of the multilayer thin film is proved to be superior to GST and support long-term data retention in the working temperature. The interface between the phase change materials and electrodes is also taken into consideration to ensure the reliability. The variation of thickness and surface roughness upon the phase transition of Sb₇Te₃/GeSb₆Te thin film is slight enough to satisfy the nanoscale confinement. As a result, Sb₇Te₃/GeSb₆Te-based PCM cell achieves higher storage density with three resistance states and maintains the advantage of fast switching speed possessed by each layer. Since the resistance contrast between the '0' state and '1' state leaves enough space for modification, this PCM cell may also be compatible with the programming strategy to store more bits for encoded information or the exploration of in-memory computing.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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