LETTER TO THE EDITOR

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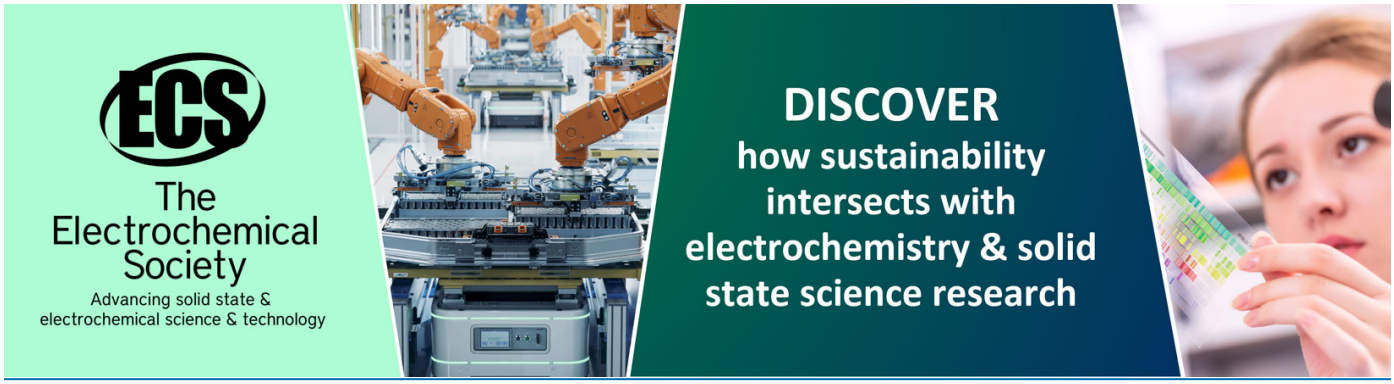

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LETTER TO THE EDITOR

Film thickness constraints for manufacturable strained silicon CMOS

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Abstract
This paper studies the effect of the strained silicon thickness on the characteristics of strained silicon MOSFETs on SiGe virtual substrates. NMOSFETs were fabricated on strained silicon substrates with various strained silicon thicknesses, both above and below the strained silicon critical thickness. The low field electron mobility and subthreshold characteristics of the devices were measured. Low field electron mobility is increased by about 1.8 times on all wafers and is not significantly degraded on any of the samples, even for a strained silicon thickness far greater than the critical thickness. From the subthreshold characteristics, however, it is shown that the off-state leakage current is greatly increased for the devices on the wafers with a strained silicon thickness that exceeds the critical thickness. The mechanism of the leakage was examined by using photon emission microscopy. Strong evidence is shown that the leakage mechanism is source/drain electrical shorting caused by enhanced dopant diffusion near misfit dislocations.

1. Introduction

The strained silicon MOSFET on a SiGe virtual substrate is rapidly emerging as a potential mainstream CMOS technology [1–3]. Early research demonstrated strained silicon MOSFETs with greatly increased carrier mobility relative to unstrained bulk silicon [4–9]. Recently, strained silicon devices have also been proven to be scalable [2] and NMOSFETs with gate lengths down to 25 nm have shown 15–30% performance enhancement over bulk silicon. Strained silicon technology has evolved beyond the research phase and is moving towards production.

To enable successful commercialization, new issues must be studied that were not examined during the early phases of strained silicon technology development. In this paper we present a study of one of these issues: the limitation on the maximum strained silicon film thickness for a manufacturable MOSFET technology. Guidelines for the minimum strained silicon thickness have been reported [6], but the constraints on the maximum film thickness have yet to be defined. Previously published results have demonstrated individual MOSFETs with excellent characteristics fabricated with a wide variety of silicon thicknesses, many of which were greater than the strained silicon critical thickness. However, the effect on a MOSFET of the misfit dislocations that are generated by exceeding the critical thickness has not been thoroughly studied. Many researchers suspect that misfit dislocations may have a harmful effect on MOSFET characteristics [6, 10], but their exact impact has never before been precisely identified nor explained.

In this paper we study strained silicon MOSFETs with silicon thicknesses below and above the critical thickness to understand the strained silicon thickness limitations. We first demonstrate that mobility enhancement is not greatly affected by exceeding the critical thickness. We then show that exceeding the critical thickness does indeed have a deleterious impact on MOSFET behaviour. MOSFETs fabricated on strained silicon films greater than the critical thickness are shown to have dramatically increased levels of off-current. Finally, we propose a mechanism for the

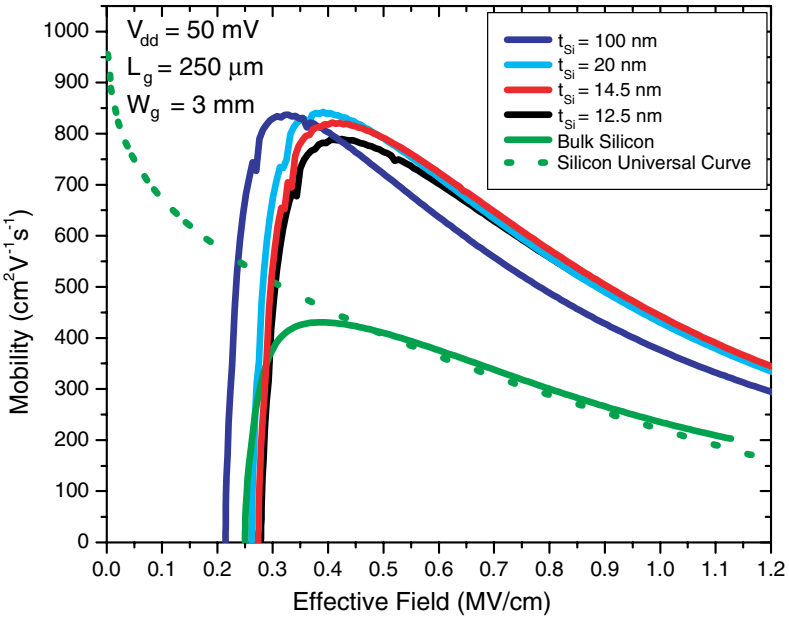

Figure 1. Electron mobility of a bulk silicon MOSFET and of strained silicon MOSFETs with different strained silicon thickness. The strained silicon MOSFETs show enhanced mobility even with silicon films significantly greater than the strained silicon critical thickness.

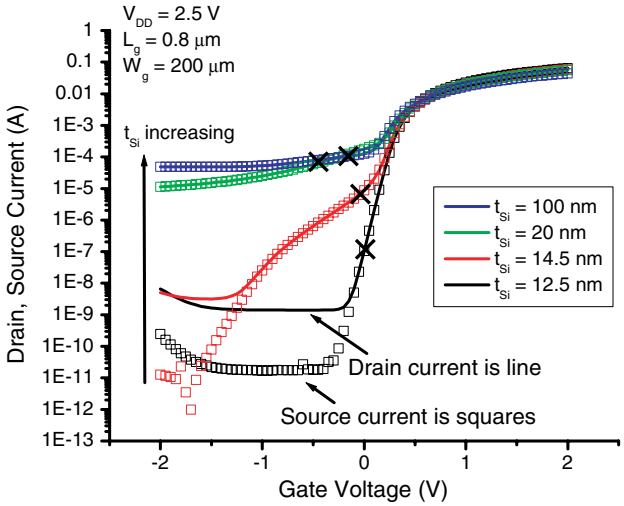

Figure 2. Subthreshold characteristics of strained silicon MOSFETs with a strained silicon thickness above and below the critical thickness. The devices that are above critical thickness (14.5 nm, 20 nm, 100 nm) show greatly increased levels of off-state current leakage, while the device below the critical thickness (12.5 nm) does not. Both the source current and the drain current are shown and they are equal in the elevated leakage regime. Therefore the leakage path is known to extend from the drain to the source, not from the drain to the substrate. The X marks indicate the gate voltage bias point of the PEM pictures in figure 5.

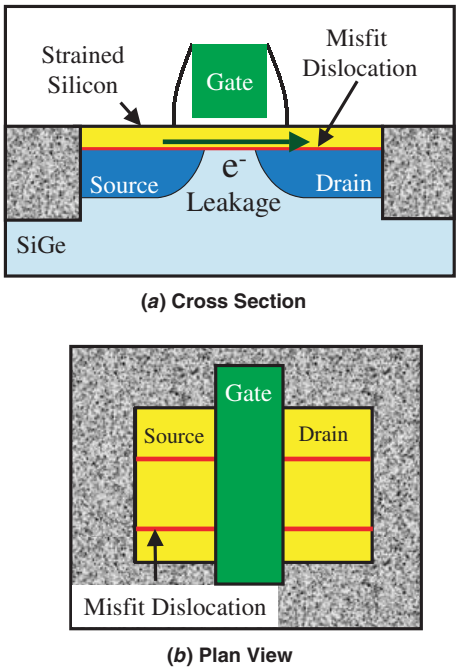

Figure 3. Schematic views of a strained silicon MOSFET showing the drain current leakage mechanism in strained silicon films that contain misfits. Misfit dislocations at the strained silicon/SiGe interface form dislocation pipes and result in highly localized points of current.

off-current increase. Using photon emission microscopy, we present strong evidence that the misfit dislocations at the silicon/SiGe interface that occur in the films over the critical thickness create diffusion pipes that cause source/drain electrical shorts. This work yields a simple yet important conclusion: strained silicon film thickness must be kept below the critical thickness for the films to be suitable for CMOS manufacturing.

2. Description of experiment

Strained silicon NMOSFETs were fabricated on four different wafers with the same SiGe graded buffer construction but with four different strained silicon thicknesses. The SiGe virtual substrates were grown by LPCVD on p-type Si wafers. The SiGe graded layer was grown at a grading rate of 10% Ge μm^{-1} to a final Ge content of 20%, yielding a 2 μm thick graded layer.

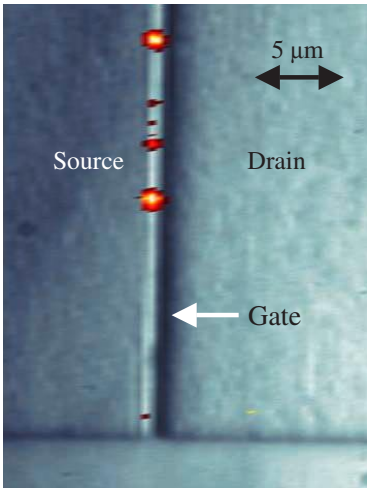

Figure 4. Photon emission microscopy image of light emission from a strained silicon MOSFET. The emission image is superimposed over a reflected light image, showing that the emitted light originates near the gate of the device.

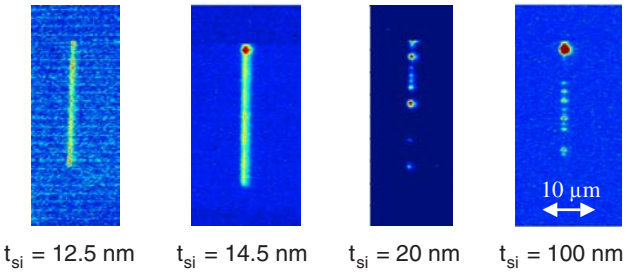

Figure 5. Emitted light images of NMOSFETs on the four different strained silicon wafers. The NMOSFETs are biased in off-state ($V_{ds} = 4.5$ V, $V_{gs} < V_t$) and the exact gate bias voltage is indicated for each device by the X in figure 2. For the $t_{si} = 12.5$ nm (less than t_{crit}), the light emission is dim and is uniform along the channel width. For the other three samples, where $t_{si} > t_{crit}$, leakage current produces light at highly localized points along the channel width. This result strongly supports the hypothesis that misfit dislocation diffusion pipes cause source/drain shorts.

The graded layer was capped with a 2 μm uniform 20% SiGe layer. The SiGe buffer layer growth temperature was 1000 °C. The characteristic crosshatch surface roughness resulting from graded layer growth was removed by chemical mechanical polishing [11]. Subsequently, an additional 1.5 μm layer of uniform 20% SiGe was grown and topped with strained silicon. The strained silicon layer growth temperature was 650 °C. The four different strained silicon thicknesses were 12.5 nm, 14.5 nm, 20 nm and 100 nm. NMOSFETs with gate lengths between 0.5 μm and 200 μm were fabricated on these four substrates and on a bulk silicon monitor wafer. The fabrication process used a single mask level and featured n-type doped polysilicon gates, 5 nm thick thermally grown SiO_2 gate oxide, SiO_2 spacers and titanium salicide source/gate/drain metallization. The significant components of the device fabrication thermal budget were the gate oxide growth (800 °C, 45 min), dopant activation (1000 °C, 1 s), silicide formation anneal (675 °C, 5 min) and sinter (450 °C, 30 min).

The strained silicon thickness values (12.5, 14.5, 20 and 100 nm) were specifically chosen to enable the study of the

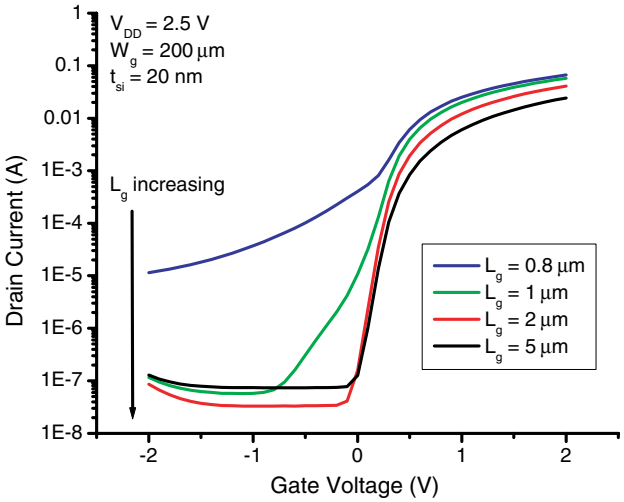

Figure 6. Subthreshold characteristics of strained silicon MOSFETs with $t_{si} = 20$ nm at several different gate lengths. Elevated off-state leakage occurs only for short gate length.

effect of misfit dislocations on the characteristics of strained silicon MOSFETs. The strained silicon critical thickness (t_{crit}) is defined as the maximum strained silicon film thickness for which a dislocation-free silicon film is thermodynamically stable [12]. For a silicon film thickness greater than t_{crit}, misfit dislocation introduction is energetically favourable. For film thicknesses slightly over t_{crit}, misfit dislocations are formed at the Si/SiGe interface via the glide of pre-existing threading dislocations, resulting in small amounts of plastic relaxation of strain in the silicon film. Strained silicon t_{crit} on 20% SiGe is approximately 14 nm. Therefore, the 12.5 nm thick strained silicon film is less than t_{crit}, while the strained silicon on the other three wafers is greater than t_{crit}. Misfit dislocation spacing (which is the average spacing between adjacent misfits) was measured on the different wafers using plan-view TEM. The misfit spacing for the 12.5 nm thickness was infinite (representing the complete absence of misfit dislocations). The misfit spacing in the 14.5, 20 and 100 nm films was approximately 30, 2 and 1 μm, respectively.

3. Results and discussion

The effects of misfit dislocations at the silicon/SiGe interface were studied by comparing the characteristics of NMOSFETs on the four different wafers and the bulk silicon monitor wafer. The devices were characterized using current–voltage measurements, capacitance–voltage measurements and photon emission microscopy.

Low field electron mobility was extracted from large area transistors ($L_g = 250$ μm, $W_g = 3$ mm) on each of the four strained silicon substrates and the silicon monitor wafer using the split-CV technique. Figure 1 shows the low field electron mobility as a function of the vertical effective field. The low field mobility was enhanced by a factor of about 1.8 relative to the bulk silicon monitor wafer for all the samples. This is a somewhat non-intuitive result because the thicker films are partially relaxed due to the misfit dislocation introduction and therefore could be expected to exhibit less electron mobility enhancement. We hypothesize that the relaxation of the

strained silicon films greatly exceeding t_{crit} is incomplete due to dislocation blocking at the strained layer/substrate interface, a well-known effect in strained layer heterosystems. Thus, strain and mobility enhancement are largely maintained even for silicon film thicknesses far greater than t_{crit}. The motivation for maintaining strained silicon film thicknesses below t_{crit} is clearly not the avoidance of the loss of strain and the loss of mobility enhancement, but another important issue described here for the first time.

The subthreshold characteristics of transistors ($L_g = 0.8$ μm, $W_g = 200$ μm) on each of the four strained silicon wafers are compared in figure 2. The devices on the wafer with 12.5 nm of strained silicon show normal behaviour: the drain current falls exponentially with gate voltage for a gate voltage moderately below threshold and then settles to a constant current floor for a gate voltage far below threshold. However, the devices fabricated on wafers with strained silicon thicker than t_{crit} show aberrant behaviour. They suffer from greatly elevated levels of off-current leakage, and the magnitude of the leakage current increases with the thickness of the strained silicon beyond the t_{crit}.

We propose here a hypothesis to explain the mechanism of the elevated leakage current observed in the strained silicon MOSFETs beyond the critical thickness. The proposed explanation can be understood by considering the position of the misfit dislocations in the structure of the MOSFET, as shown in figure 3. The misfit dislocations form at the silicon/SiGe interface and can cross between a MOSFET source and drain. We suggest that these misfit dislocations form dopant diffusion pipes that cause localized source-to-drain shorts, resulting in increased off-current levels.

There are several alternative explanations for the increased off-state leakage current. Misfit dislocations could cause leakage between the drain and the substrate, not between the drain and the source. Or the leakage could occur due to direct conduction along a dislocation, and not involve dopant diffusion in any way. Another possible explanation is that stress effects at the gate edges could cause edge leakage in the devices with films over the critical thickness. However a review of the literature, combined with further experimentation, yielded several pieces of data that strongly suggest that dopant diffusion along misfit dislocations is the correct explanation for the increased leakage.

First, it is well known in the literature that misfit dislocations can greatly increase the diffusivity of dopant species [13]. In particular, it has been shown experimentally that misfit dislocations at the Si/SiGe interface can increase the diffusivity of As (the dopant which here forms the source and drain) by up to six orders of magnitude [14]. Therefore, it is entirely plausible to suggest that dopant diffusivity plays a role in the leakage current phenomena.

Second, simultaneous measurement of the source and drain current shows that the leakage path is from the drain to the source and not from the drain to the substrate. This is shown in figure 2, which includes the drain current (square symbols) and the source current (line). In the elevated leakage regime, the magnitude of the source current equals the magnitude of the drain current. Therefore it is clear that the current flows from the drain to the source.

Third, photon emission microscopy (PEM) was utilized to further illuminate the mechanism responsible for the increased off-current. Using the PEM system (described in [15]), which includes voltage sources, a microscope, a camera and control software, bias was applied to the devices and emitted light was recorded. The results for samples biased in the off-state ($V_{ds} = 4.5$ V, $V_{gs} < V_t$) are shown in figures 4 and 5. Figure 4 shows an emission image superimposed over a reflected light image of a MOSFET. Light is emitted near the gate during device operation because of electron impact ionization and subsequent recombination (light emission was found to actually originate from the drain side of the gate). Figure 5 shows light emission for devices on each of the four strained silicon substrates when the devices are biased in the off-state. The gate bias point for each device is shown as an X in figure 2. For clarity, only the emitted light images (and not the reflected light images) are shown in figure 5. For the sample with a silicon thickness of 12.5 nm, light emission was dim and uniform across the gate width, as expected from a properly operating MOSFET in the subthreshold region. For the sample with a silicon thickness of 14.5 nm, light emission was mostly dim and uniform, but a single bright spot was detected in this field of view. For the samples with a silicon thickness of 20 and 100 nm, the light emission was highly non-uniform. Light emission occurred at discrete points along the channel width. These results indicate that the off-current leakage is highly localized to only specific points in the channel. This result matches the expected behaviour if the misfit dislocations are acting as dopant diffusion pipes: the leakage current, and therefore the light emission, occurs only at the specific points along the channel width where the misfit dislocations have caused a source-to-drain short.

Fourth, the drain leakage current occurs only in MOSFETs with short gate length, as shown in figure 6. This shows the subthreshold leakage for MOSFETs above critical thickness with several different gate lengths. High off-state current leakage occurs for the 0.8 and 1 μm gate length devices above critical thickness. The magnitude of the leakage current decreases with longer gate length. For long enough gate length (2 μm) there is no increased leakage current. This result also matches what is expected if dopant diffusion along misfit dislocations is the mechanism responsible for leakage: leakage only occurs when the gate length is less than approximately the diffusion length of As along the misfit dislocation.

4. Conclusion

This paper addresses the critical question of the maximum thickness limit of the strained silicon film in strained silicon MOSFETs. We demonstrate that strained silicon MOSFETs with silicon films beyond their critical thickness have little loss of mobility enhancement but greatly increased off-state current leakage. We propose that the mechanism responsible for the increased leakage is dopant diffusion along misfit dislocation pipes at the strained silicon/SiGe interface. This hypothesis is strongly supported by substantial experimental evidence. This work demonstrates conclusively that strained silicon thickness must be kept below the critical thickness to permit the fabrication of high-yield, manufacturable strained silicon MOSFETs.

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