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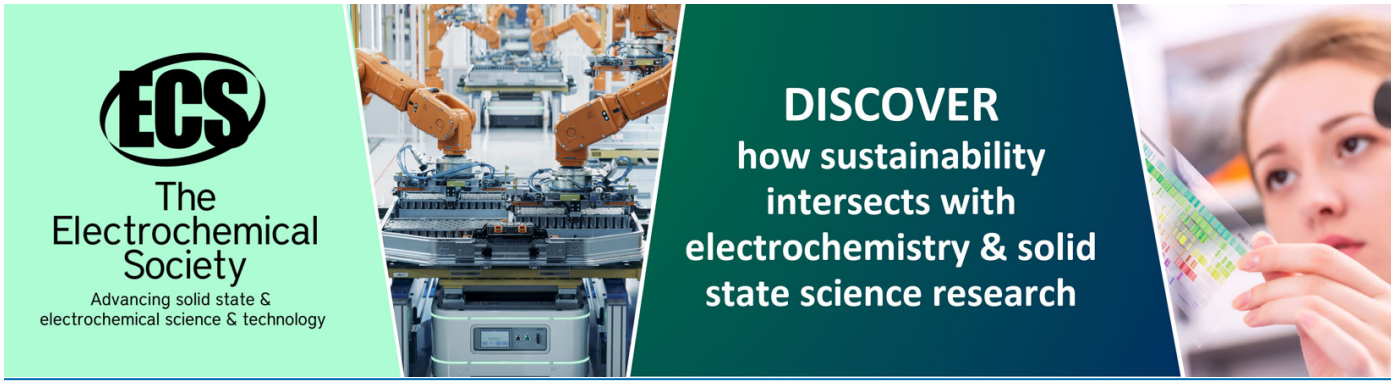

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High performance solution-processed amorphous zinc tin oxide thin film transistor

Seok-Jun Seo[1], **Chaun Gi Choi**[2], **Young Hwan Hwang**[1] and **Byeong-Soo Bae**[1,3]

[1] Department of Materials Science and Engineering, KAIST, Daejeon 305-701 Korea
[2] Corporate R and D Center, Samsung SDI Co., Ltd., 428-5, Yongin-si, Gyeonggi-do 449-902 Korea

E-mail: bsbae@kaist.ac.kr

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Abstract
Thin film transistors (TFTs) with amorphous zinc tin oxide (ZTO) channel layer were fabricated by a simple and low-cost solution process. The ZTO thin films are highly transparent (>90% transmittance) in the visible region. The ZTO TFTs fabricated at 400 and 500 °C are operated in enhancement mode. The TFT annealed at 500 °C shows a mobility of 14.11 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage of 1.71 V, a subthreshold slope of 0.4 V dec^{-1} and an on–off current ratio greater than 10^8. In addition, we investigated the gate bias stability of the TFT. Positive gate bias results in a positive shift of the threshold voltage due to the charge trapping in the channel/dielectric interface.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Metal oxide materials have been widely investigated for passive devices such as capacitors, dielectrics and transparent conducting oxides (TCOs). In particular, TCOs such as zinc oxide (ZnO) and tin oxide (SnO_2) have been studied significantly due to their wide applications in displays, solar cells and electrochromatic windows [1–3]. Recently, transparent oxide semiconductors (TOSs) have attracted a great deal of attention as the active layer in transparent thin film transistors (TTFTs) [4–8]. Amorphous silicon based thin film transistors (TFTs), the most dominant backplane devices in displays, have been well optimized concerning uniformity and fabrication process; however, they exhibit low mobilities of less than 1 $cm^2\ V^{-1}\ s^{-1}$. TOSs are very attractive in displays compared with amorphous silicon due to their high mobility sufficient to drive active matrix organic light emitting diodes (AMOLEDs), good environmental stability, low cost and high transparency for backplanes with large aperture ratio.

Among TOSs, amorphous oxides based on heavy metal oxides with the $(n-1)d^{10}ns^0 (n \geqslant 4)$ electronic configuration are promising candidates for high performance TTFT channel materials [9, 10]. Zinc based amorphous oxides such as indium gallium zinc oxide (IGZO) [11–14], zinc tin oxide (ZTO) [15–20] and indium zinc oxide (IZO) [21, 22] have been reported for the TTFT channel layer. These amorphous oxide TFTs were fabricated on various substrates, including silicon, glass and flexible polymers, and showed high mobilities up to 40 $cm^2\ V^{-1}\ s^{-1}$. In particular, ZTO thin films have been used for TTFTs with good transistor characteristics [15] and flexible field-effect transistors (FETs) [16]. The ZTO TFTs exhibited mobilities and on–off current ratios in the range of 5–20 $cm^2\ V^{-1}\ s^{-1}$ and 10^6–10^7, respectively. However, most amorphous oxides have been prepared by vacuum processes such as rf magnetron sputtering and pulse laser deposition, which require expensive equipment and result in high fabrication costs.

The solution process is an alternative thin film deposition method which is a simple and low-cost pathway and enables large area coating and high throughput. Moreover, direct patterning is available through ink-jet printing, imprinting and screen printing without the complex photolithography process. Recently, ZTO and IZO based TFTs [23–25] have been fabricated by the solution process. The results showed a high mobility of 16 $cm^2\ V^{-1}\ s^{-1}$ and ink-jet printability.

[3] Author to whom any correspondence should be addressed.

However, most solution-processed TFTs had high off current and a low on–off current ratio of 10^6 compared with the typical vacuum-processed TFTs, which reduce the effective switching property.

For application of practical devices, the bias stress effect of TFTs is required. In the case of amorphous silicon, poly silicon and organic TFTs, there are several reports about the bias stress. Though many groups have studied TOSs based TFTs, only few papers about the bias stress stability have been reported [20, 26, 27]. In particular, in the case of the solution-processed TOS TFTs, the bias stress effect is not reported yet.

This paper reports a simple and low-cost process to fabricate the highly transparent ZTO thin films under ambient condition and the performances of TFTs using a ZTO active channel layer. By a solution process using zinc and tin precursors in solvent which are capable of forming uniform and continuous thin films through spin-coating, TFTs with an amorphous ZTO thin film semiconductor were obtained. The ZTO TFT showed competitive performances, high saturation mobility and high on–off current ratio, compared with the previously reported ZTO TFTs using the vacuum process [15, 16]. In addition, the gate bias stress stability of the solution-processed ZTO TFT was investigated.

2. Experimental procedures

Metal precursor solution for fabricating ZTO thin films was prepared by dissolving 0.3M zinc acetate ($Zn(CH_3COO)_2$, Aldrich) and 0.3M tin chloride ($SnCl_2$, Aldrich) in 2-methoxyethanol separately. In order to make the solution stable, the precursors were chelated with acetylacetone ($CH_3COCH_2COCH_3$, Aldrich) with an equivalent molar ratio. Then two solutions were mixed and stirred for 6 h at room temperature. The resulting solution was filtered through a 0.22 μm syringe filter (PTFE, GE) and then deposited on the substrate by the spin-coating method at 5000 rpm for 30 s.

Heavily boron(p+) doped silicon wafers were used in the bottom gate/top contact structure for the fabrication of ZTO TFTs. The SiO_2 layer with a thickness of 100 nm was thermally grown on top of the silicon wafer as the gate dielectric. After ZTO film deposition, heat treatment was conducted at 400 and 500 °C for 1 h in ambient air. The source and drain electrodes were deposited on the ZTO layer through a shadow mask, using aluminium. The channel length was 120 μm and the channel width was 1000 μm. The TFT devices were analysed with an HP 4145B semiconductor parameter analyzer at room temperature in a dark room.

In order to observe thermal decomposition behaviour, thermogravimetric analysis ((TGA), TA instrument Q50) measurements were performed under air atmosphere at a heating rate of 5 °C min^{-1}. The thickness of the ZTO thin film was measured by scanning electron microscopy ((SEM), Philips XL30). The phase and crystalline orientation of the films were determined by x-ray diffraction ((XRD), Rigaku D/MAX-RC diffractometer with Cu Kα radiation) using a fixed glancing incidence angle (2°). The optical transmittance of the ZTO film was measured using an ultraviolet–visible–near infrared (UV–vis–NIR) spectrophotometer (Shimadzu UV3101PC) at various wavelengths.

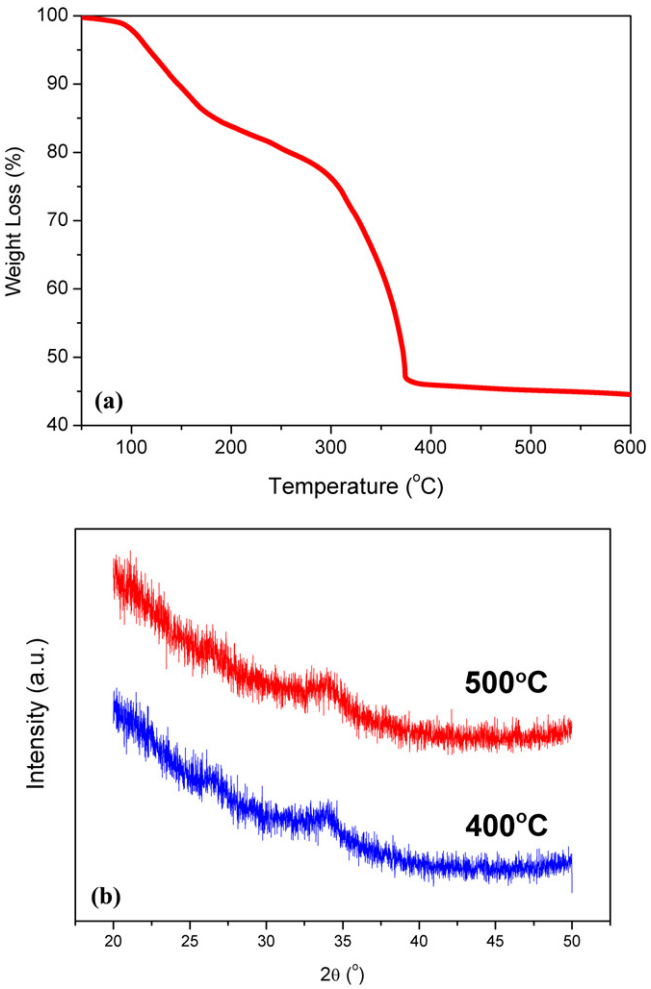

Figure 1. (*a*) TGA of the ZTO precursor solution at 5 °C min^{-1} heating rate in air and (*b*) the XRD pattern obtained from the ZTO thin film annealed at 400 and 500 °C for 1 h in air.

3. Results and discussion

The resultant TGA curve of the ZTO solution, dried at 130 °C to remove the solvent, is shown in figure 1(*a*). An initial weight loss below 150 °C represents the evaporation of the residual solvent (i.e. 2-methoxyethanol). The next weight loss up to 300 °C indicates the decomposition of zinc acetate. The abrupt weight loss around 300–350 °C is attributed to the decomposition of tin chloride, and the thermal decomposition is completed at ∼400 °C. These results suggest that a heat treatment temperature of 400–500 °C would be sufficient for the formation of the ZTO thin film. Figure 1(*b*) shows the XRD patterns of the spin-coated ZTO thin films annealed at 400 and 500 °C for 1 h in air. In both cases, the XRD patterns exhibit a broad and small peak at $2\theta = 34°$, which is characteristic of the amorphous ZTO films previously reported in the literature [15].

A schematic structure and a SEM image of the ZTO TFT are shown in figure 2. The cross-sectional SEM image shows a 20 nm uniform ZTO thin film deposited on a SiO_2/Si substrate by spin-coating and annealing at 500 °C.

Figure 3 shows the transmission spectrum of the ZTO thin film deposited on the quartz substrate. The ZTO thin film is highly transparent with 90% in the visible range (400–750 nm).

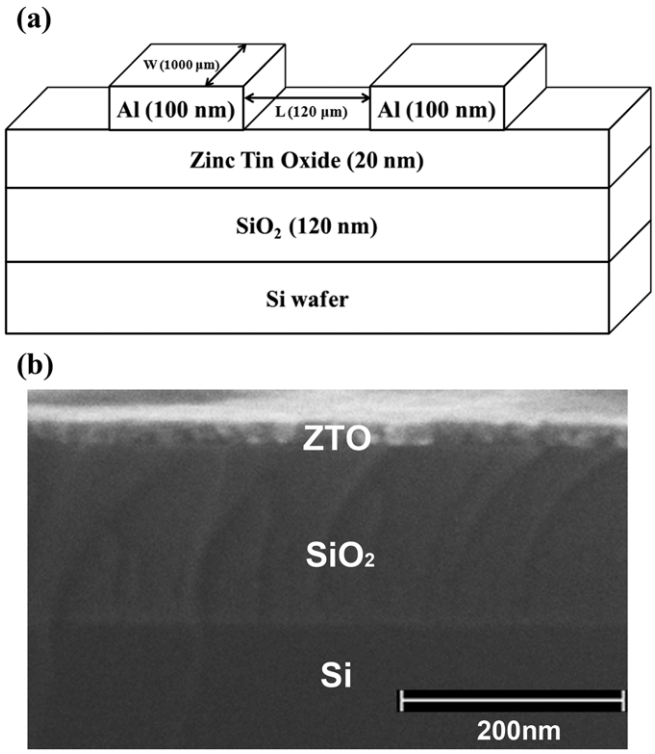

Figure 2. (*a*) Schematic cross-sectional view of the ZTO TFT structure (channel length = 120 μm; channel width = 1000 μm) and (*b*) tilted cross-sectional SEM images of the ZTO TFT.

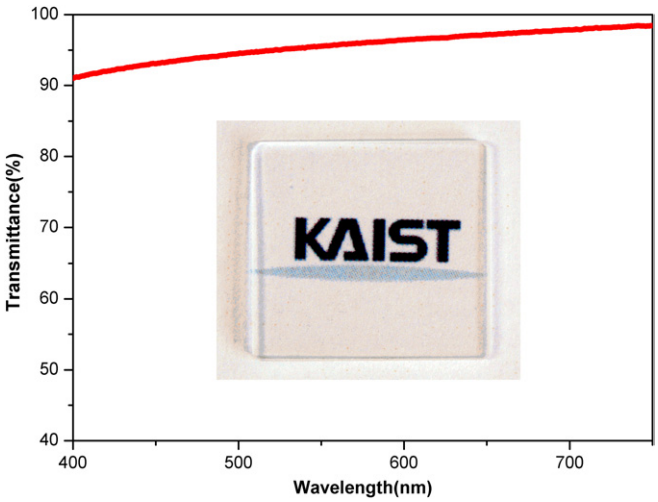

Figure 3. UV–vis transmittance spectrum and optical image (inset) of the ZTO thin film on a quartz substrate.

The optical image in the inset of figure 3 also confirmed the transparency of the film.

Figure 4(*a*) shows the drain current versus drain-to-source voltage ($I_D - V_{DS}$) output characteristics of the ZTO TFT annealed at 500 °C at various gate voltages (V_G); the results show the n-type transistor behaviour with hard saturation.

Figure 4(*b*) shows the transfer characteristics of I_D versus V_G at V_{DS} = 40 V for the ZTO TFTs annealed at 400 and 500 °C. The electrical parameters including the saturation mobility and the threshold voltage were derived from a linear fitting to the plot of the square root of I_D versus V_G using the

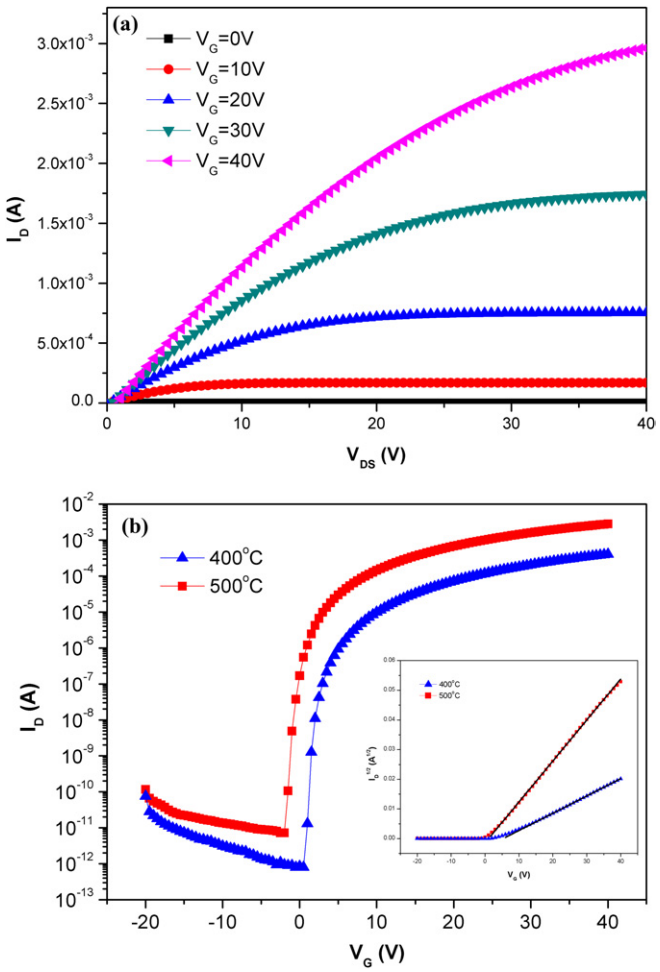

Figure 4. (*a*) Drain current versus drain-to-source voltage ($I_D - V_{DS}$) output characteristics of the ZTO TFT annealed at 500 °C and (*b*) drain current versus gate voltage ($I_D - V_G$) and the square root of the drain current versus gate voltage ($I_D^{1/2} - V_G$, inset) transfer characteristics of the ZTO TFT annealed at 400 °C and 500 °C with V_{DS} = 40 V.

following equation [29] of the saturation region:

$$I_D = \frac{WC_i}{2L}\mu_{SAT}(V_G - V_{th})^2, \quad (1)$$

where W and L are the channel width and the length, respectively, μ_{SAT} is the saturation mobility, C_i is the capacitance per unit area of the SiO_2 gate insulator (dielectric constant ~3.9) and V_{th} is the threshold voltage. The ZTO TFT annealed at 400 °C exhibits the saturation mobility of 2.49 cm^2 V^{-1} s^{-1} and the threshold voltage of 5.93 V and the TFT annealed at 500 °C shows high performance, the saturation mobility of 14.11 cm^2 V^{-1} s^{-1} and the threshold voltage of 1.71 V, which is competitive with vacuum-processed ZTO TFTs annealed at low temperatures [15, 16]. These parameters that indicate the ZTO TFTs are operated in enhancement mode on a positive gate bias. In order to investigate the effects of the annealing temperature, other electrical parameters and atomic contents were obtained by Hall measurements and Auger electron spectroscopy (AES) respectively (table 1). The ZTO film annealed at 500 °C

Table 1. Electrical parameters and AES atomic ratios for the ZTO films annealed at 400 °C and 500 °C.

Annealing temperature (°C)	Carrier density (cm^{-3})	Resistivity (Ω cm)	Hall mobility ($cm^2 V^{-1} s^{-1}$)	Saturation mobility ($cm^2 V^{-1} s^{-1}$)	Threshold voltage (V)	I_{on}/I_{off}	Subthreshold slope ($V dec^{-1}$)	Sn/Zn/O
400	1.71×10^{16}	4.99×10^{2}	7.32	2.49	5.93	5.08×10^{8}	0.40	1.90/1/2.92
500	5.65×10^{16}	7.04	15.70	14.11	1.71	3.86×10^{8}	0.40	2.02/1/3.13

exhibits a higher carrier density, a lower resistivity and a higher Hall mobility with a higher Sn/Zn ratio. Therefore, the increase in the carrier density and the mobility could be due to an enrichment of Sn in the ZTO film. On the other hand, the devices annealed at 400 and 500 °C exhibit indistinguishable XRD patterns; thus it is reasonable to assume that the high mobility of the TFT annealed at 500 °C could also result from the modification of the semiconductor/dielectric interface, improved local atomic rearrangement [15] or decrease in the gap state and/or the tail state near the conduction band minimum at high temperature. Despite the lower mobility of the ZTO TFT annealed at 400 °C than the values of the vacuum-deposited ones, the mobility of 1–10 cm^2 V^{-1} s^{-1} seems to be sufficient to fulfil the brightness and resolution requirements of AMOLEDs; thus, the solution-processed ZTO TFT fabricated at 400 °C can be applicable to the backplane of the AMOLED [28]. Additionally, the turn-on voltage (V_{on}) [29], which is the gate voltage at the onset of the initial sharp increase in current in transfer characteristics, is equal to 0.5 and −1 V for the ZTO TFTs. The turn-on voltage directly characterizes the gate voltage required to fully 'turn off' the transistor in a switching application. Since the ZTO TFT annealed at 400 °C is normally off, the circuit design can be simpler and the power dissipation can be lower.

The on–off current ratios are higher than 10^8 with the low off current of $<10^{-11}$ A, which is a superior property compared with those of the usual solution-processed amorphous oxide TFTs ($\sim 10^6$) [23, 24] and is similar to those of the vacuum-processed amorphous oxide TFTs ($\sim 10^8$) [12, 21]. These low off currents could result from the thin thickness and the amorphous phase of the ZTO film. In addition, the AES data indicate the presence of only 0.5 at% chlorine in both samples; thus, a few mobile ions in the ZTO thin films can also reduce the off current. The ZTO TFTs exhibit good subthreshold slopes, S, defined as the voltage required to increase the drain current by a factor of 10, of 0.4 V dec^{-1}, which is quite small relatively to other solution-processed TFTs [23, 24] and even vacuum-processed TFTs [15, 19, 20]. The small S is attributed to a small number of the interface traps [30] in the amorphous ZTO thin film, which does not include the grain boundary. These high on–off current ratios and small subthreshold slope are suitable for switching devices in active matrix flat panel displays. Moreover, since the solution process has the advantage of simplicity and low cost, the solution-processed ZTO TFT can be applied for backplane devices of displays instead of the vacuum-processed amorphous oxide TFTs.

To investigate the gate bias stability, the device fabricated at 500 °C was stressed at $V_G = 20$ V for 3600 s. Figure 5(a) shows the plot of the square root of drain current versus gate voltage of the solution-processed ZTO TFT before and after a gate bias stress. Since both curves have almost the same slope in the linear region, the saturation mobility does not change after the gate bias stress. The threshold voltage, on the other hand, is positively shifted ($\Delta V_{th} = 5.82$ V) due to the trapped negative charge at the semiconductor/dielectric interface. The trapped charge screens the gate voltage; therefore, the threshold voltage increases after the gate bias stress. Figure 5(b) shows the transfer curves of the TFT. After the gate bias stress, the off current decreases. The negative mobile charge trapping under the gate bias induces the low off current. The subthreshold slope before and after the gate bias stress is similar ($S \sim 0.4$), which indicates that no extra electron states are created at the semiconductor/dielectric

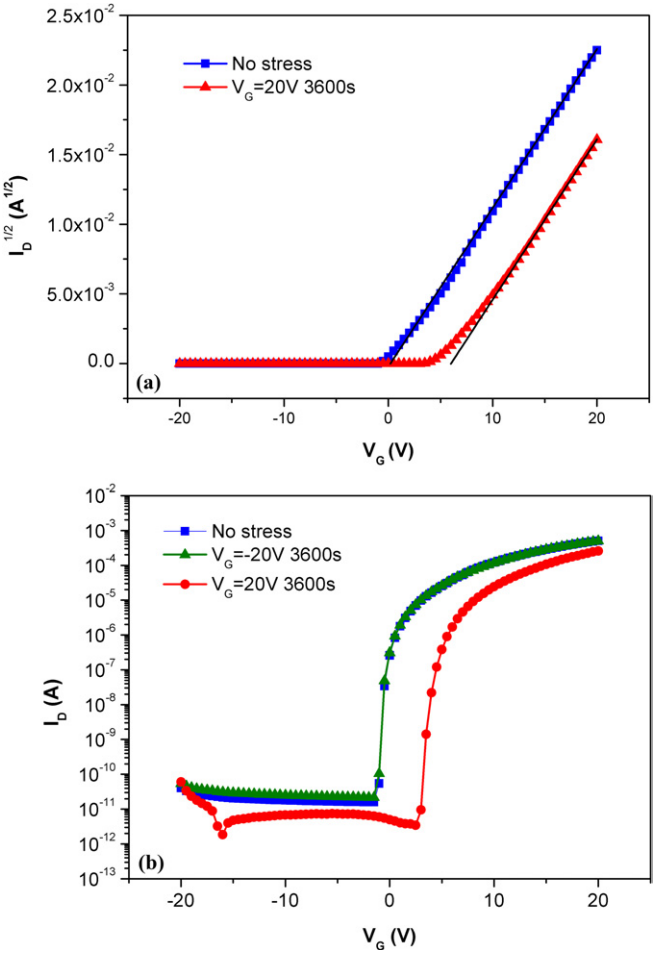

Figure 5. (a) Square root of the drain current versus gate voltage ($I_D^{1/2} - V_G$) before and after gate bias stress at $V_G = 20$ V for 3600 s and (b) the drain current versus gate voltage ($I_D - V_G$) transfer characteristics under positive and negative gate bias stress for 3600 s with $V_{DS} = 20$ V.

interface [31]. For further investigation of the gate bias stress effect, we compared positive and negative bias stresses. Figure 5(*b*) shows the change in the transfer curve after negative or positive bias stress. Compared with the positive bias stress, the negative bias stress induces a very small change in the threshold voltage and the drain current. This means, under negative bias stress, electrons are depleted at the semiconductor/dielectric interface; thus, there are no mobile charges for charge trapping [27].

4. Conclusions

In summary, the ZTO thin films were fabricated by a simple and low-cost precursor solution process through spin-coating. The films were annealed at 400 and 500 °C and exhibit high transparency and an amorphous phase. The TFTs are operated in enhancement mode and the device fabricated at 500 °C has a saturation mobility of 14.11 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage of 1.71 V, an on–off current ratio higher than 10^8 and a subthreshold slope of 0.4 dec^{-1}, which are applicable for high performance backplane of displays. Additionally, under the positive gate bias stress, the threshold voltage is shifted to the positive direction due to charge trapping in the semiconductor/dielectric interface.

Acknowledgments

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