Soft/write-error-resilient CMOS/magnetic tunnel junction nonvolatile flip-flop based on majority-decision shared writing

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Soft/write-error-resilient CMOS/magnetic tunnel junction nonvolatile flip-flop based on majority-decision shared writing

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A soft/write-error-resilient nonvolatile flip-flop (NVFF) using three-terminal magnetic tunnel junctions (MTJs) is presented. The proposed NVFF exploits a redundant structure with a majority bit implicitly stored, which is tolerant to soft errors including both single-event transients (SETs) and single-event upsets (SEUs). For write-error resilience, all the bits of the redundant MTJs are written using the majority bit with a shared write-current path, exhibiting 1-bit soft-error correction and 1-bit write-error masking. In addition, the shared writing scheme reduces the number of write-current paths to one-third of that with a redundant NVFF with 1-bit soft/write-error masking. Using 65 nm CMOS/MTJ technologies, the proposed NVFF achieves a few orders-of-magnitude reduction in the failure in time (FIT), a 31% reduction in the transistor count, and a 65% reduction in the write energy in comparison with the redundant NVFF. © 2017 The Japan Society of Applied Physics

1. Introduction

Magnetic tunnel junctions (MTJs)1–4 integrated with MOS transistors are promising storage elements for ultralow-power applications, such as nonvolatile flip-flops (NVFFs),5 MRAMs,6 MCUs,7 and search-engine systems.8 However, there are two critical issues: write errors and soft errors in CMOS/MTJ hybrid integrated circuits. Regarding write errors, data bits might be incorrectly written to MTJ devices due to the probabilistic switching behavior of MTJ devices.9–13) Regarding soft errors, the MTJ device itself is robust against soft errors14,15) due to alpha particle and neutron strikes, whereas these strikes induce single-event transients (SETs) and single-event upsets (SEUs) in MOS transistors.16,17) As a result, data bits flipped by a SET or SEU in MOS transistors are written to MTJ devices, causing soft errors in CMOS/MTJ circuits. Recently, only the issues of SEUs have been addressed for CMOS/MTJ hybrid integrated circuits.18,19)

In this paper, both write- and soft-error issues including SETs and SEUs are addressed by our proposed majority-decision shared-writing scheme for CMOS/MTJ-based NVFFs.

2. Soft error and write error in CMOS/MTJ-based NVFFs

2.1 CMOS/MTJ-based NVFFs

Figure 1 shows a three-terminal MTJ device that can be mainly implemented on the basis of domain-wall motion (DWM) devices and spin–orbit-torque devices.2,4) In the three-terminal device, read and write paths are separated as shown in Fig. 1(a), leading to no read disturb errors, in contrast to two-terminal MTJ devices.1,3) The read resistance of the MTJ device, \( R_{\text{MTJ}} \), is one of two values: \( R_L \) or \( R_H \), where the symbol is shown in Fig. 1(b).

\[ \begin{align*}
R_L &= 5 \, \text{k}\Omega \\
R_H &= 10 \, \text{k}\Omega 
\end{align*} \]

In the three-terminal device, \( I_w \) is switched by \( R_{\text{MTJ}} \), as shown in Fig. 1(c). A conventional CMOS/MTJ-based NVFF is illustrated in Fig. 2. It includes a CMOS-based master latch and a CMOS/MTJ-based slave latch. There are three operation modes: normal, backup, and restore. In the normal mode, the NVFF operates as a CMOS-based flip-flop with \( WCK = \text{low} \). It stores a data bit to \((C, Cb)\) using a cross-coupled keeper. In the backup mode, \( WCK \) is high to write a data bit \((D)\) to the two MTJs using a current signal. For example, when \( D \) is
“0”, the write current signal is generated from the right to left of the figure, changing (R, Rb) to (Rl, Rh). After the backup operation, the supply voltage is low for power gating. In the restore mode after the supply voltage is recovered, PON is low to maintain C andCb at the same voltage level and then is high to decide the voltage levels, which depend on (R, Rb).

2.2 Soft errors in NVFFs

There are four categories of soft error in CMOS/MTJ-based NVFFs: MTJ-direct, MTJ-indirect, CMOS-direct, and CMOS-indirect as shown in Fig. 3. In the MTJ-direct effect, the resistance state of MTJ devices might be flipped by direct particle strikes, causing soft errors. The error probabilities of MTJ devices due to direct particle strikes were previously measured and showed zero error probability.14 Hence, the MTJ device itself is reasonably robust against particle strikes. In the MTJ-indirect effect, peripheral transistors around an MTJ device are affected by particle strikes, generating current pulse signals, called SET signals. The SET signals might switch the resistance state of the MTJ device because MTJ devices exhibit probabilistic switching behaviors.9–13 The switching probabilities are negligibly small in the case of a certain critical current (e.g., 50 μA) according to device simulations.15

The other two categories are CMOS-related. In the CMOS-direct effect, a data bit stored in the CMOS cross-coupled keeper of the NVFF might be flipped by particle strikes.16,17 The CMOS-direct effect is called a SEU. In CMOS/MTJ-based NVFFs, the flipped data is written to MTJ devices, causing soft errors. SEU issues have been addressed for CMOS-based memory circuits.20–22 In the CMOS-indirect effect, SET signals are generated in logic gates and then propagate to NVFFs, which might flip a data bit stored in the CMOS cross-coupled keeper of the NVFF. The flipped data causes soft errors as well as the CMOS-direct effect. The CMOS-indirect effect has been addressed for CMOS-based flip-flops.23–25 However, these CMOS-related issues have not been addressed for CMOS/MTJ-based NVFFs.

2.3 Write errors in NVFFs

The write errors in CMOS/MTJ-based NVFFs are described in this subsection. MTJ devices are essentially probabilistic switching devices, as shown in Fig. 4. When a data bit is written to an MTJ device, a current signal is generated, which changes the resistance state of the MTJ device. The switching probability, \( p_w \), basically depends on the write current and write time. For memory circuits, a current signal is generated for a long period (e.g., 40 ns) to write data correctly, causing a large write energy. In contrast, the probabilistic switching behavior can be used for other applications, such as random number generators and analog-to-stochastic converters.26–29

In the CMOS/MTJ-based NVFF shown in Fig. 2, two MTJ devices are used to store 1-bit data. As the two MTJ devices must be correctly written to store data, the write-error rate (WER) of the NVFF is defined as

\[
\text{WER} = 1 - p_w^2.
\]

The WER and SER are considered for soft/write-error-resilient NVFFs.

2.4 Restore-error rate in NVFFs

CMOS/MTJ-based nonvolatile processors are often power-gated to reduce the leakage current when they are in the idle state.7 Before power gating, data bits are written to MTJ devices in CMOS/MTJ-based NVFFs as a backup operation. After the supply voltage is recovered, the data bits are restored by reading the MTJ devices as the restore operation. If data bits are not correctly restored due to soft errors and/or write errors, the nonvolatile processors cannot continue the operation and hence their initialization is required.30

Let us define the restore-error rate (RER) of a conventional CMOS/MTJ-based NVFF. As a conventional NVFF is not tolerant to both soft and write errors, it can correctly restore data bits unless both soft and write errors occur. Hence, the RER is defined as

\[
\text{RER}_{\text{conv}} = 1 - (1 - \text{SER}) \cdot (1 - \text{WER}),
\]

where SER stands for the soft-error rate.

3. Majority-decision shared-writing scheme for soft/write-error resilient nonvolatile flip-flops

3.1 Baseline design

To reduce the RER of the NVFFs, a soft/write-error tolerant CMOS/MTJ-based NVFF is first designed that is based on a soft-error tolerant CMOS flip-flop. There are several candidate soft-error-tolerant CMOS flip-flops.23–25 A soft-error-tolerant CMOS flip-flop based on a dual redundant structure25 is selected in this paper. The master/salve part exploits two latches with a delay element and a C-element that changes the output state (Q) if the input states (S0 and S1) are the same, and remains the previous state otherwise. If S0 or S1 is affected by a SET or SEU, the majority bit (Q) is stable. Hence, the original soft-error tolerant CMOS flip-flops exhibit 1-bit soft-error masking.
The original design uses only MOS transistors, but an NVFF in which the slave part is replaced by CMOS/MTJ-based storage elements is designed as the baseline NVFF as shown in Fig. 5, in this study. The slave part contains two CMOS/MTJ-based latches and a CMOS/MTJ C-element. As each block includes two MTJs to store 1-bit data, there are six MTJs in total. The baseline design also exhibits 1-bit soft-error masking, but there are two issues. The first one is a high write energy due to three independent write-current paths as opposed to one write-current path in the conventional NVFF. The second one is that an incorrect bit flipped by a SET or SEU is written to MTJ devices.

Let us define the RER of the baseline NVFF. In the baseline NVFF, three redundant bits are written to MTJ devices: two for the CMOS/MTJ latches and one for the CMOS/MTJ C-element. The RER is defined by considering two scenarios: no soft error and a 1-bit soft-error. If there is no soft error, a 1-bit write error is masked because three redundant bits are used. Suppose that $S_0 = 1$, $S_1 = 1$, and $Q = 0$ are written, where $S_0$ is affected by soft errors. In this case, the two correct bits ($S_1$ and $Q$) must be correctly written to the MTJ devices in order to maintain $Q = 0$ after restoring. This means that there is no 1-bit write-error masking capability if there is a soft error.

As the two scenarios described are considered, the RER of the baseline design is defined as

$$
\text{RER}_{\text{base}} = 1 - (1 - \text{SER}) \cdot [(1 - \text{WER})^3 + 3 \cdot (1 - \text{WER})^2 \cdot \text{WER} - \text{SER} \cdot [(1 - \text{WER})^3 + (1 - \text{WER})^2 \cdot \text{WER}],
$$

As a result, the baseline design exhibits 1-bit soft-error masking and 1-bit write-error masking unless a soft error occurs.

### 3.2 Proposed design

To address the two issues of the baseline design, the majority-decision shared writing is proposed as shown in Fig. 6. Unlike the baseline design, all the data bits in the two latches and the C-element are written to MTJ devices using the majority bit ($Q$) stored in the C-element. This prevents us for writing an incorrect bit flipped by a SET or SEU. Hence,
a 1-bit write error is masked using the three redundant bits regardless of whether a soft error occurs or not. The RER of the proposed NVFF is defined as

$$\text{RER}_{\text{prop}} = 1 - ((1 - \text{WER})^3 + 3 \cdot (1 - \text{WER})^2 \cdot \text{WER}).$$ (4)

As a result, the proposed design exhibits 1-bit soft-error correction and 1-bit write-error masking. The difference between Eqs. (3) and (4) is whether SER is included or not.

In addition, all the MTJ devices are written using the shared write-current path owing to the low write resistance of three-terminal devices. The shared write-current path reduces the number of write-current paths and write drivers from three in the baseline design to one, leading to a smaller write energy and area.

4. Evaluation

4.1 Simulated circuit verification

The proposed and baseline NVFFs are designed using 65 nm CMOS/MTJ technologies and simulated using NS-SPICE. For the MTJ parameters, \( R_L = 5 \, \text{k}\Omega \), \( R_H = 10 \, \text{k}\Omega \), a write resistance of 75\,\Omega, and a critical current of 100\,\mu A are used. The MTJ model presented in Ref. 31 is used and can be simulated with MOS transistors using NS-SPICE, where the MTJ model was created on the basis of fabricated three-terminal DWM MTJ devices. The write current for each MTJ device is approximately set to the same value of 200\,\mu A. Figure 7 shows simulated waveforms of the proposed flip-flop with a SET pulse signal on XD. The SET signal is captured by a latch, storing \( S_0 = 1 \), but is not captured by another latch owing to the delay element. Hence, the output bit \( Q \) is stable. Figure 8 shows write and restore operations with a flipped bit of \( S_0 \) due to a SET. When data bits are written to the MTJ devices, the majority bit corrects the flipped bit and hence correctly writes the bit. After the power gating, the correct bit is restored as demonstrated in the simulation.

4.2 Comparisons of RER

Table I shows a summary of the features of the CMOS/MTJ-based NVFFs. The conventional NVFF is a regular flip-flop that is not tolerant to both soft and write errors. The baseline NVFF exploits three redundant bits that exhibit 1-bit soft-error masking and 1-bit write-error masking unless a soft error occurs. The redundancy increases the number of write-current paths and write energy. The proposed majority-based shared writing remains the number of write-current paths 1 and hence correctly writes the bit. After the power gating, the correct bit is restored as demonstrated in the simulation.

<table>
<thead>
<tr>
<th>Number of MTJs</th>
<th>Conventional</th>
<th>Baseline</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of write-current paths</td>
<td>2</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Soft-error tolerance</td>
<td>No</td>
<td>1-bit error correction</td>
<td>1-bit error correction</td>
</tr>
<tr>
<td>Write-error tolerance</td>
<td>No</td>
<td>1-bit error masking</td>
<td>1-bit error masking</td>
</tr>
</tbody>
</table>

Table I. Summary of features of the CMOS/MTJ-based NVFFs.

Figure 9 shows RERs without soft errors in the CMOS/MTJ-based NVFFs, depending on: (a) write time and (b) write energy.

(a) Write time [ns]

(b) Write energy [pJ]
redundancy. In contrast, as the baseline NVFF requires three times larger write energy than that of the conventional and proposed NVFFs, the RER of the baseline NVFF is the largest for the same write energy as shown in Fig. 9(b). As a result, the proposed NVFF achieves around nine orders-of-magnitude reduction in the RER in comparison with the baseline NVFF for the same write energy of 1 pJ.

Figure 10 shows RER vs write energy with soft errors. Soft errors affect the conventional and the baseline NVFFs. In particular, the conventional NVFF is strongly affected. The baseline NVFF mitigates the soft-error effects because of its 1-bit soft-error masking capability. In contrast, the proposed NVFF is not affected by soft errors because of the 1-bit soft-error correction capability. As a result, the proposed design reduces the write energy by around 75% in comparison with the baseline design for an RER of 10\(^{-3}\) and a SER of 10\(^{-3}\).

Figure 11 shows the failure in time (FIT) divided by the number of bits vs the number of backup/restore operations per day (\(N_{br}\)) in the CMOS/MJT-based NVFFs for the same write energy of 1.59 pJ. As shown in the figure, when SER increases, the baseline design is slightly better than the conventional design. The proposed NVFF achieves around 15 orders-of-magnitude reduction in the FIT in comparison with the conventional and baseline NVFFs.

4.3 Performance comparisons in hardware

Table II shows performance comparisons of the slave part of the baseline and proposed NVFFs using 65 nm CMOS/MJT technologies for a write time of 7.95 ns and \(N_{br} = 10,000\). Note that the delay time means that the time gap between an input-signal transition and an output-signal transition, which determines the speed (operating frequency) of the NVFFs. Because of the majority-decision shared writing, the proposed circuit reduces the transistor count and the write energy by 31% and 65%, respectively, in comparison with the baseline circuit. In addition, the proposed circuit achieves a few orders-of-magnitude reduction in the FIT while maintaining a similar delay time and dynamic power dissipation. Note that the clk-to-Q delay is 217 ps in the proposed circuit.

5. Conclusions

In this paper, a soft/write-error resilient CMOS/MJT-based NVFF has been presented. The proposed majority-shared writing scheme addresses two issues of the baseline soft-error-tolerant NVFF, which uses redundant bits. For performance comparisons, both a baseline NVFF and a proposed NVFF are designed and simulated using 65 nm CMOS/MJT technologies and NS-SPICE. As a result, the proposed NVFF achieves a 31% reduction in area and a 65% reduction in write energy in comparison with the baseline NVFF for the same write time. In addition, for the same write energy, the proposed NVFF achieves around 15 orders-of-magnitude reduction in the FIT.

Acknowledgments

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