Three-dimensional monolithic integration of III–V and Si(Ge) FETs for hybrid CMOS and beyond

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Three-dimensional monolithic integration of III–V and Si(Ge) FETs for hybrid CMOS and beyond

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Three-dimensional (3D) monolithic integration can enable higher density and has the potential to stack independently optimized layers at transistor level. Owing to high mobility and lower processing temperatures, InGaAs is well-suited to be used as the top layer channel material in 3D monolithic integration along with Si/SiGe FETs. A review of recent progress to develop InGaAs-on-Si(Ge) 3D Monolithic technology is presented here. © 2017 The Japan Society of Applied Physics

1. Introduction

The conventional CMOS technology or two-dimensional (2D) CMOS technology is facing significant challenges for downsizing the area of circuits in advanced nodes owing to high densities required. Exploiting the third dimension through vertical stacking of device layers presents an interesting opportunity to achieve higher device density without scaling down the dimensions. In this context monolithic 3D (3DM) integration has the potential to achieve very high interconnect densities,1,2) due to very high granularity provided by transistor level stacking. Besides conventional digital circuits,3) it offers the opportunity to stack independently optimized multi-functional layers at transistor level for More-than-Moore technologies.4) Recently, there has been significant effort in developing scalable monolithic 3D integration with group IV semiconductor channels involving Si or Ge FET layer on top of Si/SiGe FET layer.5) However, due to the inherently high thermal budget of Si MOSFET process, monolithic 3D integration of Si(Ge)-on-Si faces a major challenge in terms of degradation of bottom layer FET performance due to the top layer FET thermal budget. This mandates the development of a low temperature process for top layer Si or Si(Ge) FETs while maintaining the device performance. Recent efforts in this direction6,7) demonstrate the significance of this technological challenge.

In this purview, III–V channel FETs (specifically InGaAs based FETs) present an exciting opportunity. As InGaAs based FET process is inherently a lower thermal budget process (typically <650 °C), it brings a native advantage for utilization as top layer FET. Moreover, InGaAs material system is well-known to have higher electron mobility compared to Silicon9) and is being considered as potential n-channel material for scaled CMOS nodes to replace Silicon. Considerable progress has also been made recently in InGaAs based MOSFETs demonstrating high performance at low supply voltages, both on InP substrate,8,9) and on silicon platform.10–12) Besides the recent consideration as n-channel material for CMOS technology, InGaAs based material system has traditionally been utilized as channel in high-electron mobility transistors (HEMTs) for high-frequency applications. Benefiting from the developments made in InGaAs based FETs, impressive cut-off frequencies have been demonstrated in MOS-HEMT and MOSFET architectures.13,14) Thus, a III–V channel material such as InGaAs, has potential to enable both high-performance digital logic as well as high-frequency circuits tightly co-integrated, down to transistor level, in 3D monolithic integration. Therefore one can envisage a truly multi-functional 3D monolithic integration scheme where InGaAs nFETs on top of Si/SiGe FETs can allow higher performance hybrid CMOS and high frequency InGaAs RF-FETs can benefit from closely integrated CMOS circuits.15)

The recent developments towards such a multi-functional hybrid 3D monolithic integration involving III–V (mainly InGaAs based materials) and group IV materials (mainly Si/SiGe) are reviewed here. First of all, efforts involving III–V material integration on Silicon substrate, specifically those that can enable a scalable 3D monolithic platform are reviewed. Then the-state-of-the-art of device integration in such a hybrid 3D monolithic integration is reviewed. Then various works demonstrating both DC and RF performance in a III–V and Si 3D monolithic integration scheme are detailed. Finally, conclusions and future perspectives are discussed.

2. III–V material integration through direct wafer bonding

One of the very important modules in 3D monolithic integration of III–V materials with Si/SiGe is the process of forming III–V channel layer on top of Si/SiGe device layer. For a robust and scalable 3D monolithic integration scheme, it would be advantageous to have a continuous, high-quality film of the channel material. As in the case of SiGe)-on-Si 3D monolithic integration, direct wafer bonding (DBW) (of III–V materials in this case) through oxide–oxide molecular bond provides a scalable and manufacturable approach. Also, DWB process produces very low defect density with major ones being bonding defects due to particulates or outgassing during bonding. Both of these can be controlled with bonding under clean environment and including annealing steps to release trapped gas prior to bonding.

In order to obtain low defectivity channel material, it is essential to grow it on a lattice matched donor substrate. InP is lattice matched InGaAs with 53% In content. Therefore, InP substrates are ideal to be used as donor substrates to transfer InGaAs layer on to Si/SiGe device layer. It is

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essential choosing a bonding oxide that can enable relatively low temperature bonding with high bonding strength. Early work from various groups\cite{17,18} has shown $\text{Al}_2\text{O}_3$ to be excellent material for this purpose. Figure 1 shows the schematic of bonding process with InP donor wafer.

The process starts with growing etch stop layers and final InGaAs channel layer on an InP wafer. Typically this is done on 2-in. InP wafers due to their relative ease of availability and reasonable cost (wafers of higher diameter can be extremely expensive). After growing the channel layer with all the etch stops, a bonding oxide is deposited on top. Next a silicon receiver wafer is deposited with bonding oxide. Thereafter the two wafers are bonded together by bringing oxide surfaces to contact and forming oxide–oxide molecular bond. Afterwards, the InP wafer can either be etched away or cleaved out and recycled if pre-implanted with hydrogen ions as described in Ref. 18. In the case of 3D monolithic integration of III–V and Si/Si(Ge) layers, the receiver wafer has Si/Si(Ge) FET layer processed and an interlayer dielectric deposited, planarized and bonding oxide deposited on top (if different from interlayer dielectric).

As mentioned before, due to lack of availability of large diameter InP wafers at lower cost, the method of transferring top layer from InP donor wafer gets limited to 2-in. diameter. This makes it non-viable for manufacturing. Therefore, it is essential to have method that provides scalability to large area substrates. Recently significant progress has been made in this direction\cite{19,21} and InGaAs-on-insulator (InGaAs-OI) wafer up to 300 mm diameter have been demonstrated.\cite{21} The method consists of first growing strain relaxing metamorphic buffer layers on large area silicon substrates and finally growing the channel material. This process allows to obtain low-defectivity top channel material. The fabrication process of the InGaAs-OI substrate starting from Silicon donor substrate as described in Ref. 20 is shown in Fig. 2.

The donor is InGaAs (53% In content) grown by molecular beam epitaxy (MBE) on a 200 mm Si(100) substrate. Starting from Si substrate, first a 2.5 µm Ge buffer was directly grown on Si followed by 0.5 µm Ga(Al)As and 1.5–2 µm In$_{0.53}$Al$_{0.47}$As metamorphic buffer (MB) and finally 500 nm InGaAs channel (53% In content) material. The wafer was planarized using chemical mechanical polishing (CMP) and a post CMP roughness below 0.4 nm was obtained. After CMP, $\text{Al}_2\text{O}_3$ bonding oxide (BOX) layer was deposited. The donor wafer was subsequently removed by wet-etching and a 200 mm InGaAs-OI substrate was obtained. At this step InGaAs thickness of about 250 nm was obtained. A second CMP step on the InGaAs-OI wafer was used to reduce the active layer thickness to about 50 nm. The reported spectroscopic ellipsometry map of the 200 mm wafer after second CMP step is shown in Fig. 2. The so obtained InGaAs-OI layer was reported to have a defectivity of $3 \times 10^8 \text{cm}^{-2}$.

A similar process but improved to allow donor wafer recycling through SmartCut™ was developed in Ref. 22. InGaAs-OI wafers of 300 mm diameter were demonstrated in this work. The process flow described in Ref. 22 is shown in Fig. 3. Here, the buffer layer consist of GaAs and InP. Prior to oxide–oxide bonding with receiver wafer, H$^+$ implantation is carried out to create defects in InP layer that enable splitting of wafer after bonding. Post-splitting, the donor wafer can be recycled to perform bonding again. 300 mm InGaAs-OI wafer so obtained is shown in Fig. 3.

These methods can be utilized to develop 3D monolithic integration of InGaAs on large area Si/Si(Ge) FET processed wafers. In that case, the Si/Si(Ge) FET layer with interlayer dielectric deposited and planarized will become the receiver wafer.

3. InGaAs-on-Si(Ge) 3D monolithic integration

All the works demonstrating InGaAs-on-Si(Ge) 3D monolithic integration for digital logic have been summarized in Table I.

The first demonstration of InGaAs-on-Ge 3D monolithic integration was carried out by Irisawa et al. as reported in Ref. 23. The work demonstrated, for the first time, 3D monolithic integration of InGaAs nFETs on Ge pFETs. Ge pFETs were fabricated on bulk Ge substrate with a gate-first
flow. Ge pFET source/drain regions were formed by NiGe alloy formation. No implantation or epitaxially grown doped source/drain was used. InGaAs layer (53% In content) was transferred on top of the pFET layer through DWB from 2-in. InP wafer similar to process described in previous section. InGaAs nFETs were also fabricated with gate-first flow and low temperature (<350 °C) Ni–InGaAs alloy formed the source/drain. No impact on Ge pFET performance was observed after nFET fabrication. 3D inverters with top InGaAs nFET and bottom Ge pFET were reported with voltage transfer characteristics (VTC) measured down to \( V_{dd} = 0.2 \) V. Both pFET and nFET had limited drive currents. Although relatively simpler integration scheme was used for pFET and nFETs, it was the first demonstration of 3D monolithic circuits involving InGaAs and Ge devices.

Another important 3D monolithic integration of InGaAs-on-SiGe was demonstrated by the same group (Irisawa et al.24)). The 3D monolithic integration reported was relatively more complex featuring independent back-gates for both top InGaAs nFETs and bottom SiGe-on-insulator (SiGe-OI) pFETs. A schematic of the reported 3D monolithic stack with back-gates for both layers is shown in Fig. 4.

The integration scheme involved fabrication of bottom SiGe-OI p-finFETs through Ge condensation, followed by gate-first flow with Ni–SiGe source/drain. No implantation or RSD was used to form source/drain regions. After bottom SiGe-OI pFET fabrication, back gate for top layer was formed through TaN deposition. Oxide was then deposited on top and InGaAs layer was transferred through DWB. InGaAs nFETs featured fins down to 30 nm. Source/drain regions were formed through Ni–InGaAs alloy. 3D CMOS inverters with symmetric characteristics (down to \( V_{dd} = 0.2 \) V) and 21 stage ring-oscillators were reported with individual back gate tunability. Thus the work demonstrated relatively large circuits with complex 3D monolithic integration. Although, individual FET performances were limited by access resistance, the work demonstrated potential of InGaAs-on-SiGe 3D monolithic integration and advantages of independent back-gate.

Recently, advanced 3D monolithic integration of InGaAs-on-SiGe was demonstrated by Deshpande et al.15) The work featured InGaAs planar and wide-fin nFETs on top of SiGe-OI pFETs. Both layers featured state-of-the-art device integration with top InGaAs nFETs processed with replacement-metal-gate (RMG) flow and bottom SiGe-OI pFETs processed with gate-first (GF) process. The bottom pFETs featured self-aligned raised source/drain (RSD) and salicide process and the top InGaAs nFETs also featured self-aligned RSD. Since silicide on the bottom pFET sets the thermal budget limitation for the top nFET process, having an epitaxially grown RSD process for top nFETs (highest thermal budget of all process steps for top nFET) demonstrated the complete hybrid CMOS process without compromises on either layers. An optimized RSD process for top nFET layer enabled negligible impact on the performance of bottom pFET layer. Figure 5 shows the process flow for the 3D monolithic integration scheme as described in Ref. 15.
Firstly, bottom layer SiGe-OI fin pFETs were fabricated with GF process similar to the one described in Refs. 25 and 26. The process involved thinning of silicon layer of an 8-in. SOI wafer followed by Ge condensation to obtain SiGe-OI layer (with 25% Ge content). Then active pFET areas were formed and gate-stack featuring high-k dielectric and metal gate was deposited. After gate patterning and spacer formation, in-situ doped SiGe epitaxy was carried out to form self-aligned RSD regions. Then NiPt silicidation was performed for low contact resistivity on the pFETs. The thermal budget limit for the top nFET processing is set by the stability of this silicide. The top layer nFET fabrication was carried out after the silicidation step of SiGe-OI fin pFET process. Firstly, an inter-layer oxide was deposited and chemical mechanical planarization (CMP) was carried out. The InGaAs layer was transferred on to this oxide with direct wafer bonding from 2-in. InP donor wafer with the process described in previous section. InGaAs nFET fabrication was then performed with a RMG process described in Ref. 20. This involved patterning the active transistor regions followed by a dummy gate stack deposition. Then NiPt silicidation was performed and chemical mechanical planarization (CMP) was carried out. Thereafter an optimized self-aligned RSD process was carried out. As this step has the highest thermal budget of all the processes involved in top nFET fabrication, it determines the impact on the performance of the bottom pFET. However, this is also a crucial step to obtain high-performance InGaAs nFET as it provides low contact resistivity. The dummy gate replacement was carried out by oxide deposition and CMP to expose the top of dummy gate and selective removal of dummy gate stack. An optimized high-k/metal gate stack was deposited and metal CMP was carried out. Finally, oxide encapsulation was performed and contact holes were opened to both top and bottom layers. Metallization was completed to create contact pads for both layers. It should be noted that owing to different etching depth, bottom layer contacts need to be performed in different lithography step compared to top layer. This leads to density penalty in 3D circuit layout due to overlay margin for two different contact lithography steps. However, this challenge can be overcome by forming an intermediate contact and metal level (inter-tier vias). Cross section TEM images of the reported 3D monolithic integration is shown in Fig. 6.

The reported DC transfer characteristics of the top layer InGaAs nFET featuring a gate length of 70 nm and a bottom layer SiGe-OI pFET featuring a gate length of 25 nm are shown in Figs. 7 and 8 respectively. SiGe-OI pFET shows excellent electrostatic integrity ($SS_{Sat} = 81 \text{ mV/dec}$, DIBL = 48 mV/V) at $L_g = 25 \text{ nm}$ owing to the optimized process (Refs. 25 and 26). InGaAs nFET reported is a planar FET.
and demonstrates competitive electrostatic integrity ($SS_{sat} = 96$ mV/dec, DIBL = 83 mV/V) at $L_g = 70$ nm.

The DIBL and $SS_{sat}$ roll-off characteristics of the nFET were also reported and are shown in Figs. 9 and 10. Well-controlled nFET scaling behavior was demonstrated and the performance was close to previously reported InGaAs-OI RMG FinFETs by the same group. Thus, independent optimized process for both layers developed separately, were brought together in one 3D monolithic integration scheme without adverse performance impact.

The impact on pFET characteristics post top nFET fabrication is the ultimate test for the feasibility of 3D monolithic integration scheme. The reported comparison of bottom pFET $I_d-V_g$ before and after top nFET fabrication is shown in Fig. 11. Almost comparable $I_{th(n)}$ was obtained post nFET process, indicating very minimal impact on pFET silicidation. DIBL and $SS_{sat}$ roll-offs for pFETs were also compared pre and post nFET fabrication. Very minimal change was observed post nFET process as shown in Fig. 12.

Thus the feasibility of InGaAs-on-SiGe 3D monolithic integration was demonstrated. Voltage transfer characteristics (VTC) of scaled 3D inverters with nFET $L_g = 80$ nm and $L_g \sim 30$ nm (for both nFET and pFET) were also reported shown in Figs. 13(a) and 13(b) respectively. Well-behaved transitions were obtained down to $V_{dd} = 0.25$ V. The VTC were not symmetric owing to mis-match in pFET and nFET device performances.

### 3.1 Top layer InGaAs RFFETs

As mentioned earlier, III–V channel materials are well-suited for high-frequency devices. Integrating them in a 3D monolithic scheme on top of Si/SiGe provides opportunity to realize mixed signal circuits. Recent simulation work has shown benefits of III–V high frequency devices co-integrated with Si CMOS. First efforts to characterize the RF performance of InGaAs FETs integrated on top of SiGe pFETs have recently been reported. The InGaAs RFFETs were fabricated along with the DC FETs detailed in the previous section. In order to enable RF characterization of top layer InGaAs nFETs, their layout consisted of multi-

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Fig. 9. DIBL vs $L_g$ characteristics for top layer InGaAs nFETs. Adapted from Ref. 15.

Fig. 10. $SS_{sat}$ vs $L_g$ characteristics for top layer InGaAs nFETs. Adapted from Ref. 15.

Fig. 11. (Color online) Comparison of bottom layer SiGe-OI pFET $I_d-V_g$ characteristics before and after top layer nFET fabrication as reported in Ref. 15.

Fig. 12. (Color online) Comparison of bottom layer SiGe-OI pFET DIBL and $SS_{sat}$ vs $L_g$ characteristics before and after top layer nFET fabrication as reported in Ref. 15.
finger gates with a ground–signal–ground (GSG) pad configuration. A device reported in Ref. 28 featured 10 parallel finger gates, each with a width of 2 µm (= total device width of 20 µm). DC $I_d$–$V_g$ characteristics reported are shown in Fig. 14.

The current gain ($h_{21}$) (dB) vs frequency is shown in Fig. 15, for a device with $L_g = 120$ nm. A cut-off frequency ($f_t$) of 16.4 GHz was obtained for $V_{ds} = 1$ V. Although this is relatively lower value than typical InGaAs HEMTs or MOS-HEMTs, it should be noted that the device structure was not optimized for RF performance and hence further optimization could enable higher cut-off frequencies.

Besides this, recent work from Lee et al. has shown layer transfer of various III–V materials on large area CMOS processed Si wafers through wafer bonding. This group has further demonstrated III–V HEMT elements on Si CMOS wafers on these transferred layers. Various other functional elements such LEDs have also been shown. These are very encouraging results showing diversification of InGaAs-on-Si(Ge) 3D monolithic integration platform towards “More-than-Moore” applications.

4. Conclusions

3D monolithic integration of III–V MOSFETs on top of Si/Si(Ge) provides opportunity achieving both high performance, dense CMOS as well as mixed-signal applications. It can become a truly multi-functional platform bringing best of III–V world and conventional Si/Si(Ge) CMOS world. Recently progress in this context were reviewed, starting from III–V material integration to 3D monolithic integration with state-of-the-art process flows and 3D circuits. Significant progress has been made in upscaling the III–V wafer bonding to 300 mm wafer sizes. This will become key enabler for a feasible InGaAs-on-Si(Ge) 3D monolithic technology. Progress made in advanced device integration in 3D monolithic scheme demonstrates that no major hurdles are present to realize a high-performance 3D hybrid CMOS. As a step further, improving performance of III–V devices (in 3D monolithic scheme) to the level shown on InP substrates needs to be achieved. Also, demonstration of 3D monolithic integration of InGaAs-on-Si(Si(Ge) through layer transfer on 300 nm wafer size will be significant step forward towards a manufacturable platform. Thus, exciting prospects exist for realizing a hetero-integrated 3D monolithic platform with high-mobility III–V materials.

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